

**600mA CMOS LDO REGULATOR WITH ENABLE**
**AP2112**

### General Description

The AP2112 is CMOS process low dropout linear regulator with enable function, the regulator delivers a guaranteed 600mA (min.) continuous load current.

The AP2112 provides 1.2V, 1.8V, 2.5V, 2.6V and 3.3V regulated output, and provides excellent output accuracy 1.5%, also provides an excellent load regulation, line regulation and excellent load transient performance due to very fast loop response. The AP2112 has built-in auto discharge function.

The regulator features low power consumption, and provides SOT-23-5, SOT-89-5, and SOIC-8 packages.

### Features

- Output voltage accuracy:  $\pm 1.5\%$
- Output Current: 600mA (Min.)
- Foldback Short Current Protection: 50mA
- Enable Function to Turn ON/OFF  $V_{OUT}$
- Low Dropout Voltage (3.3V): 250mV (Typ.) @  $I_{OUT}=600mA$
- Excellent Load Regulation: 0.2%/A (Typ.)
- Excellent Line Regulation: 0.02%/V (Typ.)
- Low Quiescent Current: 55 $\mu A$  (Typ.)
- Low Standby Current: 0.01 $\mu A$  (Typ.)
- Low Output Noise: 50 $\mu V_{RMS}$
- PSRR: 100Hz -65dB, 1k -65dB
- OTSD Protection
- Stable with 1.0 $\mu F$  Flexible Cap: Ceramic, Tantalum and Aluminum Electrolytic
- Operation Temperature Range: -40°C to 85°C
- ESD: MM 400V, HBM 4000V

### Applications

- Laptop computer
- Potable DVD
- LCD Monitor

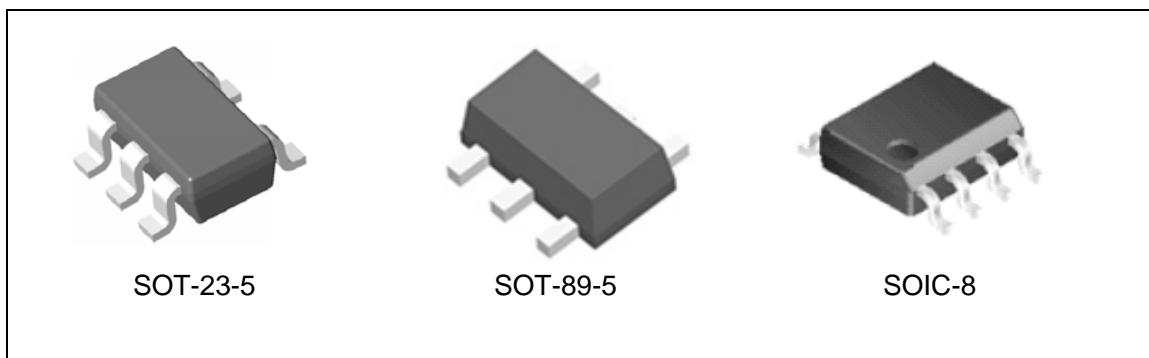


Figure 1. Package Type of AP2112

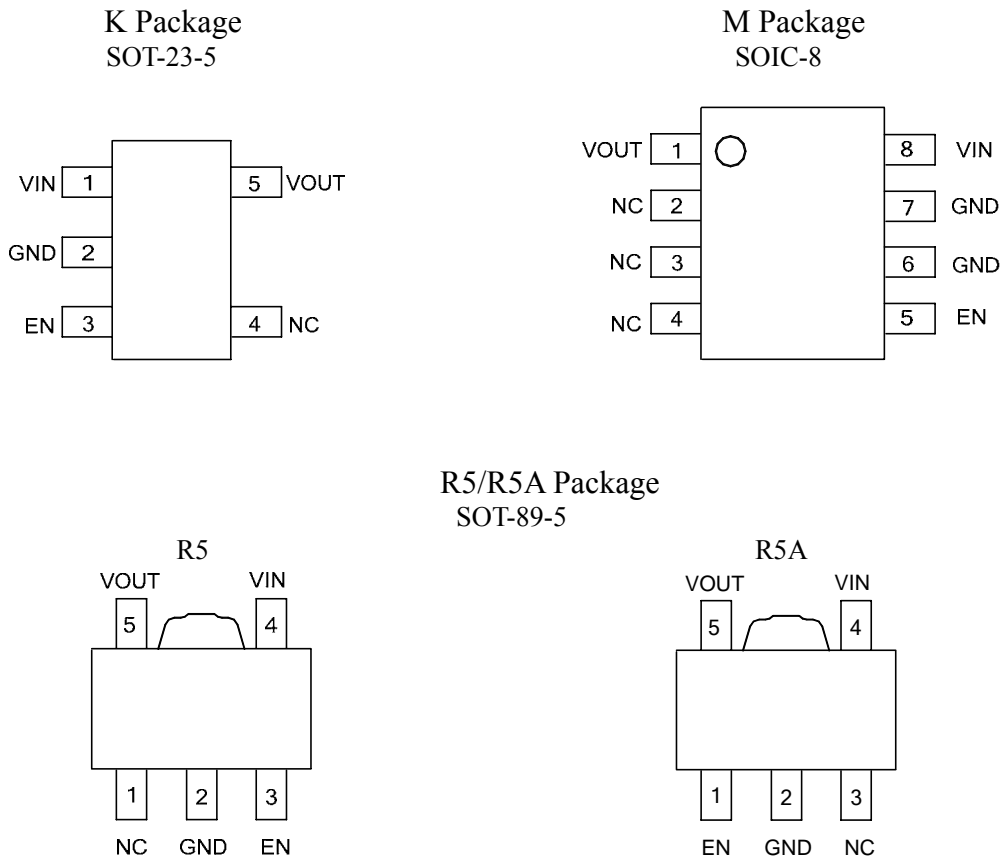
**600mA CMOS LDO REGULATOR WITH ENABLE**
**AP2112**
**Pin Configuration**


Figure 2. Pin Configuration of AP2112 (Top View)

**Pin Descriptions**

PIN No.			Name	Descriptions
SOT-23-5	SOT-89-5	SOIC-8		
1	4	8	VIN	Input Voltage
2	2	6, 7	GND	GND
3	3 (R5)	5	EN	Chip Enable, H – normal work, L – shutdown output
	1 (R5A)			
4	1 (R5)	2, 3, 4	NC	No Connection
	3 (R5A)			
5	5	1	VOUT	Output Voltage

**Functional Block Diagram**

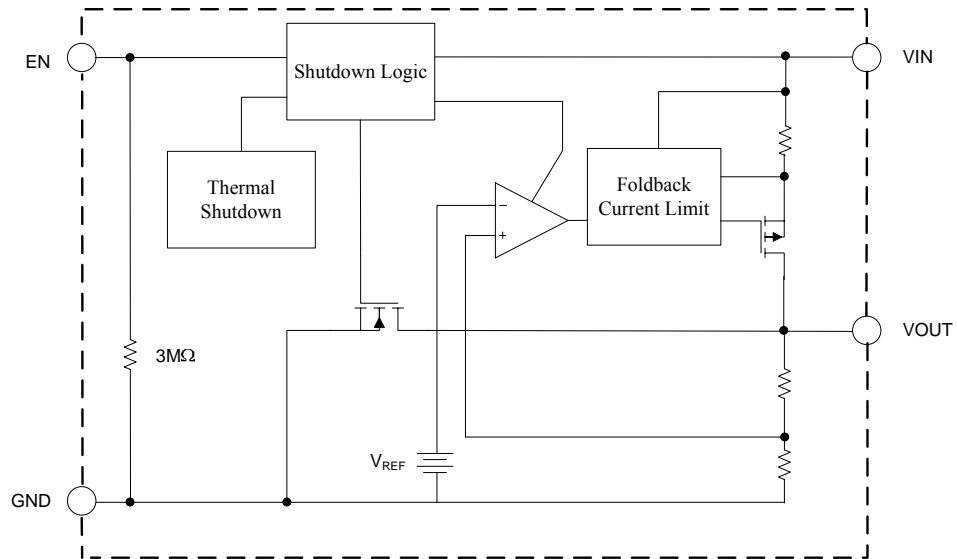


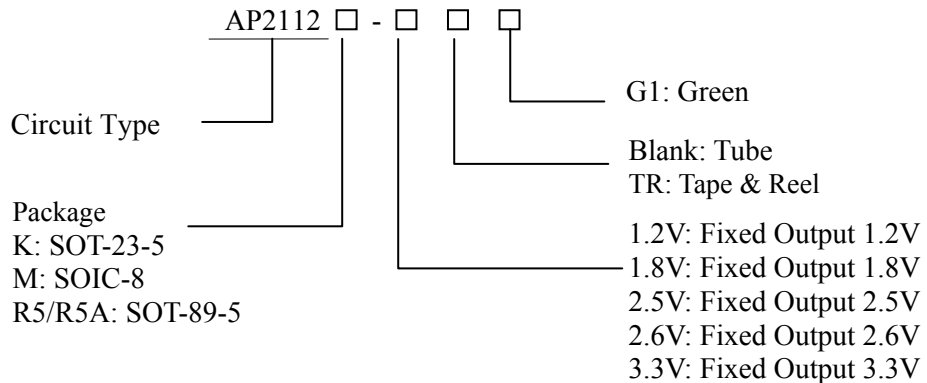
Figure 3. Functional Block Diagram of AP2112



**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Ordering Information**



Package	Temperature Range	Condition	Part Number	Marking ID	Packing Type
SOT-23-5	-40 to 85°C	1.2V	AP2112K-1.2TRG1	G3L	Tape & Reel
		1.8V	AP2112K-1.8TRG1	G3M	Tape & Reel
		2.5V	AP2112K-2.5TRG1	G3N	Tape & Reel
		2.6V	AP2112K-2.6TRG1	G5N	Tape & Reel
		3.3V	AP2112K-3.3TRG1	G3P	Tape & Reel
SOIC-8	-40 to 85°C	1.2V	AP2112M-1.2G1	2112M-1.2G1	Tube
			AP2112M-1.2TRG1	2112M-1.2G1	Tape & Reel
		1.8V	AP2112M-1.8G1	2112M-1.8G1	Tube
			AP2112M-1.8TRG1	2112M-1.8G1	Tape & Reel
		2.5V	AP2112M-2.5G1	2112M-2.5G1	Tube
			AP2112M-2.5TRG1	2112M-2.5G1	Tape & Reel
		2.6V	AP2112M-2.6G1	2112M-2.6G1	Tube
			AP2112M-2.6TRG1	2112M-2.6G1	Tape & Reel
		3.3V	AP2112M-3.3G1	2112M-3.3G1	Tube
			AP2112M-3.3TRG1	2112M-3.3G1	Tape & Reel
SOT-89-5	-40 to 85°C	1.2V(R5)	AP2112R5-1.2TRG1	G37D	Tape & Reel
		1.8V(R5)	AP2112R5-1.8TRG1	G37E	Tape & Reel
		2.5V(R5)	AP2112R5-2.5TRG1	G37F	Tape & Reel
		2.6V(R5)	AP2112R5-2.6TRG1	G13F	Tape & Reel
		3.3V(R5)	AP2112R5-3.3TRG1	G37G	Tape & Reel
SOT-89-5	-40 to 85°C	1.2V(R5A)	AP2112R5A-1.2TRG1	G33C	Tape & Reel
		1.8V(R5A)	AP2112R5A-1.8TRG1	G33E	Tape & Reel
		2.5V(R5A)	AP2112R5A-2.5TRG1	G28G	Tape & Reel
		2.6V(R5A)	AP2112R5A-2.6TRG1	G13E	Tape & Reel
		3.3V(R5A)	AP2112R5A-3.3TRG1	G28H	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and Green.

**600mA CMOS LDO REGULATOR WITH ENABLE****AP2112****Absolute Maximum Ratings (Note 1)**

Parameter		Symbol	Value	Unit	
Power Supply Voltage		$V_{CC}$	6.5	V	
Operating Junction Temperature Range		$T_J$	150	°C	
Storage temperature Range		$T_{STG}$	-65 to 150	°C	
Lead Temperature (Soldering, 10 Seconds)		$T_{LEAD}$	260	°C	
Thermal Resistance (Junction to Ambient) (No heatsink)		$\theta_{JA}$	SOT-23-5	184	°C/W
			SOIC-8	114	
			SOT-89-5	120	
ESD	Machine Model		400	V	
	Human Body Model		4000	V	

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_{IN}$	2.5	6.0	V
Ambient Operation Temperature Range	$T_A$	-40	85	°C



**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Electrical Characteristics**

**AP2112-1.2 Electrical Characteristic (Note 2)**

V<sub>IN</sub>=2.5V, C<sub>IN</sub>=1.0μF (Ceramic), C<sub>OUT</sub>=1.0μF (Ceramic), Typical T<sub>A</sub>= 25°C, **Bold** typeface applies over -40°C≤T<sub>J</sub>≤85°C ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V <sub>OUT</sub>	V <sub>IN</sub> =2.5V, 1mA ≤ I <sub>OUT</sub> ≤ 30mA	<b>V<sub>OUT</sub></b> *98.5%	1.2	<b>V<sub>OUT</sub></b> *101.5%	V
Maximum Output Current	I <sub>OUT(MAX)</sub>	V <sub>IN</sub> =2.5V, V <sub>OUT</sub> =1.182V to 1.218V	<b>600</b>			mA
Load Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	V <sub>IN</sub> =2.5V, 1mA ≤ I <sub>OUT</sub> ≤ 600mA		0.2	±0.1	%/A
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	2.5V ≤ V <sub>IN</sub> ≤ 6V, I <sub>OUT</sub> =30mA		0.02		%/V
Dropout Voltage	V <sub>DROP</sub>	I <sub>OUT</sub> =10mA		1000	1300	mV
		I <sub>OUT</sub> =300mA		1000	1300	
		I <sub>OUT</sub> =600mA		1000	1300	
Quiescent Current	I <sub>Q</sub>	V <sub>IN</sub> =2.5V, I <sub>OUT</sub> =0mA		55	80	μA
Standby Current	I <sub>STD</sub>	V <sub>IN</sub> =2.5V, V <sub>EN</sub> in OFF mode		0.01	1.0	μA
Power Supply Rejection Ratio	PSRR	Ripple 0.5Vp-p V <sub>IN</sub> =2.5V, I <sub>OUT</sub> =100mA	f=100Hz		65	dB
			f=1KHz		65	
Output Voltage Temperature Coefficient	$(\Delta V_{OUT}/V_{OUT})/\Delta T$	I <sub>OUT</sub> =30mA T <sub>A</sub> = -40°C to 85°C		±100		ppm
Short Current Limit	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V		50		mA
RMS Output Noise	V <sub>NOISE</sub>	No Load, 10Hz ≤ f ≤ 100kHz		50		μV <sub>RMS</sub>
V <sub>EN</sub> High Voltage	V <sub>IH</sub>	Enable logic high, regulator on	1.5		6.0	V
V <sub>EN</sub> Low Voltage	V <sub>IL</sub>	Enable logic low, regulator off	0		0.4	
Start-up Time	T <sub>S</sub>	No Load		20		μs
EN Pull Down Resistor	R <sub>PD</sub>			3.0		MΩ
V <sub>OUT</sub> discharge Resistor	R <sub>DCHG</sub>	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T <sub>OTSD</sub>			160		°C
Thermal Shutdown Hysteresis	T <sub>HYOTSD</sub>			25		
Thermal Resistance	θ <sub>JC</sub>	SOT-23-5		96		°C/W
		SOIC-8		75		
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at T<sub>A</sub>=25°C. Over temperature specifications guaranteed by design only.



**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Electrical Characteristics (Continued)**

**AP2112-1.8 Electrical Characteristic (Note 2)**

V<sub>IN</sub>=2.8V, C<sub>IN</sub>=1μF (Ceramic), C<sub>OUT</sub>=1μF (Ceramic), Typical T<sub>A</sub> = 25°C, **Bold** typeface applies over -40°C≤T<sub>J</sub>≤85°C ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V <sub>OUT</sub>	V <sub>IN</sub> =2.8V, 1mA ≤ I <sub>OUT</sub> ≤ 30mA	<b>V<sub>OUT</sub></b> *98.5%	1.8	<b>V<sub>OUT</sub></b> *101.5%	V
Maximum Output Current	I <sub>OUT(MAX)</sub>	V <sub>IN</sub> =2.8V, V <sub>OUT</sub> =1.773V to 1.827V	<b>600</b>			mA
Load Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	V <sub>OUT</sub> =1.8V, V <sub>IN</sub> =V <sub>OUT</sub> +1V, 1mA ≤ I <sub>OUT</sub> ≤ 600mA		0.2		%/A
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	2.8V ≤ V <sub>IN</sub> ≤ 6V, I <sub>OUT</sub> =30mA		0.02	±0.1	%/V
Dropout Voltage	V <sub>DROP</sub>	I <sub>OUT</sub> =10mA		500	700	mV
		I <sub>OUT</sub> =300mA		500	700	
		I <sub>OUT</sub> =600mA		500	700	
Quiescent Current	I <sub>Q</sub>	V <sub>IN</sub> =2.8V, I <sub>OUT</sub> =0mA		55	80	μA
Standby Current	I <sub>STD</sub>	V <sub>IN</sub> =2.8V, V <sub>EN</sub> in OFF mode		0.01	1.0	μA
Power Supply Rejection Ratio	PSRR	Ripple 0.5Vp-p V <sub>IN</sub> =2.8V, I <sub>OUT</sub> =100mA	f=100Hz	65		dB
			f=1KHz	65		
Output Voltage Temperature Coefficient	$(\Delta V_{OUT}/V_{OUT})/\Delta T$	I <sub>OUT</sub> =30mA T <sub>A</sub> = -40°C to 85°C		±100		ppm
Short Current Limit	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V		50		mA
RMS Output Noise	V <sub>NOISE</sub>	No Load, 10Hz ≤ f ≤ 100kHz		50		μV <sub>RMS</sub>
V <sub>EN</sub> High Voltage	V <sub>IH</sub>	Enable logic high, regulator on	1.5		6.0	V
V <sub>EN</sub> Low Voltage	V <sub>IL</sub>	Enable logic low, regulator off	0		0.4	
Start-up Time	T <sub>S</sub>	No Load		20		μs
EN Pull Down Resistor	R <sub>PD</sub>			3.0		MΩ
V <sub>OUT</sub> Discharge Resistor	R <sub>DCHG</sub>	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T <sub>OTSD</sub>			160		°C
Thermal Shutdown Hysteresis	T <sub>HYOTSD</sub>			25		
Thermal Resistance	θ <sub>JC</sub>	SOT-23-5		96		°C/W
		SOIC-8		75		
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at T<sub>A</sub>=25°C. Over temperature specifications guaranteed by design only.



**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Electrical Characteristics (Continued)**

**AP2112-2.5 Electrical Characteristic (Note 2)**

V<sub>IN</sub>=3.5V, C<sub>IN</sub>=1μF (Ceramic), C<sub>OUT</sub>=1μF (Ceramic), Typical T<sub>A</sub> = 25°C, **Bold** typeface applies over -40°C≤T<sub>J</sub>≤85°C ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V <sub>OUT</sub>	V <sub>IN</sub> =3.5V, 1mA ≤ I <sub>OUT</sub> ≤ 30mA	<b>V<sub>OUT</sub></b> *98.5%	2.5	<b>V<sub>OUT</sub></b> *101.5%	V
Maximum Output Current	I <sub>OUT(MAX)</sub>	V <sub>IN</sub> =3.5V, V <sub>OUT</sub> =2.463V to 2.537V	<b>600</b>			mA
Load Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	V <sub>OUT</sub> =2.5V, V <sub>IN</sub> =V <sub>OUT</sub> +1V, 1mA ≤ I <sub>OUT</sub> ≤ 600mA		0.2		%/A
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	3.5V ≤ V <sub>IN</sub> ≤ 6V, I <sub>OUT</sub> =30mA		0.02	±0.1	%/V
Dropout Voltage	V <sub>DROP</sub>	I <sub>OUT</sub> =10mA		5	8	mV
		I <sub>OUT</sub> =300mA		125	200	
		I <sub>OUT</sub> =600mA		250	400	
Quiescent Current	I <sub>Q</sub>	V <sub>IN</sub> =3.5V, I <sub>OUT</sub> =0mA		55	80	μA
Standby Current	I <sub>STD</sub>	V <sub>IN</sub> =3.5V, V <sub>EN</sub> in OFF mode		0.01	1.0	μA
Power Supply Rejection Ratio	PSRR	Ripple 0.5Vp-p V <sub>IN</sub> =3.5V, I <sub>OUT</sub> =100mA	f=100Hz	65		dB
			f=1KHz	65		
Output Voltage Temperature Coefficient	$(\Delta V_{OUT}/V_{OUT})/\Delta T$	I <sub>OUT</sub> =30mA T <sub>A</sub> = -40°C to 85°C		±100		ppm
Short Current Limit	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V		50		mA
RMS Output Noise	V <sub>NOISE</sub>	No Load, 10Hz ≤ f ≤ 100kHz		50		μV <sub>RMS</sub>
V <sub>EN</sub> High Voltage	V <sub>IH</sub>	Enable logic high, regulator on	1.5		6.0	V
V <sub>EN</sub> Low Voltage	V <sub>IL</sub>	Enable logic low, regulator off	0		0.4	
Start-up Time	T <sub>S</sub>	No Load		20		μs
EN Pull Down Resistor	R <sub>PD</sub>			3.0		MΩ
V <sub>OUT</sub> Discharge Resistor	R <sub>DCHG</sub>	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T <sub>OTSD</sub>			160		°C
Thermal Shutdown Hysteresis	T <sub>HYOTSD</sub>			25		
Thermal Resistance	θ <sub>JC</sub>	SOT-23-5		96		°C /W
		SOIC-8		75		
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at T<sub>A</sub> = 25°C. Over temperature specifications guaranteed by design only.





**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Electrical Characteristics (Continued)**

**AP2112-2.6 Electrical Characteristic (Note 2)**

V<sub>IN</sub>=3.6V, C<sub>IN</sub>=1μF (Ceramic), C<sub>OUT</sub>=1μF (Ceramic), Typical T<sub>A</sub> = 25°C, **Bold** typeface applies over -40°C≤T<sub>J</sub>≤85°C ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V <sub>OUT</sub>	V <sub>IN</sub> =3.6V, 1mA ≤ I <sub>OUT</sub> ≤ 30mA	<b>V<sub>OUT</sub></b> *98.5%	2.6	<b>V<sub>OUT</sub></b> *101.5%	V
Maximum Output Current	I <sub>OUT(MAX)</sub>	V <sub>IN</sub> =3.6V, V <sub>OUT</sub> =2.561V to 2.639V	<b>600</b>			mA
Load Regulation	(ΔV <sub>OUT</sub> /V <sub>OUT</sub> )/ ΔI <sub>OUT</sub>	V <sub>OUT</sub> =2.6V, V <sub>IN</sub> =V <sub>OUT</sub> +1V, 1mA ≤ I <sub>OUT</sub> ≤ 600mA		<b>0.2</b>		%/A
Line Regulation	(ΔV <sub>OUT</sub> /V <sub>OUT</sub> )/ ΔV <sub>IN</sub>	3.6V ≤ V <sub>IN</sub> ≤ 6V, I <sub>OUT</sub> =30mA		<b>0.02</b>	±0.1	%/V
Dropout Voltage	V <sub>DROP</sub>	I <sub>OUT</sub> =10mA		<b>5</b>	<b>8</b>	mV
		I <sub>OUT</sub> =300mA		<b>125</b>	<b>200</b>	
		I <sub>OUT</sub> =600mA		<b>250</b>	<b>400</b>	
Quiescent Current	I <sub>Q</sub>	V <sub>IN</sub> =3.6V, I <sub>OUT</sub> =0mA		<b>55</b>	<b>80</b>	μA
Standby Current	I <sub>STD</sub>	V <sub>IN</sub> =3.6V, V <sub>EN</sub> in OFF mode		<b>0.01</b>	<b>1.0</b>	μA
Power Supply Rejection Ratio	PSRR	Ripple 0.5Vp-p V <sub>IN</sub> =3.6V, I <sub>OUT</sub> =100mA	f=100Hz		<b>65</b>	dB
			f=1KHz		<b>65</b>	
Output Voltage Temperature Coefficient	(ΔV <sub>OUT</sub> /V <sub>OUT</sub> )/ ΔT	I <sub>OUT</sub> =30mA T <sub>A</sub> = -40°C to 85°C		<b>±100</b>		ppm
Short Current Limit	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V		<b>50</b>		mA
RMS Output Noise	V <sub>NOISE</sub>	No Load, 10Hz ≤ f ≤ 100kHz		<b>50</b>		μV <sub>RMS</sub>
V <sub>EN</sub> High Voltage	V <sub>IH</sub>	Enable logic high, regulator on	<b>1.5</b>		<b>6.0</b>	V
V <sub>EN</sub> Low Voltage	V <sub>IL</sub>	Enable logic low, regulator off	<b>0</b>		<b>0.4</b>	
Start-up Time	T <sub>S</sub>	No Load		<b>20</b>		μs
EN Pull Down Resistor	R <sub>PD</sub>			<b>3.0</b>		MΩ
V <sub>OUT</sub> Discharge Resistor	R <sub>DCHG</sub>	Set EN pin at Low		<b>60</b>		Ω
Thermal Shutdown Temperature	T <sub>OTSD</sub>			<b>160</b>		°C
Thermal Shutdown Hysteresis	T <sub>HYOTSD</sub>			<b>25</b>		
Thermal Resistance	θ <sub>JC</sub>	SOT-23-5		<b>96</b>		°C /W
		SOIC-8		<b>75</b>		
		SOT-89-5		<b>47</b>		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at T<sub>A</sub> = 25°C. Over temperature specifications guaranteed by design only.



**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Electrical Characteristics (Continued)**

**AP2112-3.3 Electrical Characteristic (Note 2)**

V<sub>IN</sub>=4.3V, C<sub>IN</sub>=1μF (Ceramic), C<sub>OUT</sub>=1μF (Ceramic), Typical T<sub>A</sub> = 25°C, **Bold** typeface applies over -40°C≤T<sub>J</sub>≤85°C ranges, unless otherwise specified (Note 3).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V <sub>OUT</sub>	V <sub>IN</sub> =4.3V, 1mA ≤ I <sub>OUT</sub> ≤ 30mA	<b>V<sub>OUT</sub></b> *98.5%	3.3	<b>V<sub>OUT</sub></b> *101.5%	V
Maximum Output Current	I <sub>OUT(MAX)</sub>	V <sub>IN</sub> =4.3V, V <sub>OUT</sub> =3.251V to 3.350V	<b>600</b>			mA
Load Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	V <sub>IN</sub> =4.3V, 1mA ≤ I <sub>OUT</sub> ≤ 600mA		0.2		%/A
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	4.3V ≤ V <sub>IN</sub> ≤ 6V, I <sub>OUT</sub> =30mA		0.02	±0.1	%/V
Dropout Voltage	V <sub>DROP</sub>	I <sub>OUT</sub> =10mA		5	8	mV
		I <sub>OUT</sub> =300mA		125	200	
		I <sub>OUT</sub> =600mA		250	400	
Quiescent Current	I <sub>Q</sub>	V <sub>IN</sub> =4.3V, I <sub>OUT</sub> =0mA		55	80	μA
Standby Current	I <sub>STD</sub>	V <sub>IN</sub> =4.3V, V <sub>EN</sub> in OFF mode		0.01	1.0	μA
Power Supply Rejection Ratio	PSRR	Ripple 0.5Vp-p V <sub>IN</sub> =4.3V, I <sub>OUT</sub> =100mA	f=100Hz	65		dB
			f=1KHz	65		
Output Voltage Temperature Coefficient	$(\Delta V_{OUT}/V_{OUT})/\Delta T$	I <sub>OUT</sub> =30mA T <sub>A</sub> = -40°C to 85°C		±100		ppm
Short Current Limit	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V		50		mA
RMS Output Noise	V <sub>NOISE</sub>	No Load, 10Hz ≤ f ≤ 100kHz		50		μV <sub>RMS</sub>
V <sub>EN</sub> High Voltage	V <sub>IH</sub>	Enable logic high, regulator on	1.5		6.0	V
V <sub>EN</sub> Low Voltage	V <sub>IL</sub>	Enable logic low, regulator off	0		0.4	
Start-up Time	T <sub>S</sub>	No Load		20		μs
EN Pull Down Resistor	R <sub>PD</sub>			3.0		MΩ
V <sub>OUT</sub> Discharge Resistor	R <sub>DCHG</sub>	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T <sub>OTSD</sub>			160		°C
Thermal Shutdown Hysteresis	T <sub>HYOTSD</sub>			25		
Thermal Resistance	θ <sub>JC</sub>	SOT-23-5		96		°C /W
		SOIC-8		75		
		SOT-89-5		47		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at T<sub>A</sub> = 25°C. Over temperature specifications guaranteed by design only.



Typical Performance Characteristics

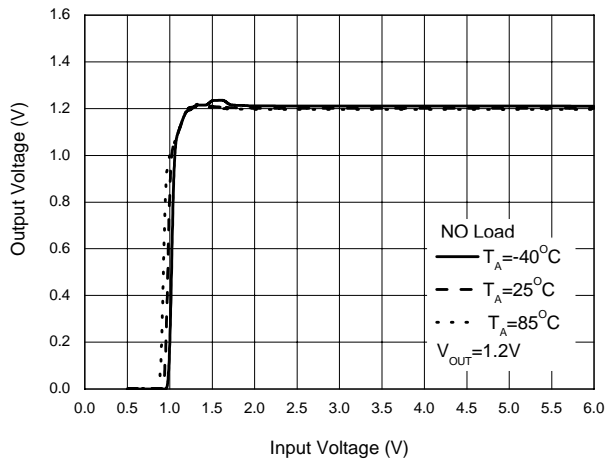


Figure 4. Output Voltage vs. Input Voltage

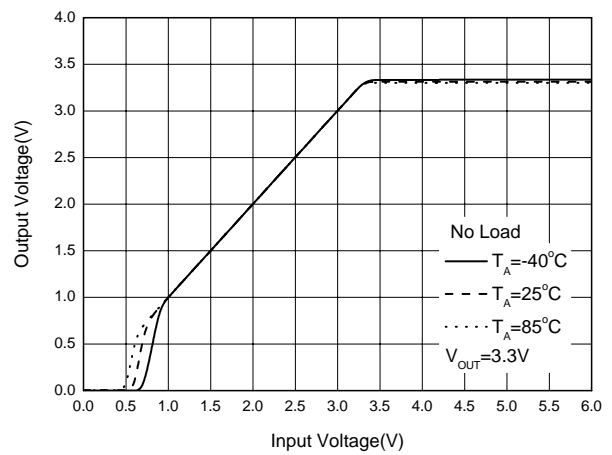


Figure 5. Output Voltage vs. Input Voltage

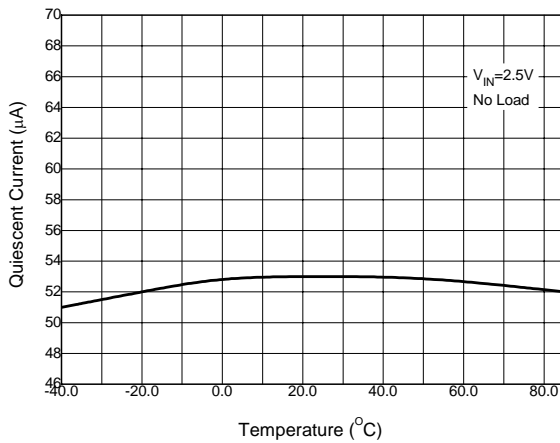


Figure 6. Quiescent Current vs. Temperature

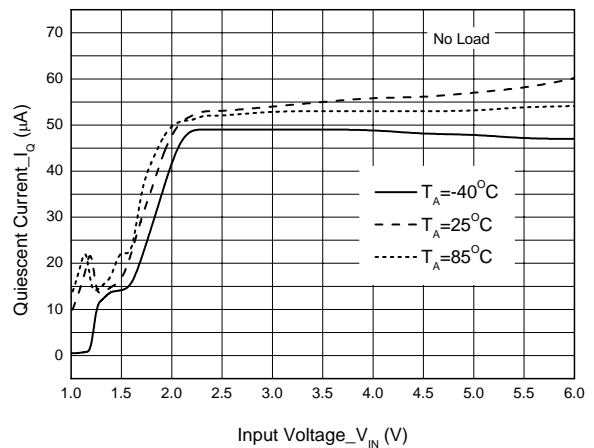


Figure 7. Quiescent Current vs. Input Voltage



Typical Performance Characteristics (Continued)

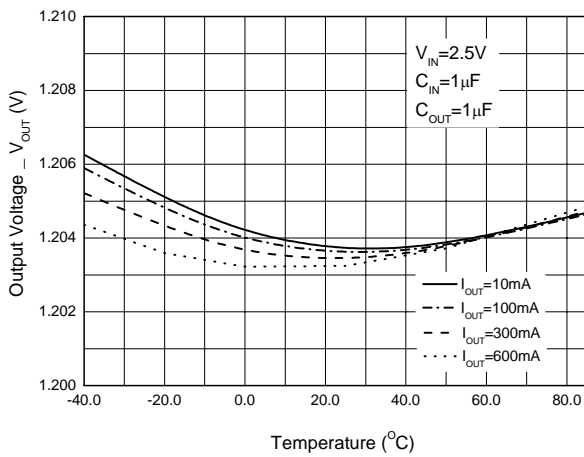


Figure 8. Output Voltage vs. Temperature

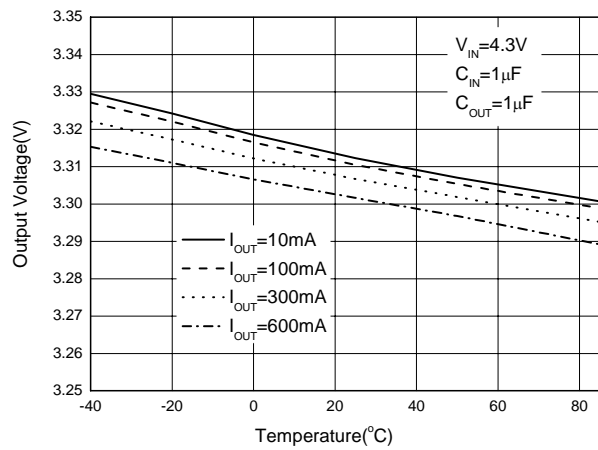


Figure 9. Output Voltage vs. Temperature

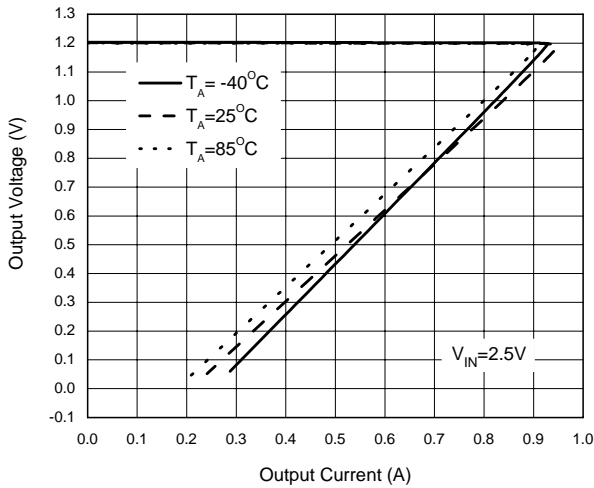


Figure 10. Output Voltage vs. Output Current

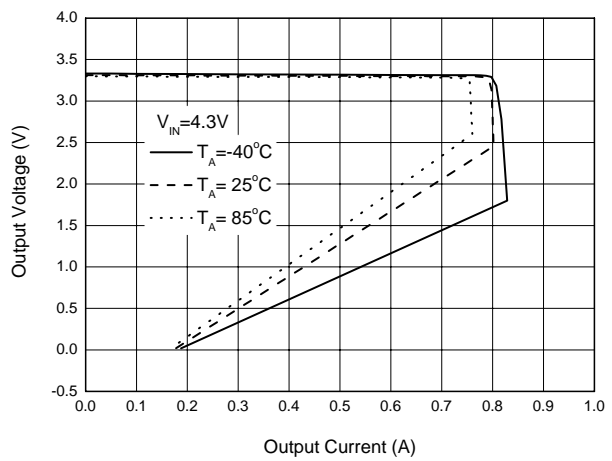


Figure 11. Output Voltage vs. Output Current

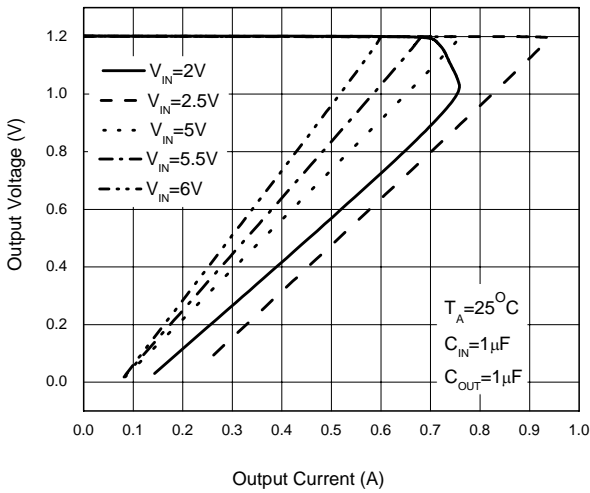
**Typical Performance Characteristics (Continued)**


Figure 12. Output Voltage vs. Output Current

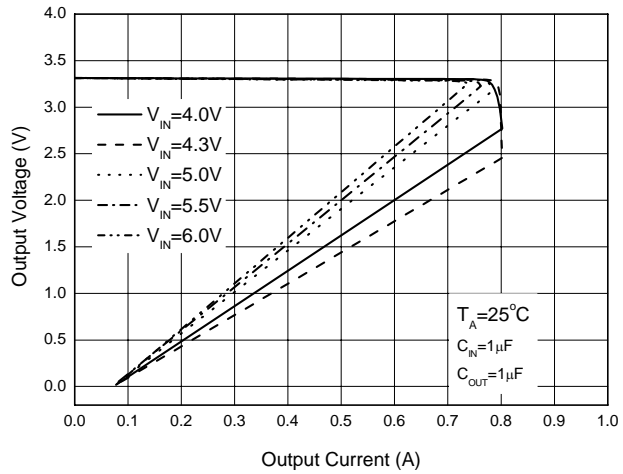


Figure 13. Output Voltage vs. Output Current

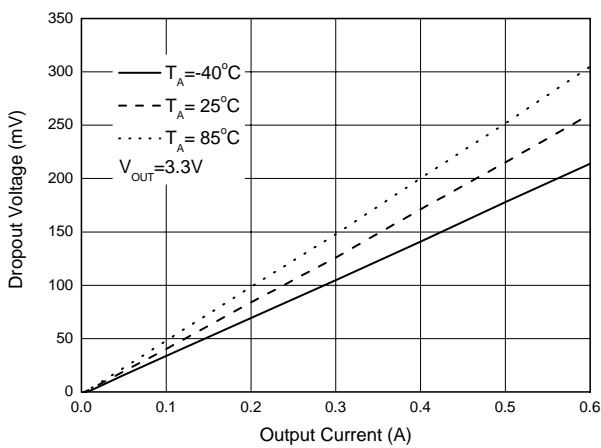


Figure 14. Dropout Voltage vs. Output Current

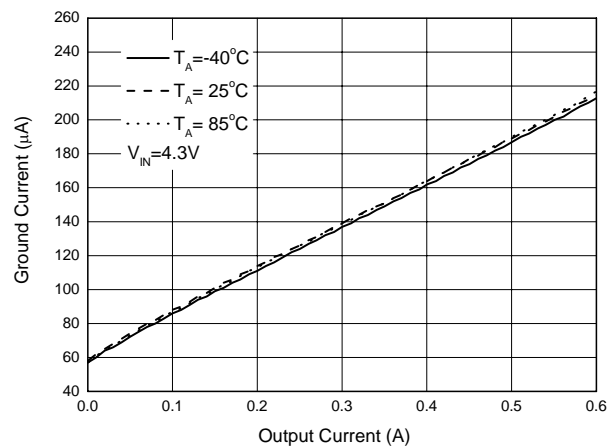


Figure 15. Ground Current vs. Output Current

**Typical Performance Characteristics (Continued)**

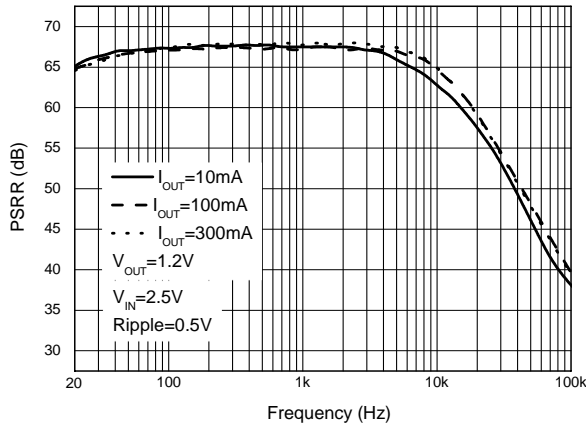


Figure 16. PSRR vs. Frequency

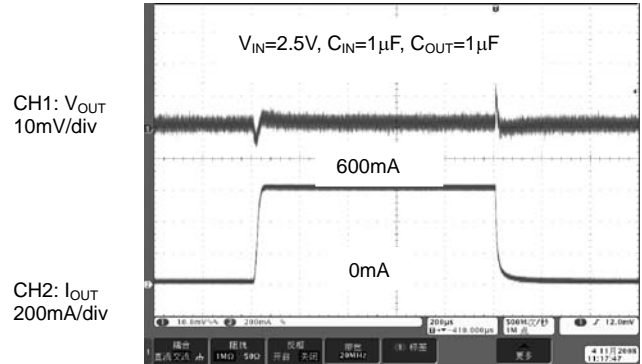


Figure 17. Load Transient

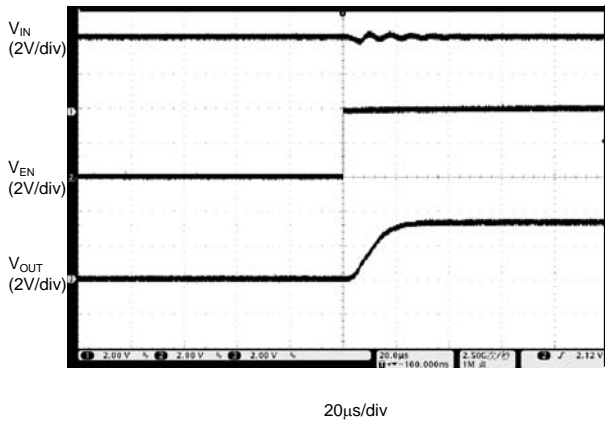


Figure 18. Enable On

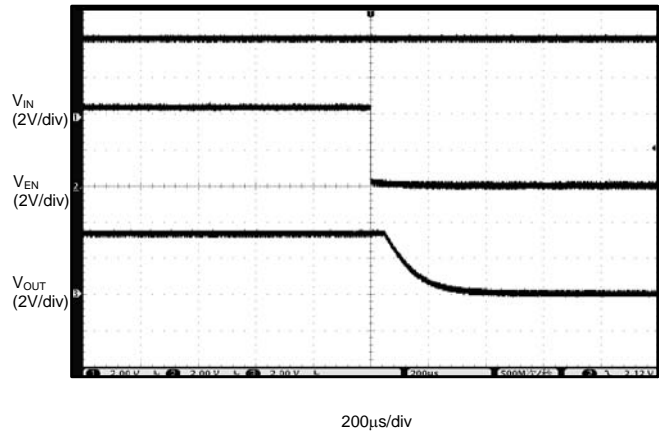
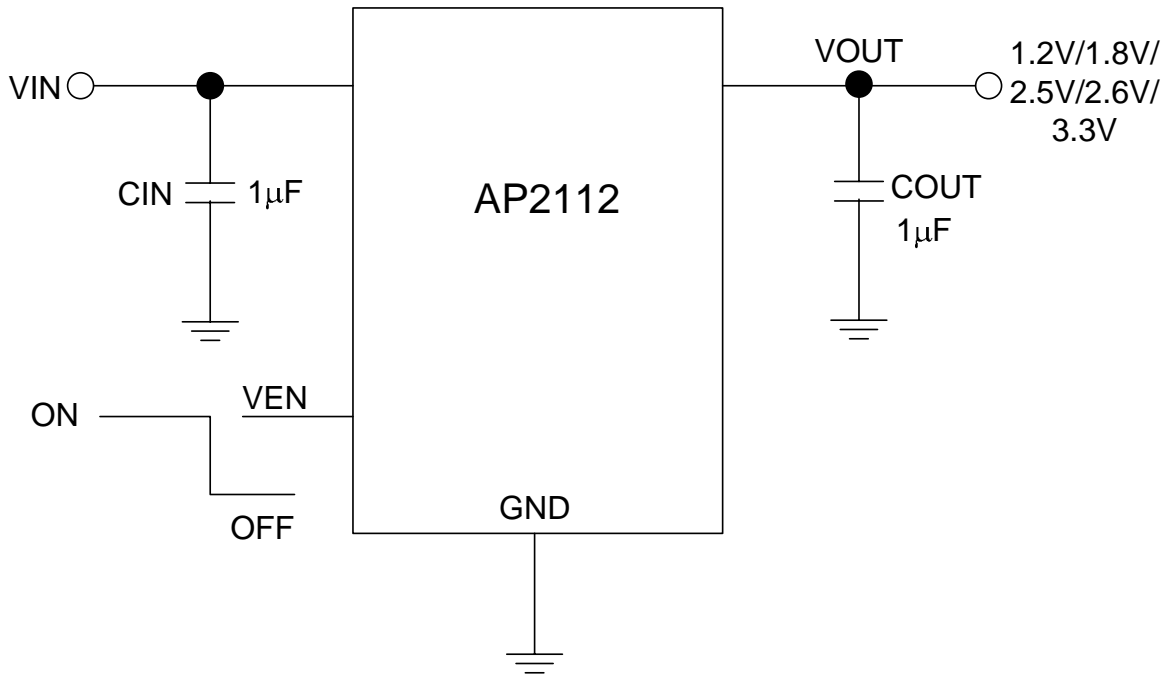


Figure 19. Enable Off

**Typical Application (Note 4)**


Note 4: It is recommended to use X7R or X5R dielectric capacitor if 1.0 $\mu$ F ceramic capacitor is selected as input/output capacitors.

Figure 20. AP2112 Typical Application

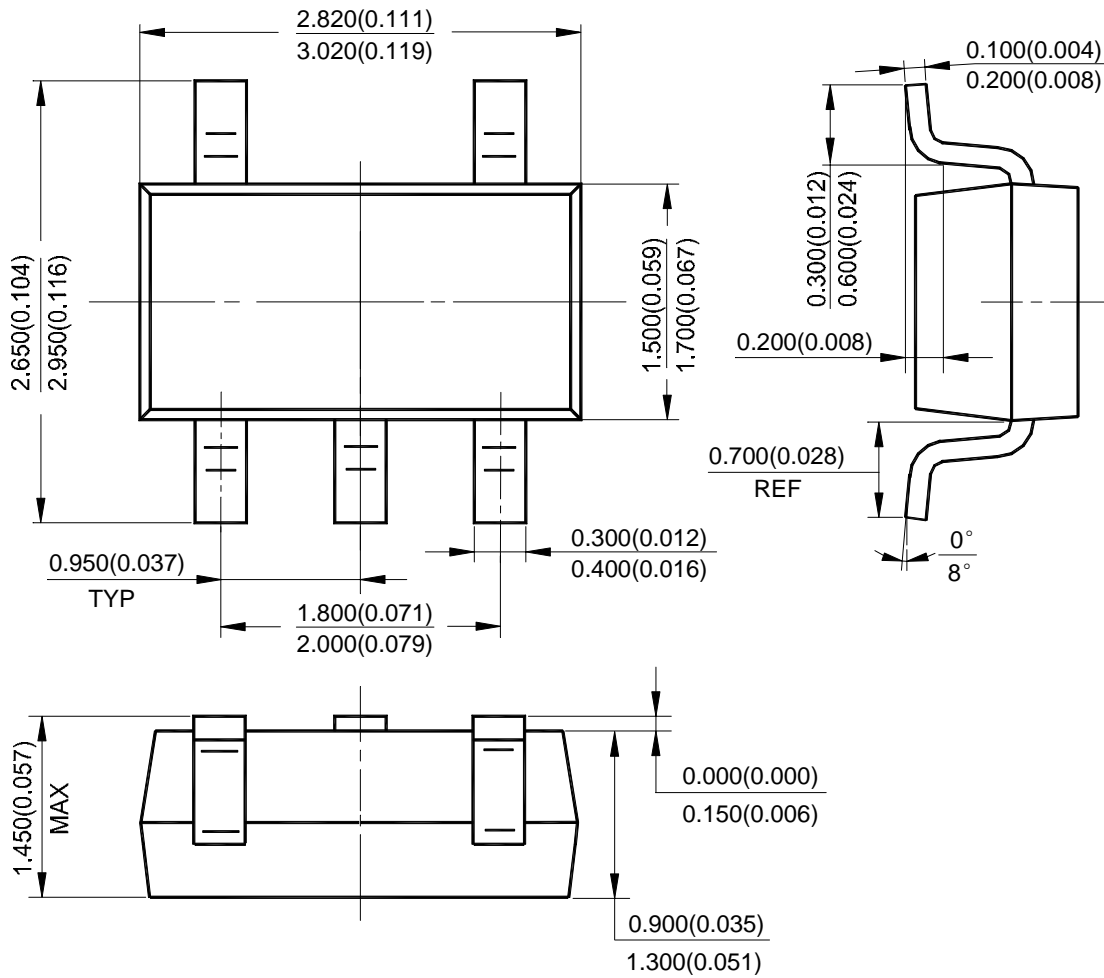
**600mA CMOS LDO REGULATOR WITH ENABLE**

**AP2112**

**Mechanical Dimensions**

**SOT-23-5**

**Unit: mm(inch)**

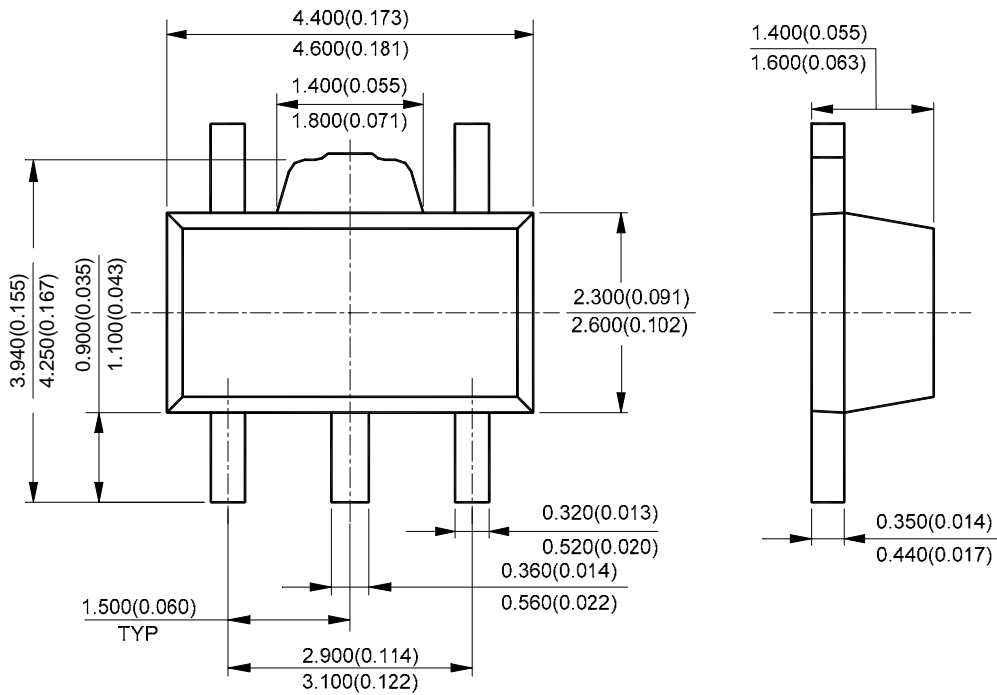




**Mechanical Dimensions (Continued)**

**SOT-89-5**

**Unit: mm(inch)**







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