ANALOG DEVICES

Ultralow Offset Voltage Op Amp

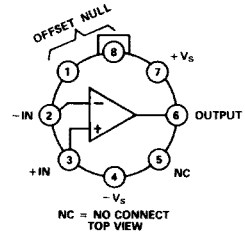
AD OP-07

FEATURES

Ultralow Offset Voltage: 10μV
Ultralow Offset Voltage Drift: 0.2μV/°C
Ultrastable vs. Time: 0.2μV/°C
Ultralow Noise: 0.35μV p–p
No External Components Required
Monolithic Construction
High Common-Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A Sockets
Military Parts and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip, TO-99 Hermetic Metal Can, or SOIC
Available in Wafer-Trimmed Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
Surface Mount (SOIC)

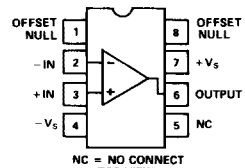
CONNECTION DIAGRAMS

TO-99 (H) Package



NC = NO CONNECT
TOP VIEW

Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



NC = NO CONNECT
TOP VIEW

PRODUCT DESCRIPTION

A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed-loop gain applications. Typical input offset voltages as low as 10μV, typical bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C (typ) and long-term stability of 0.2μV/month (typ) eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common-mode input voltage range (±13V min) common-mode rejection ratio (typically up to 126dB) and high differential input impedance (50MΩ typ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the commercial grades are also available in plastic 8-pin mini-DIP and plastic surface mount (SOIC) packages.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultralow offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultralow input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common-mode input voltage range and high common-mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

AD OP-07—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, unless otherwise specified)

Model		AD OP-07E			AD OP-07C			AD OP-07D		
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
OPEN LOOP GAIN	A_{VO}	**2,000**	5,000		**1,200**	4,000		**1,200**	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	**±12.5**	±13.0		**±12.0**	±13.0		**±12.0**	±13.0	
		±12.0	±12.8		**±11.5**	±12.8		**±11.5**	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**75**		60	**150**		60	**150**
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift										
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	**3.8**		0.8	**6.0**		0.8	**6.0**
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8	35		12	50		12	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	**±4.0**		±1.8	**±7.0**		±2.0	**±12**
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13	35		18	50		18	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{INCM}		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±13.0**	±14.0		**±13.0**	±14.0		**±13.0**	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common-Mode Rejection Ratio	CMRR	**106**	123		**100**	120		**94**	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	**4.0**		3.5	**5.0**		3.5	**5.0**
Power Consumption	P_D		90	**120**		105	**150**		105	**150**
			6.0	**9.0**		6.0	**9.0**		6.0	**9.0**
Rejection Ratio	PSRR	**94**	107		**90**	104		**90**	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, the AD OP-07A offset voltage is guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested: 90% of units meet this specification.

Specifications subject to change without notice.

AD OP-07A			AD OP-07			Test Conditions	Units
Min	Typ	Max	Min	Typ	Max		
3,000	5,000		**2,000**	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		**1,500**	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L = 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		**±12.5**	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		**±12.0**	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		**±10.5**	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		**±12.0**	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	**25**		30	**75**	Note 1	μV
	25	**60**[1]		60	**200**[1]	T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	**0.6**		0.3	**1.3**	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 2	μV/Month
	0.3	**2.0**		0.4	**2.8**		nA
	0.8	**4.0**		1.2	**5.6**	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	**±2.0**		±1.0	**±3.0**		nA
	±1.0	**±4.0**		±2.0	**±6.0**	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz	μV p-p
	10.3	18.0		10.3	18.0	$f_O = 10Hz$	nV/√Hz
	10.0	13.0		10.0	13.0	$f_O = 100Hz$	nV/√Hz
	9.6	11.0		9.6	11.0	$f_O = 1kHz$	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz	pA p-p
	0.32	0.80		0.32	0.80	$f_O = 10Hz$	pA/√Hz
	0.14	0.23		0.14	0.23	$f_O = 100Hz$	pA/√Hz
	0.12	0.17		0.12	0.17	$f_O = 1kHz$	pA/√Hz
±13.0	±14.0		**±13.0**	±14.0			V
±13.0	±13.5		**±13.0**	±13.5		T_{min} to T_{max}	V
110	126		**110**	126		$V_{CM} = \pm CMVR$	dB
106	123		**106**	123		$V_{CM} = \pm CMVR$, T_{min} to T_{max}	dB
	3.0	**4.0**		30	**4.0**	$V_S = \pm 15V$	mA
	90	**120**		90	**120**	$V_S = \pm 15V$	mW
	6.0	**8.4**		6.0	**8.4**	$V_S = \pm 3V$	mW
100	110		**100**	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		**94**	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
−55		+125	−55		+125		°C

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AD OP-07

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AD OP-07A, AD OP-07	−55°C to +125°C
AD OP-07E, AD OP-07C, AD OP-07D	0 to +70°C
Lead Temperature Range (Soldering 60sec)	+300°C

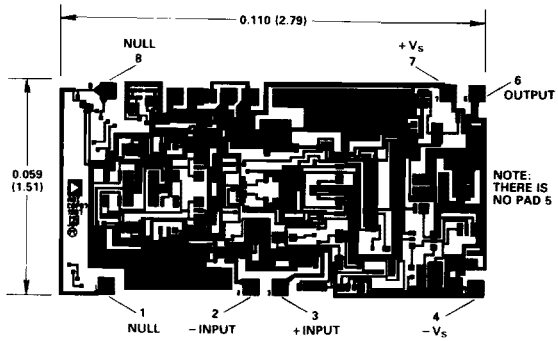
NOTE

Note 1: Maximum package power dissipation vs. ambient temperature.

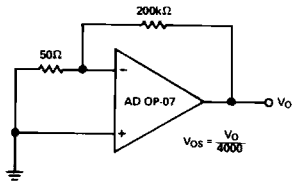
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99(H)	80°C	7.1mW/°C
Mini-DIP(N)	36°C	5.6mW/°C
Cerdip(Q)	75°C	6.7mW/°C

CHIP DIMENSIONS AND BONDING DIAGRAM

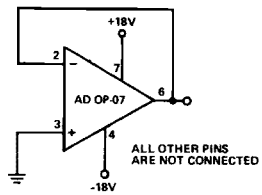
Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



THE AD OP-07 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM FOR PRECISION HYBRIDS. CONSULT THE FACTORY FOR DETAILS.



Offset Voltage Test Circuit



Burn-In Circuit

ORDERING GUIDE[1]

Model	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)	Package Description	Package Option[2]
ADOP-07EH	0 to +70	75	1.3	TO-99	H-08A
ADOP-07EN	0 to +70	75	1.3	Mini-DIP	N-8
ADOP-07EQ	0 to +70	75	1.3	Cerdip	Q-8
ADOP-07CH	0 to +70	150	1.8	TO-99	H-08A
ADOP-07CN	0 to +70	150	1.8	Mini-DIP	N-8
ADOP-07CQ	0 to +70	150	1.8	Cerdip	Q-8
ADOP-07CR	0 to +70	150	1.8	SOIC	R-8
ADOP-07CR-REEL	0 to +70	150	1.8	SOIC	
ADOP-07DH	0 to +70	150	2.5	TO-99	H-08A
ADOP-07DN	0 to +70	150	2.5	Mini-DIP	N-8
ADOP-07DQ	0 to +70	150	2.5	Cerdip	Q-8
ADOP-07AH	−55 to +125	25	0.6	TO-99	H-08A
ADOP-07AQ	−55 to +125	25	0.6	Cerdip	Q-8
ADOP-07H	−55 to +125	75	1.3	TO-99	H-08A
ADOP-07Q	−55 to +125	75	1.3	Cerdip	Q-8

NOTES

[1]A, C and D grade chips are also available.

[2]For outline information see Package Information section.

The AD OP-07 may be directly substituted for other OP-07s as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

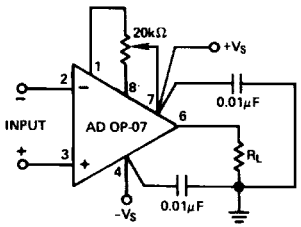


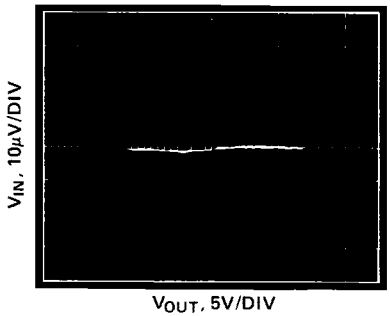
Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

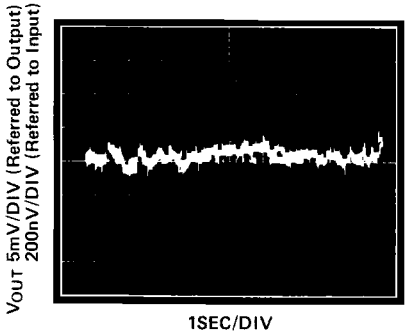
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to Pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

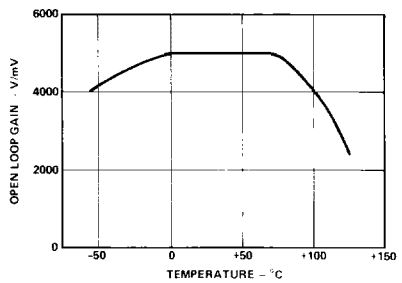
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



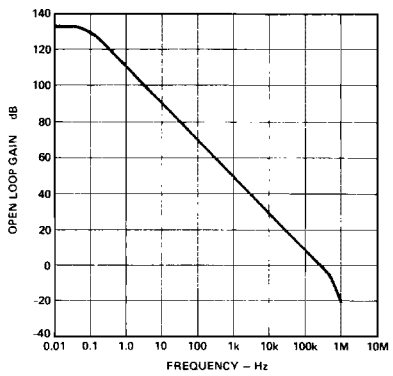
AD OP-07 Open-Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

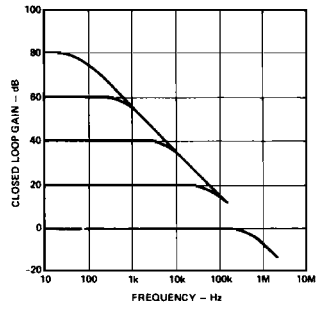


Open-Loop Gain vs. Temperature

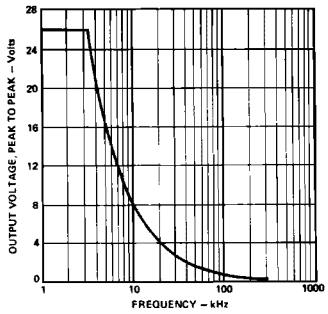


Open-Loop Frequency Response

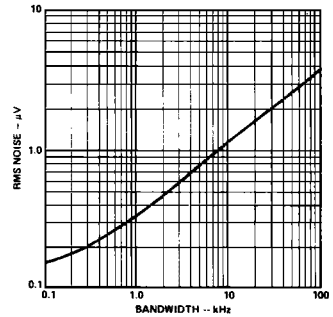
AD OP-07—Typical Performance Curves



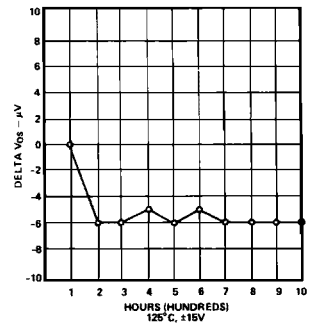
Closed-Loop Response for Various Gain Configurations



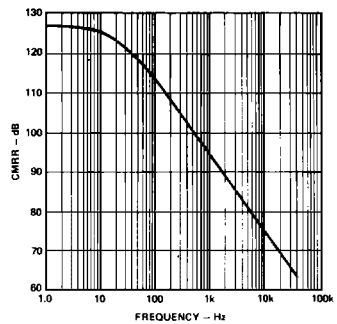
Maximum Undistorted Output vs. Frequency



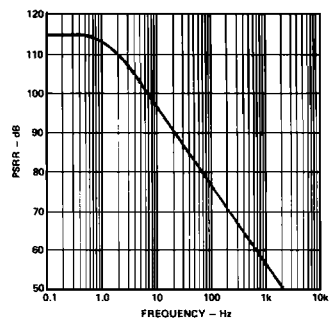
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



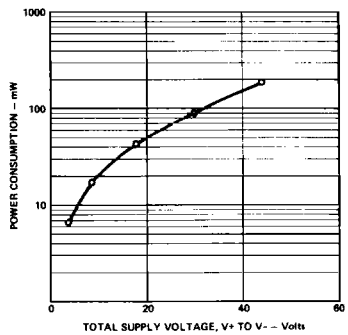
Offset Voltage vs. Time



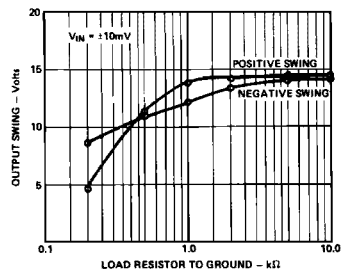
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance