1. APPLICATION

This specification manual applies to the conforming product specifications of the 68-pin, two-piece OTP-ROM card of the JEIDA version 4.1 and PCMCIA version 2.0 associations.

2. FUNDAMENTAL CIRCUITS

2.1 MEMORY CAPACITY

ITEM	MEMORY CAPACITY	MEMORY CONFIGURATION
4-OP-256	256 KByte (256KW x 8bit or 128KW x 16bit)	1 Mbit OTP-ROM x 2
4-OP-512	512 KByte (512KW x 8bit or 256KW x 16bit)	2 Mbit OTP-ROM x 2
4-OP-1M	1 MByte (1MW x 8bit or 512KW x 16bit)	2 Mbit OTP-ROM x 4
4-OP-2M	2 MByte (2MW x 8bit or 1MW x 16bit)	2 Mbit OTP-ROM x 8
4-OP-4M	4 MByte (4MW x 8bit or 2MW x 16bit)	2 Mbit OTP-ROM x 16

3. CIRCUIT CONFIGURATION AND LOGIC

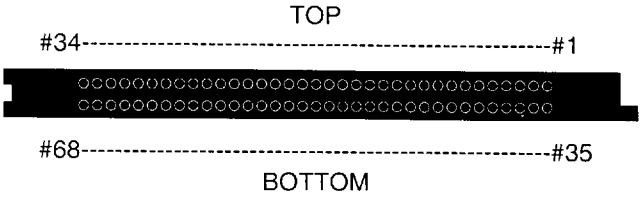
3.1 PIN ARRANGEMENT

PIN #	SYMBOL	PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG
1	GND	11	A9	21	A12	31	D1	41	D15	51	Vcc	61	*REG
2	D3	12	A8	22	A7	32	D2	42	*CSH	52	VPP2	62	*BVD2
3	D4	13	A13	23	A6	33	WP	43	NC	53	NC	63	*BVD1
4	D5	14	A14	24	A5	34	GND	44	NC	54	NC	64	D8
5	D6	15	*PGM	25	A4	35	GND	45	NC	55	NC	65	D9
6	D7	16	NC	26	A3	36	*CD1	46	A17	56	NC	66	D10
7	*CSL	17	Vcc	27	A2	37	D11	47	A18	57	NC	67	*CD2
8	A10	18	VPP1	28	A1	38	D12	48	A19	58	RESET	68	GND
9	*OE	19	A16	29	A0	39	D13	49	A20	59	*WAIT		
10	A11	20	A15	30	D0	40	D14	50	NC	60	NC		

NOTES:

1. PIN 48 (A19) and PIN 49 (A20) are made NC on the 4-OP-256-2 256 KB card.
2. PIN 48 (A19) and PIN 49 (A20) are made NC on the 4-OP-512-2 512 KB card.
3. PIN 49 (A20) is made NC on the 4-OP-1M-2 1 Mbyte card.

3.2 PIN DIAGRAM



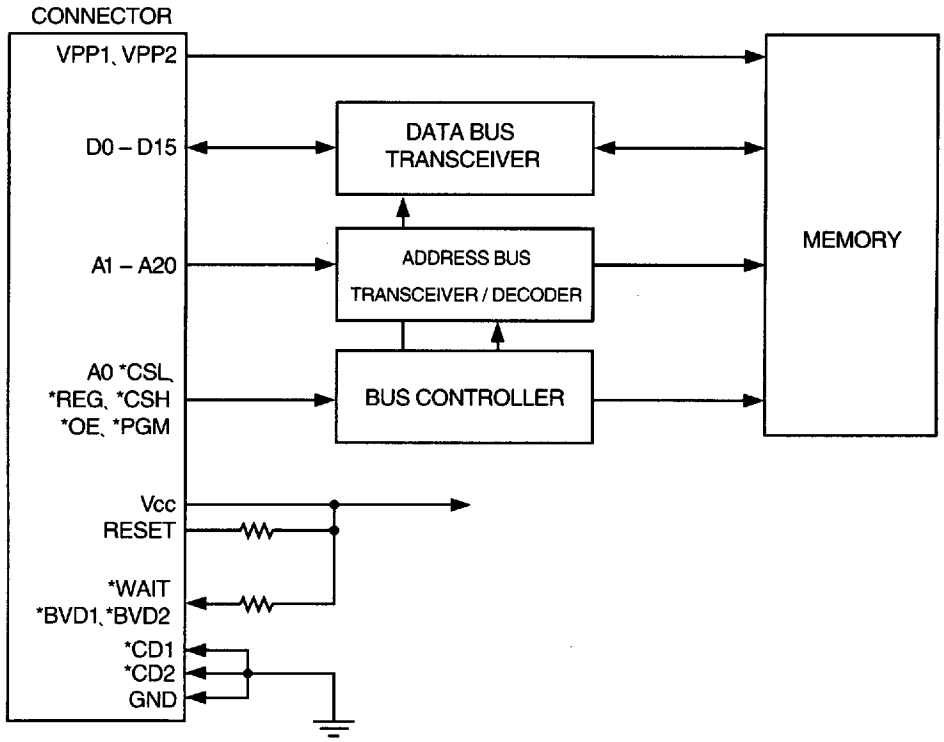
NOTE:

This PIN arrangement conforms with the standards set by the JEIDA version 4.1 and PCMCIA version 2.0 standards.

3.3 PIN DESCRIPTION

PIN #	DESCRIPTION
A0 – A20	ADDRESS INPUT
D0 – D15	DATA INPUT/ OUTPUT
*CSL, *CSH	CHIP SELECT
*OE	OUTPUT ENABLE
*PGM	PROGRAM INPUT/ OUTPUT ENABLE
VPP1, VPP2	PROGRAM SUPPLY VOLTAGE
*CD1, *CD2	CONTACT DETECTION
*BVD1, *BVD2	BATTERY VOLTAGE DETECT OUTPUT
WP	WRITE * PROGRAM
*REG	ATTRIBUTE MEMORY SELECT
RESET	RESET
*WAIT	WAIT
Vcc	POWER
GND	GROUND
NC	NO CONNECTION

3.4 BLOCK DIAGRAM



NOTES:

1. RESET = 100kΩ pull-up
2. *BVD1, *BVD2, *WAIT = 100kΩ pull-up

3.5 FUNCTION

*CSH	*CSL	A0	*OE	*PGM	VPP1	VPP2	VCC	MODE	D8 – D15	C0 – D7
H	H	X	X	X	5V	5V	5V	NON-SELECT	HIGH – Z	HIGH – Z
H	L	L	L	H	5V	5V	5V	READ(x8)	HIGH – Z	DATA OUTPUT (EVEN)
H	L	H	L	H	5V	5V	5V	READ(x8)	HIGH – Z	DATA OUTPUT (ODD)
L	H	X	L	H	5V	5V	5V	READ(x8)	DATA OUTPUT (ODD)	HIGH – Z
L	L	X	L	H	5V	5V	5V	READ(x16)	DATA OUTPUT (ODD)	DATA OUTPUT (EVEN)
X	X	X	H	H	5V	5V	5V	OUTPUT DISABLE	HIGH – Z	HIGH – Z
H	L	L	H	L	12.5V	6V	6V	PROGRAM(x8)	HIGH – Z	DATA INPUT (EVEN)
H	L	L	L	H	12.5V	6V	6V	VERIFY(x8)	HIGH – Z	DATA OUTPUT (EVEN)
H	L	H	H	L	6V	12.5V	6V	PROGRAM(x8)	HIGH – Z	DATA INPUT (ODD)
H	L	H	L	H	6V	12.5V	6V	VERIFY(x8)	HIGH – Z	DATA OUTPUT (ODD)
L	H	X	H	L	6V	12.5V	6V	PROGRAM(x8)	DATA INPUT (ODD)	HIGH – Z
L	H	X	L	H	6V	12.5V	6V	VERIFY(x8)	DATA OUTPUT (ODD)	HIGH – Z
L	L	X	H	L	12.5V	12.5V	6V	PROGRAM(x16)	DATA INPUT (ODD)	DATA INPUT (ODD)
L	L	X	L	H	12.5V	12.5V	6V	VERIFY(x16)	DATA OUTPUT (ODD)	DATA OUTPUT (ODD)

*REG = VIH

4. ABSOLUTE MAXIMUM RATINGS

DURING READ/ PROGRAM

DESCRIPTION	SIGNAL	RATING	UNIT
SUPPLY VOLTAGE	Vcc	-0.5 – +6.5	V
INPUT VOLTAGE	Vin	-0.5 – Vcc+0.5	V
OUTPUT VOLTAGE	Vout	-0.5 – Vcc+0.5	V
PROGRAM VOLTAGE	VPP1/2	-0.5 – +13.5	V
OPERATION TEMPERATURE	Topr	-10 – +60	°C
STORAGE TEMPERATURE	Tstg	-30 – +70	°C

*Voltage when the GND terminal has been standardized.

5. RECOMMENDED OPERATING CONDITIONS

SIGNAL	DESCRIPTION		RATING		UNIT
			MIN	MAX	
Vcc	POWER SUPPLY VOLTAGE	READ	4.75	5.25	V
		PROGRAM	5.75	6.25	
VPP	PROGRAM VOLTAGE	READ	4.75	5.25	V
		PROGRAM	12.2	12.8	
VIH	INPUT VOLTAGE "H" LEVEL		2.4		V
VIL	INPUT VOLTAGE "L" LEVEL			0.8	V
TOPR	OPERATION TEMPERATURE		0.0	+55	°C

6. ELECTRICAL CHARACTERISTICS

6.1 DC CHARACTERISTICS

DURING READ/ PROGRAM

SIGNAL	DESCRIPTION	RATING		UNIT	NOTES
		MIN	MAX		
ILI	INPUT LEAK CURRENT	-10	10	µA	1
		-25	10	µA	2
ILO	OUTPUT LEAK CURRENT	-10	10	µA	3
ISB1	STANDBY SUPPLY CURRENT		2	mA	4
ISB2			20	mA	5
ICC1	OPERATION SUPPLY CURRENT		65	mA	6
ICC2	AVERAGE OPERATION SUPPLY CURRENT		65	mA	7
VIH	INPUT VOLTAGE "H" LEVEL	2.4		V	
VIL	INPUT VOLTAGE "L" LEVEL		0.8	V	
VOH	OUTPUT VOLTAGE "H" LEVEL	3.8		V	8
VOL	OUTPUT VOLTAGE "L" LEVEL		0.4	V	9

Voltage when the GND terminal is standardized.

NOTES:

1. VIN = 0 to Vcc (not including *CS, *OE, *REG).
2. VIN = 0 to Vcc.
3. VOUT = 0 to Vcc, *CSL = *CSH = VIH, *OE = VIH
4. *CSL = *CSH ≥ V_{CC} -0.2V.
5. *CSL = *CSH = VIH.
6. *CSL = *CSH = VIL, VIN = VIH as well as VIL, IOUT = 0mA
7. Cycle = Min, Duty = 100%, IOUT = 0mA.
8. IOH = -2.0mA.
9. IOL = 3.2mA.

6.2 AC CHARACTERISTICS

READ CYCLE

SIGNAL	DESCRIPTION	CONDITIONS	RATING		UNIT
			MIN	MAX	
$t_{c}(R)$	READ CYCLE TIME		200		ns
$t_{a(A)}$	ADDRESS ACCESS TIME	*CS = *OE = VIL		200	ns
$t_{a(CE)}$	*CE ACCESS TIME	*OE = VIL		200	ns
$t_{a(OE)}$	*OE ACCESS TIME	*CS = VIL		100	ns
t_{DF}	*OE OUTPUT FLOATING DELAY TIME	*CS = VIL		90	ns
t_{OH}	OUTPUT HOLD AFTER *CE, *OE ADDRESS		30		ns

NOTE:

1. Vcc has simultaneous lead in current and cut off as Vpp.

PROGRAMMING CYCLE

ITEM	DESCRIPTION	RATING		UNIT
		MIN	MAX	
t_{AS}	ADDRESS SETUP TIME	2		µs
t_{OES}	*OE SETUP TIME	2		µs
t_{DS}	DATA SETUP TIME	2		µs
t_{AH}	ADDRESS HOLD TIME	0		µs
t_{DFP}	*OE OUTPUT FLOATING DELAY TIME	0	200	ns
t_{VCS}	VCC SETUP TIME	2		µs
t_{VPS}	VPP SETUP TIME	2		µs
t_{PW}	*PG (INITIAL) PULSE WIDTH	0.19	0.21	ms
t_{OPW}	*PGM (OVER PROGRAM) PULSE WIDTH	0.19	5.25	ms
t_{CES}	*CE SETUP TIME	2		µs
t_{OE}	VALID DATA OUTPUT TIME		200	ns

NOTE:

1. Vcc = 6V ± 0.25V, TOPR = 25 ± 5°C, VPP = 12.5 ± 0.3V

6.3 TERMINAL CAPACITANCE

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
CIN	INPUT TERMINAL	f = 1MHz, T_{OPR}=25 °C		40	pF
COUT	OUTPUT TERMINAL	V I/ 0 = 0V		45	pF

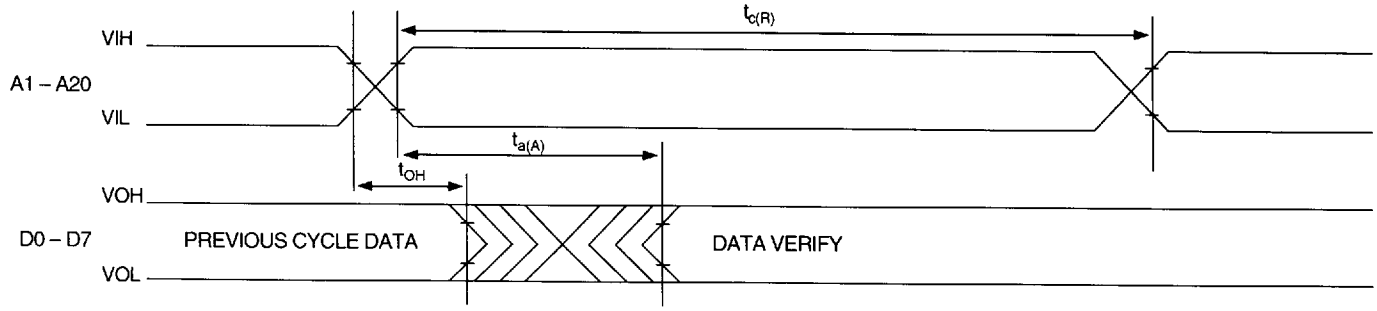
6.4 AC CHARACTERISTICS MEASUREMENT CONDITIONS

INPUT VOLTAGE	0.6V to 2.4V
INPUT PULSE LEADING EDGE/ TRAILING EDGE TIME	tR, tF = 5 to 10ns (0.8V to 2.2V)
TIMING MEASUREMENT VOLTAGE	Input VIH = 2.2V VIL = 0.8V
OUTPUT LOAD	ITTL gate + CL (100pF)

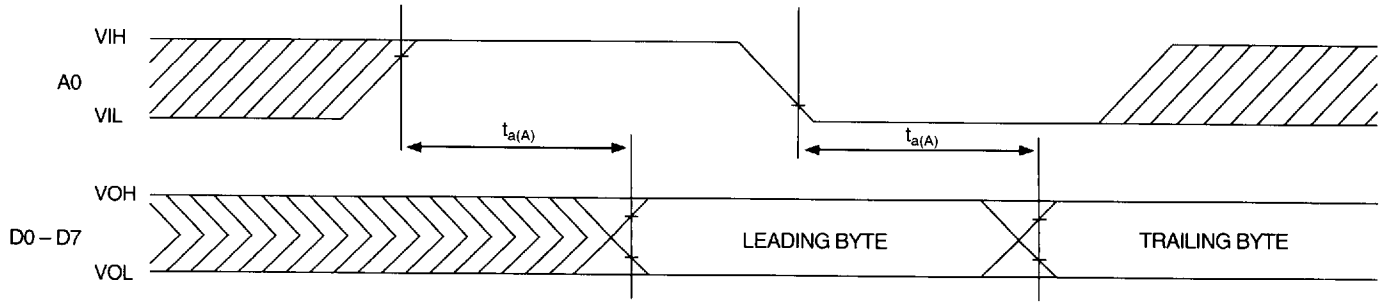
7. TIMING DIAGRAMS

7.1 READ CYCLES

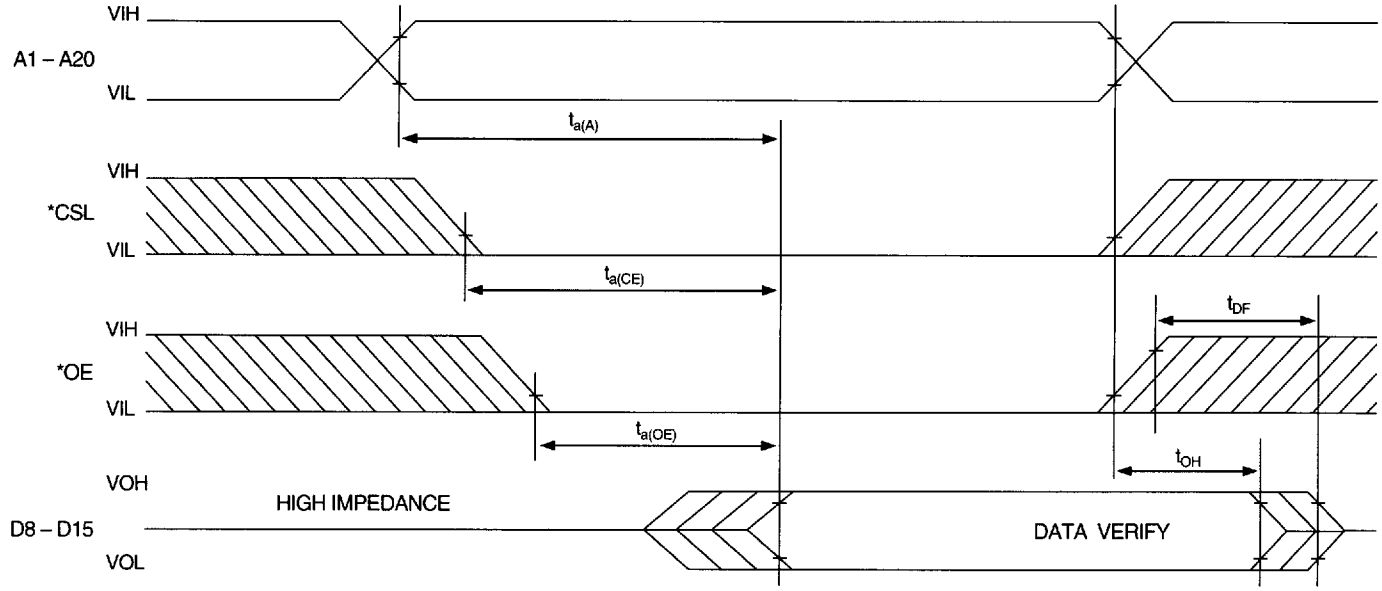
***CSH = VIH, *CSL = *OE = VIL: X 8 BIT**
***CSL = VIH, *CSH = *OE = VIL: X 8 BIT**
***CSL = *CSH = *OE = VIL: X 16 BIT**



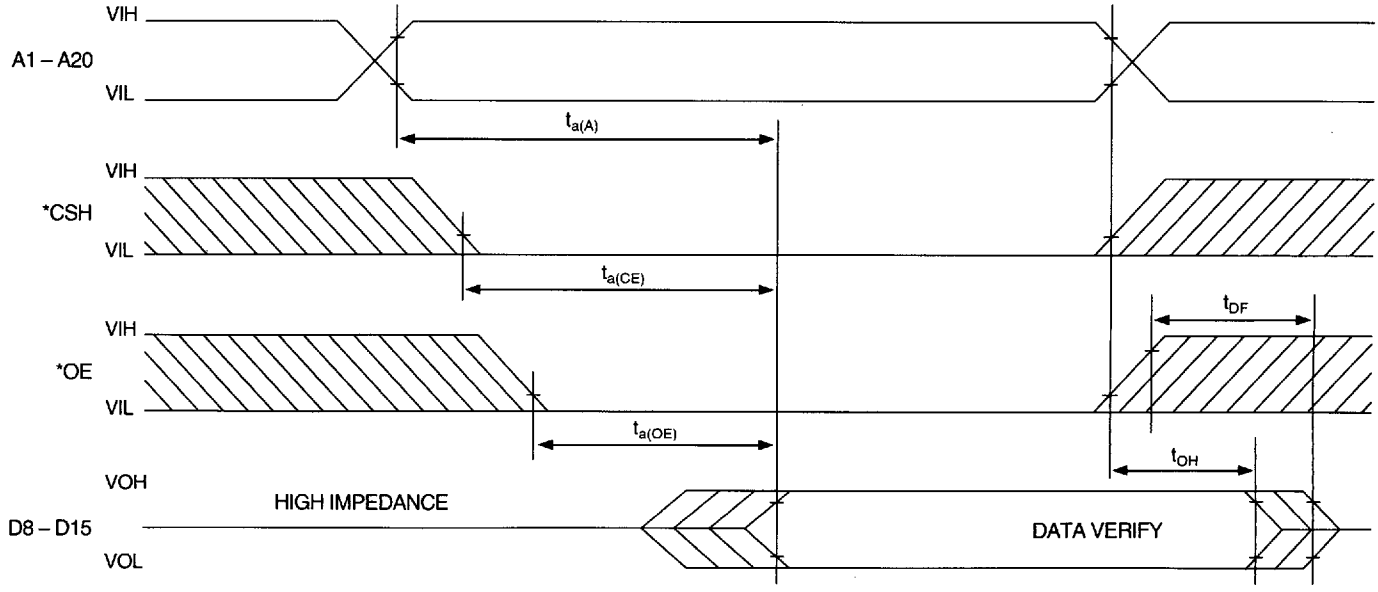
***CSH = VIH, *CSL = *OE = VIL: X 8 BIT**



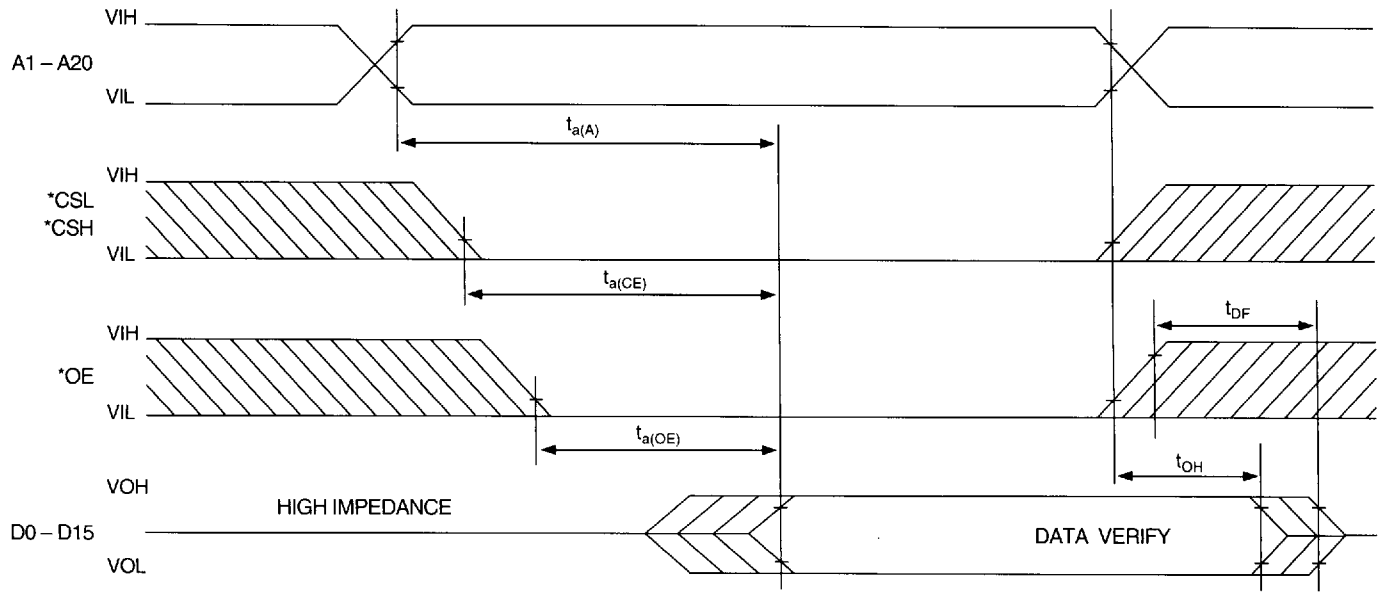
***CSH = VIH, A0 = VIL: X 8 BIT**



***CSL = VIH: X 8 BIT**

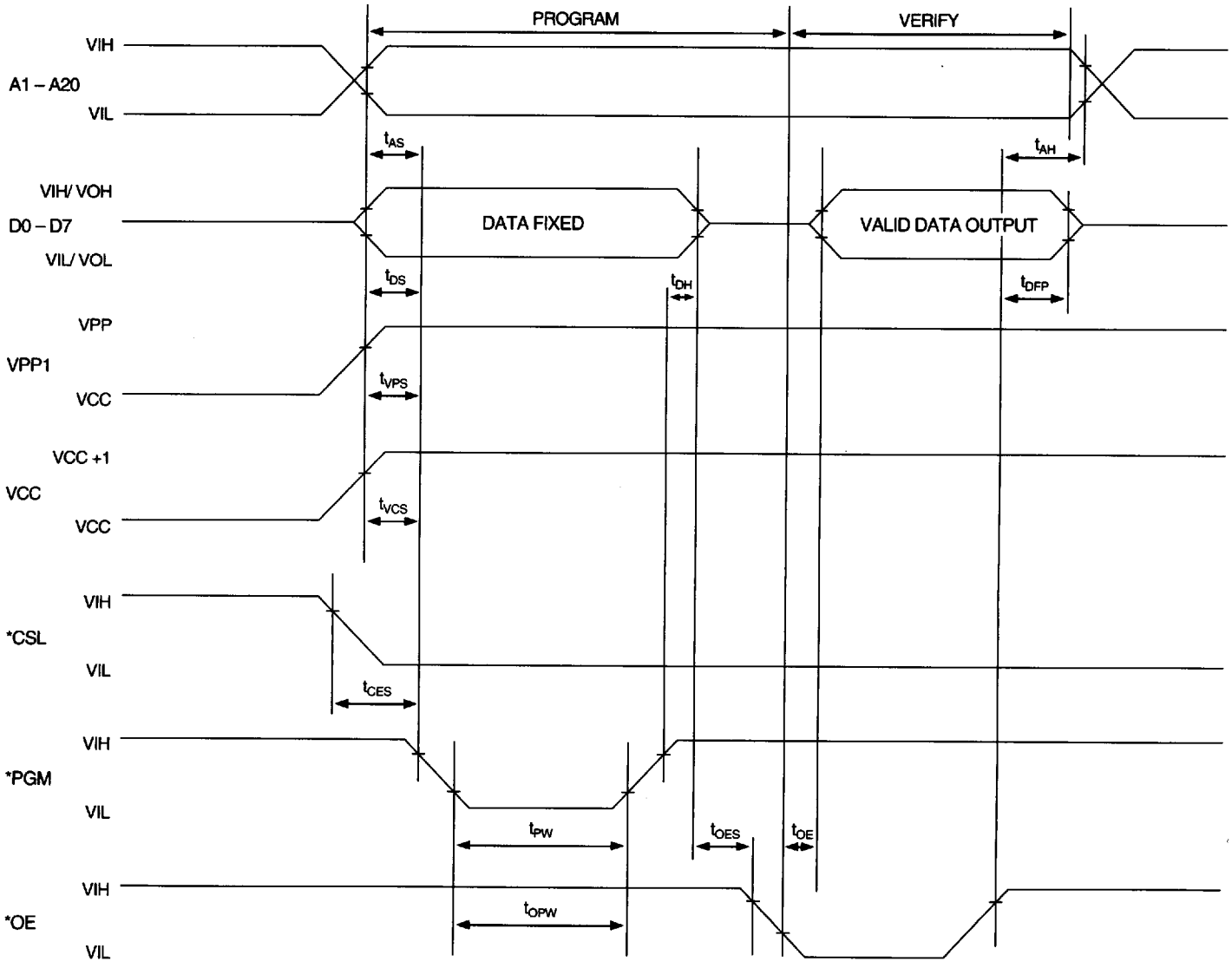


***CSL = *CSH = VIL: X 16 BIT**

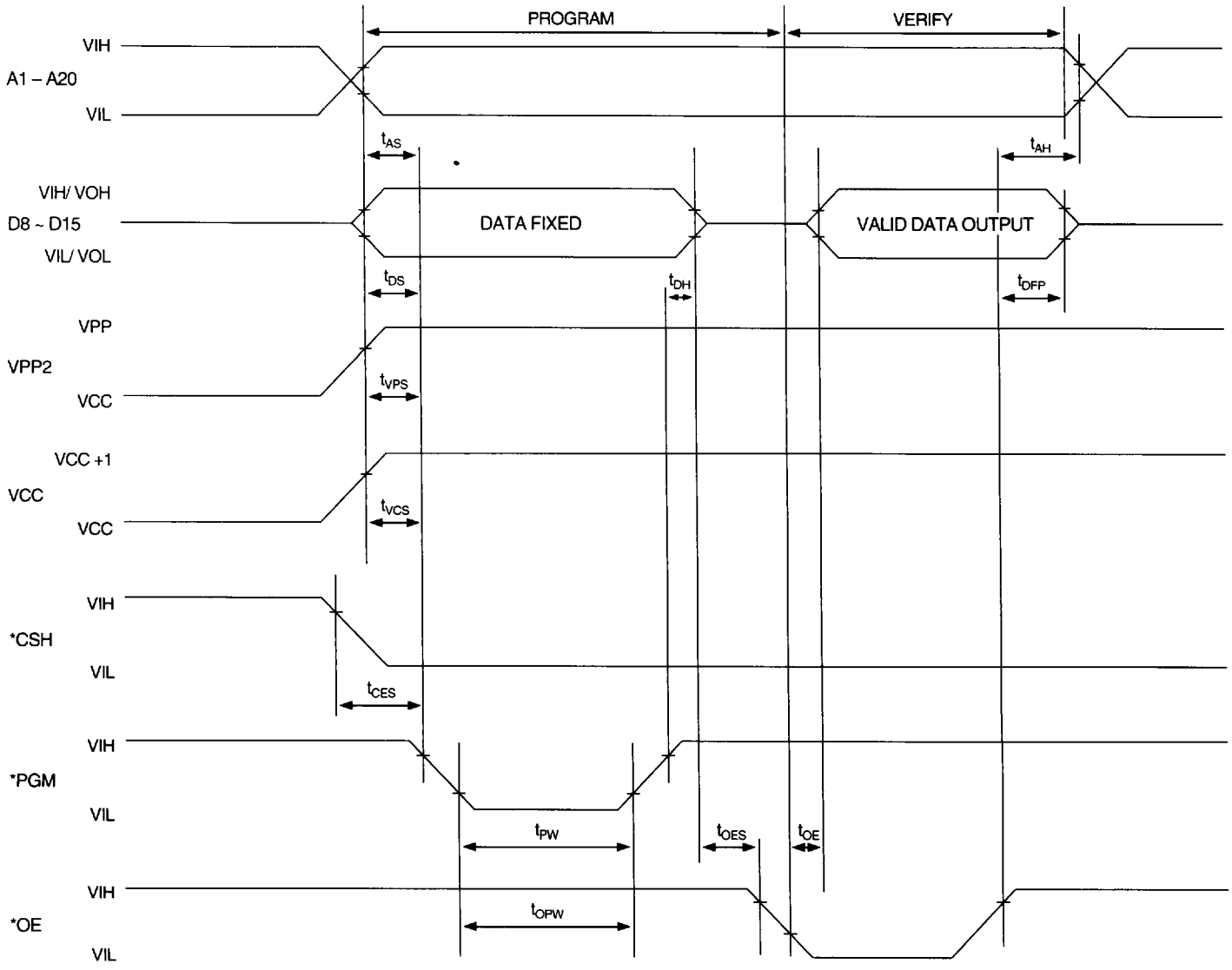


7.2 PROGRAMMING CYCLES

***CSH = VIH, A0 = VIL, VPP2 = VCC: X 8 BIT**

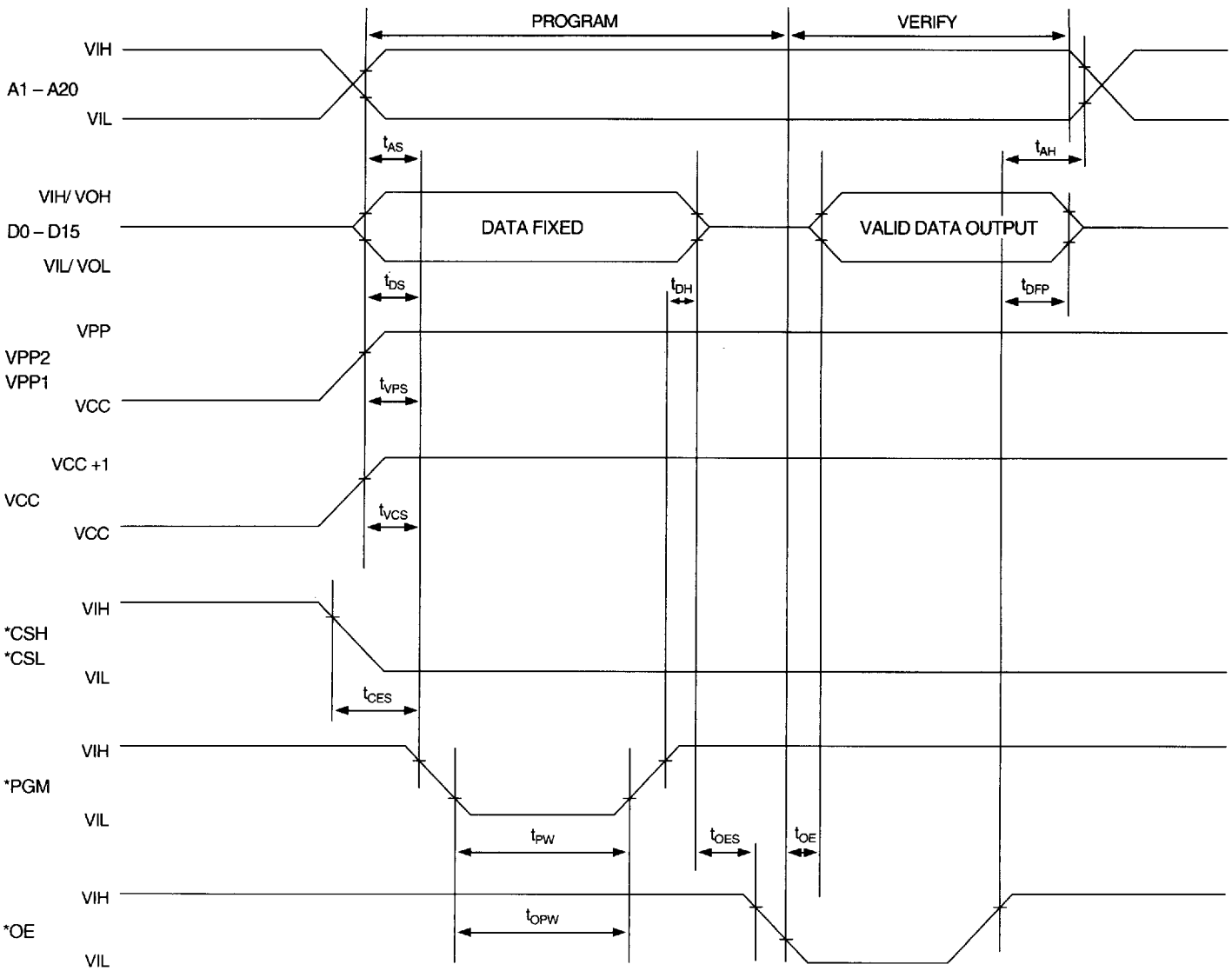


***CSL = VIH, VPP1 = VCC: X 8 BIT**



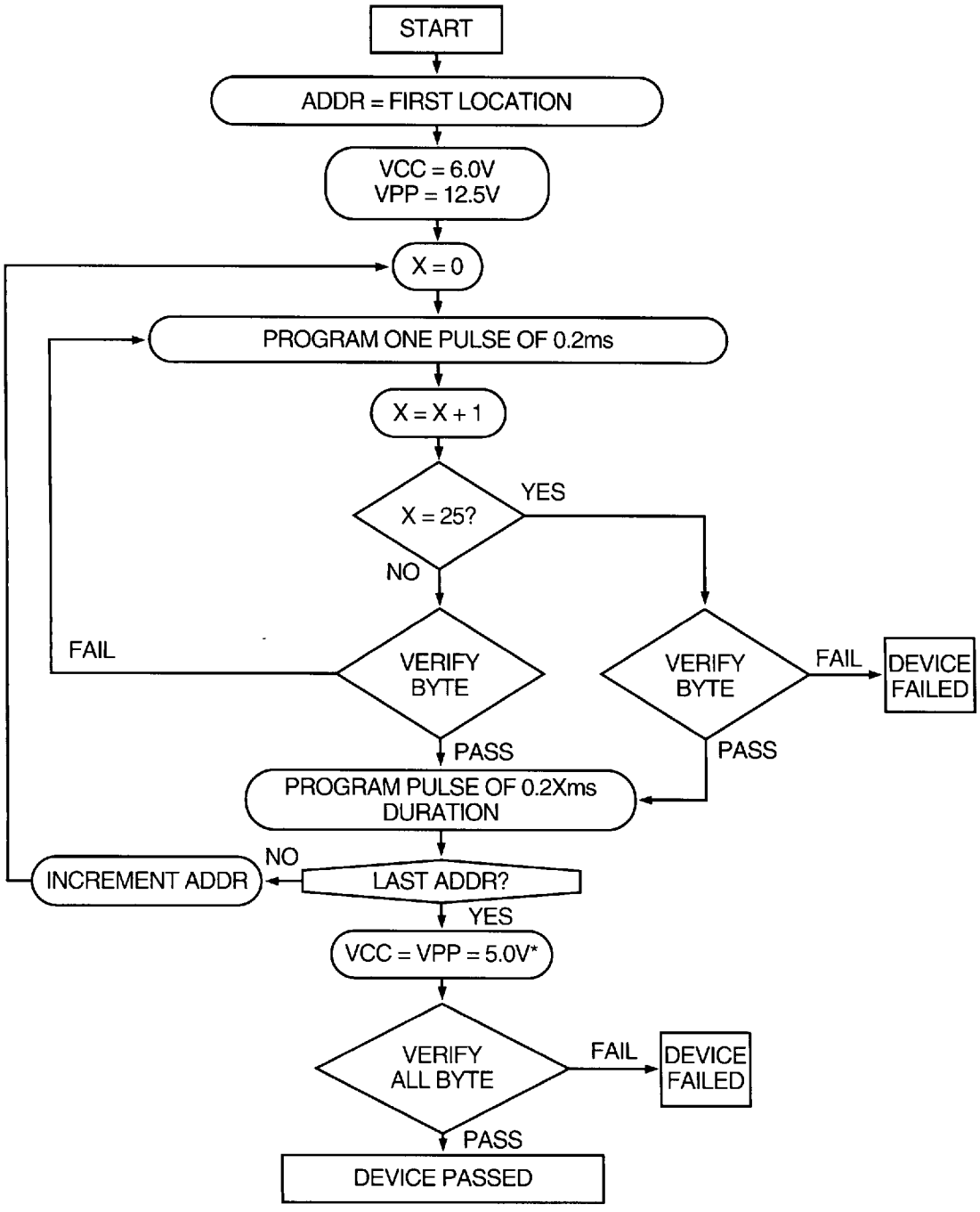
A0 = Either VIL or VIH

***VPP1 = VPP2 = 12.5V**
± 0.3V: X 16 BIT



A0 = Either VIL or VIH

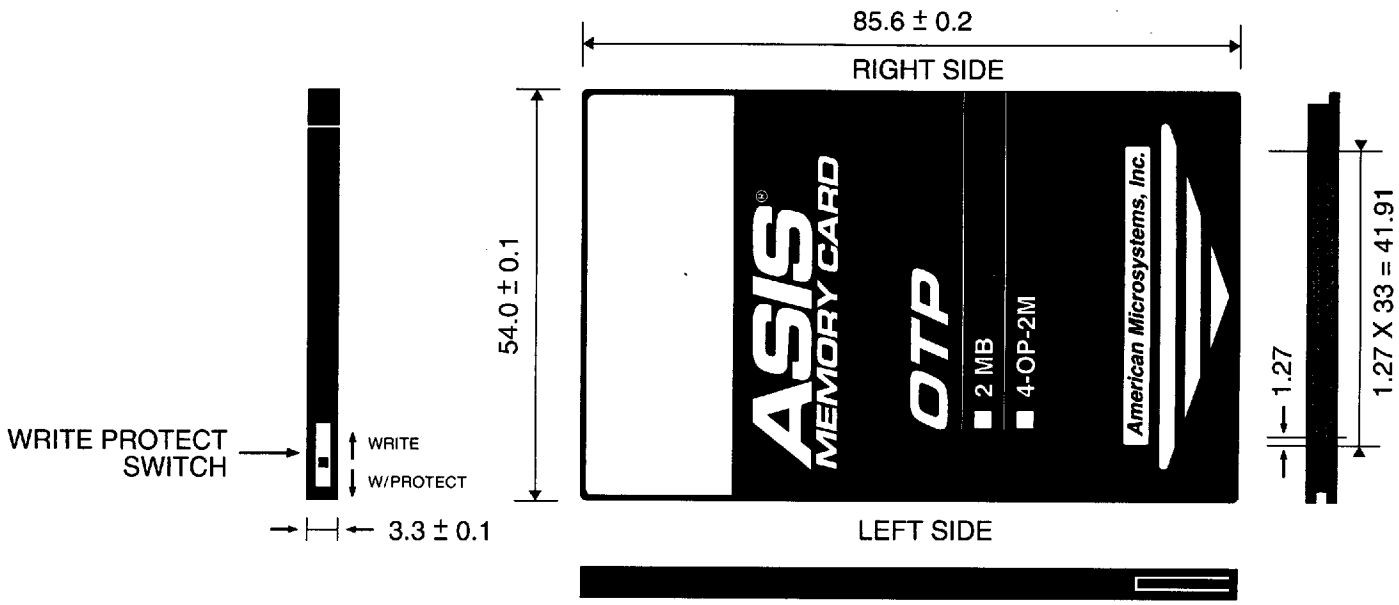
7.5 PROGRAMMING FLOW CHART



*4.75V ≤ VCC = VPP ≤ 5.25V

8. MECHANICAL CHARACTERISTICS

8.1 EXTERNAL DIMENSIONS



9. CARD INSPECTION

9.1 GENERAL INSPECTION

The following tests are performed on all cards before shipment.

ITEM	TESTING PARAMETERS	VOLTAGE	TEMPERATURE
HIGH TEMPERATURE OPERATION	MEMORY * READ TEST	5.25V/ 4.75V	+55 ± O.5°C

9.2 LOT GUARANTEE EXAMINATION

Five (5) cards are randomly selected from each lot and are tested once again under high and low temperature operating conditions as well as given an external examination after the general inspection (ref. Item 9.1).