USB2226

4th Generation USB 2.0 Flash Media Controller with Integrated Card Power FETs

PRODUCT FEATURES

Datasheet

- Complete System Solution for interfacing SmartMedia™ (SM) or xD Picture Card™ (xD), Memory Stick™ (MS), High Speed Memory Stick (HSMS), Memory Stick PRO (MSPRO), MS Duo™, Secure Digital (SD), Mini-Secure Digital (Mini-SD), TransFlash (SD), MultiMediaCard™ (MMC), Reduced Size MultiMediaCard (RS-MMC), NAND Flash, Compact Flash™ (CF) and CF Ultra™ I & II, and CF form-factor ATA hard drives to USB 2.0 bus
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
- Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
- Compliant with xD specifications for either Card Reader/Writer or Player mode applications
- On-Chip 4-Bit High Speed Memory Stick and MS PRO Hardware Circuitry
- On-Chip firmware reads and writes High Speed Memory Stick and MS PRO
- 1-bit ECC correction performed in hardware for maximum efficiency
- On-chip power FETs for supplying flash media card power with minimum board components
- USB Bus Power Certified
- 3.3 Volt I/O
- Complete USB Specification 2.0 Compatibility for Bus Powered Operation
  - Includes USB 2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- 8051 8 bit microprocessor
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal Program Memory
- On Board 24Mhz Crystal Driver Circuit
- Can be clocked by 48MHz external source
- On-Chip 1.8V Regulator for Low Power Core Operation
- Internal PLL for 480Mhz USB 2.0 Sampling, Configurable MCU clock
- Activity LED output
- Compatible with Microsoft WinXP, WinME, Win2K SP3, Apple OS10, Softconnex, and Linux Multi-LUN Mass Storage Class Drivers
- Win2K, Win98/98SE and Apple OS8.6 and OS9 Multi-LUN Mass Storage Class Drivers available from SMSC
- 128 Pin VTQFP Lead-free RoHS Compliant Package (1.0mm height, 14mm x14mm footprint)

ORDER NUMBERS:

USB2226-NU-XX FOR 128 PIN, VTQFP LEAD-FREE ROHS COMPLIANT PACKAGE

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Table of Contents

List of Tables

List of Figures

Chapter 1 General Description

The USB2226 is a USB 2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF and CF Ultra I/II) in True IDE Mode only, SmartMedia (SM) and XD cards, Memory Stick (MS), Memory Stick DUO (MSDUO) and Memory Stick Pro (MSPRO), Secure Digital (SD), and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.

The device consists of a USB 2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices. SM controller supports both SM and xD cards.

The USB2226 can read and write the following card formats:

- Secure Digital (SD), High Capacity SD (HC-SD), High Speed SD (HS-SD), Mini-SD, Micro-SD
- MultiMediaCard (MMC), MMCplus (HS-MMC), High Capacity MMC (HC-MMC), RS-MMC, MMCMobile
- Memory Stick (MS), MS Duo, Memory Stick PRO (MSPro), Memory Stick PRO-HG (Pro-HG)
- xD Picture Card, Type M, Type H
- SmartMedia (SM), TransFlash
- Compact Flash
- MicroDrive

Media activity LED output is also provided.

Internal power FETs are provided to directly supply power to the xD/SM, MMC/SD and MS/MSPro cards.

The internal ROM program implements a multi-LUN CF/SD/MMC/SM/MS reader function with individual card power control and activity indication. SMSC also provides licenses** for Win98 and Win2K drivers and setup utilities. Note: Please check with SMSC for precise features and capabilities for the current ROM code release.

Chapter 2 Acronyms

SM: SmartMedia

SMC: SmartMedia Controller

FM: Flash Media

FMC: Flash Media Controller

CF: Compact Flash

CFC: CompactFlash Controller

SD: Secure Digital

SDC: Secure Digital Controller

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

TPC: Transport Protocol Code.

ECC: Error Checking and Correcting

CRC: Cyclic Redundancy Checking

Chapter 3 Pin Configuration

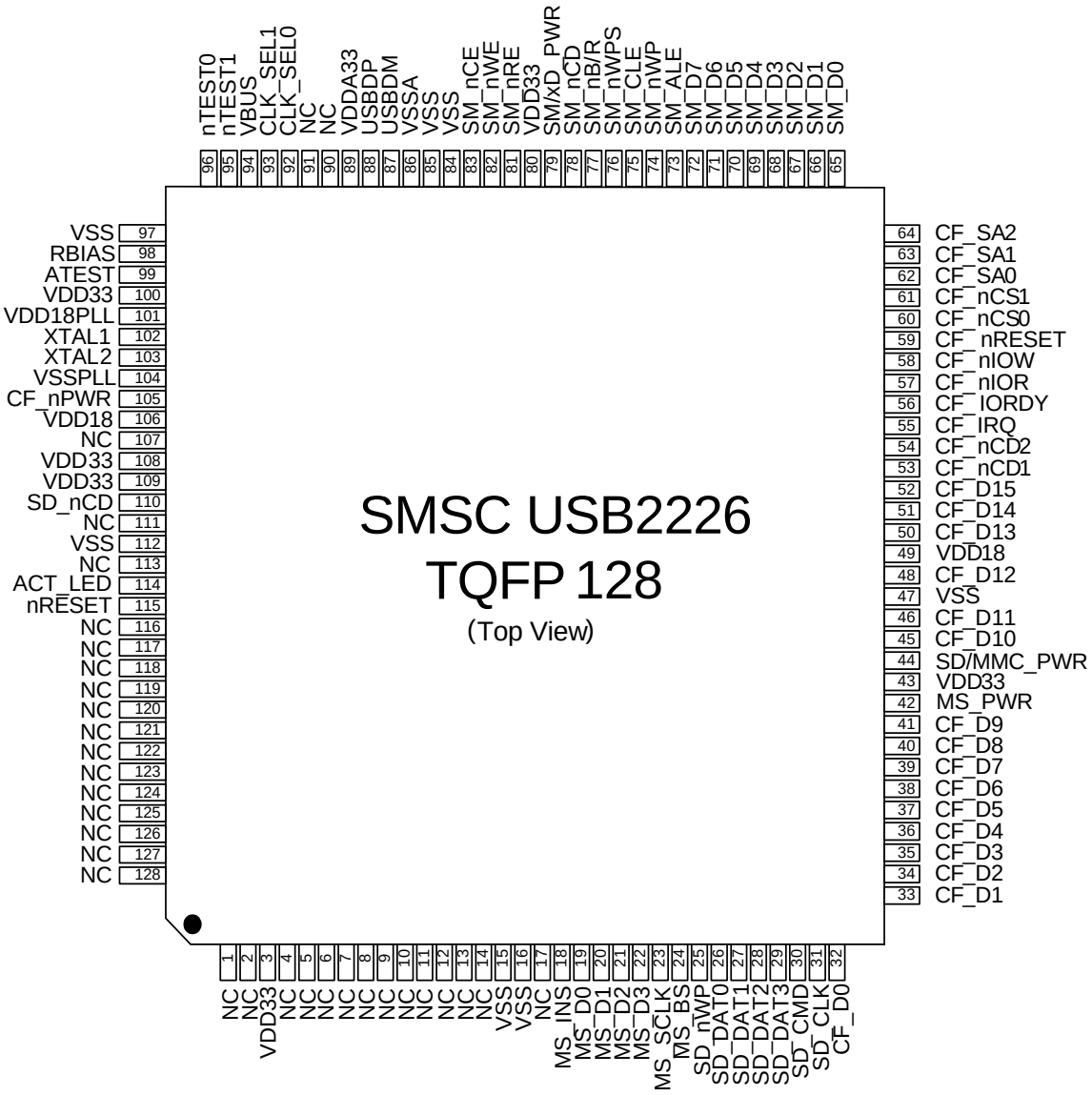

Figure 3.1 USB2226 128-Pin VTQFP

Chapter 4 Block Diagram

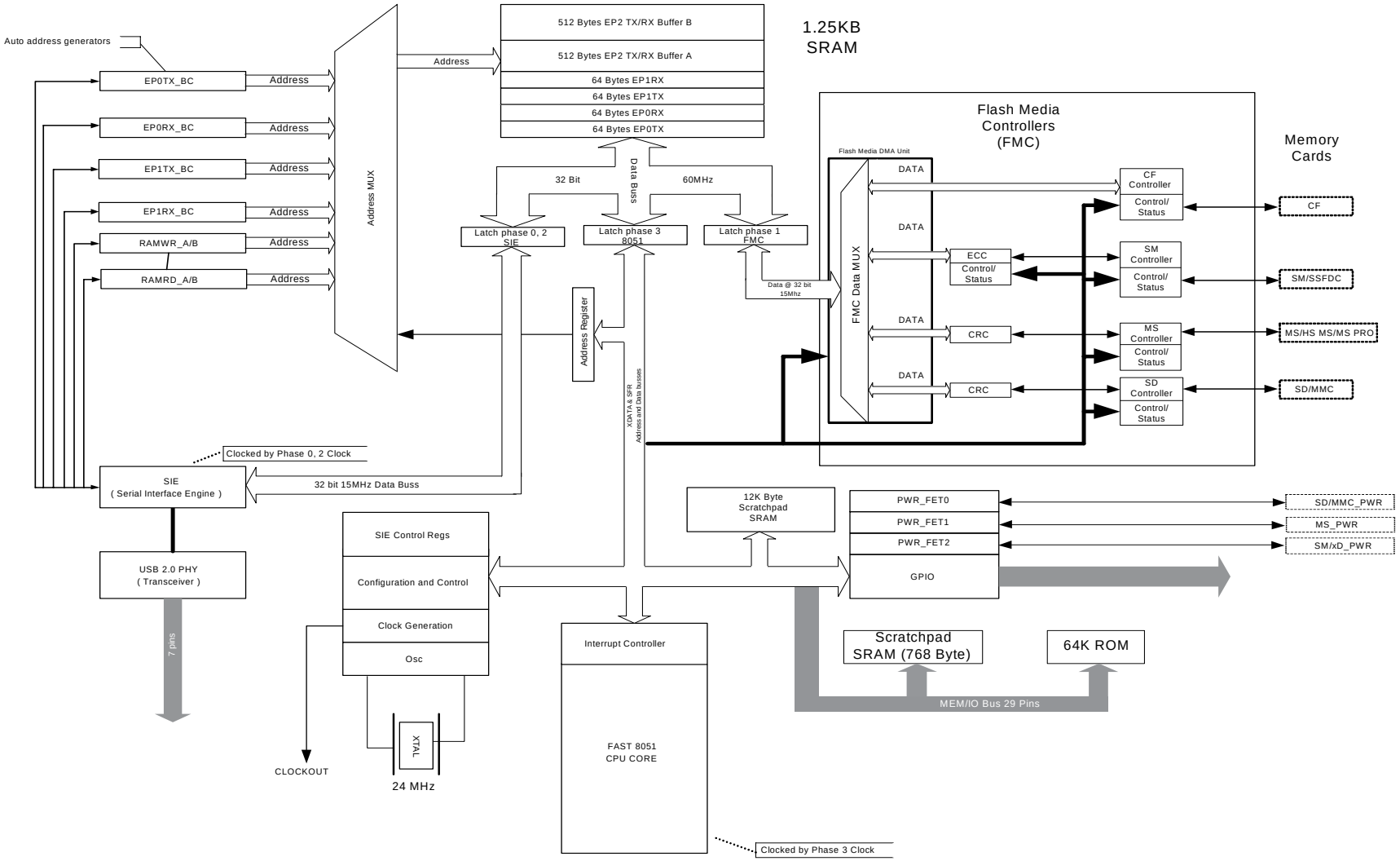

Figure 4.1 USB2226 Block Diagram

Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

5.1 PIN Descriptions

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
CompactFlash (In True IDE mode) INTERFACE			
CF_nCS1	61	O8PU	CF Chip Select 1: This pin is the active low chip select 1 signal for the CF ATA device.
CF_nCS0	60	O8PU	CF Chip Select 0: This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF_SA2	64	O8	CF Register Address 2: This pin is the register select address bit 2 for the CF ATA device.
CF_SA1	63	O8	CF Register Address 1: This pin is the register select address bit 1 for the CF ATA device.
CF_SA0	62	O8	CF Register Address 0: This pin is the register select address bit 0 for the CF ATA device.
CF_IRQ	55	IPD	CF Interrupt: This is the active high interrupt request signal from the CF device.
CF_D[15:8]	52 51 50 48 46 45 41 40	I/O8PD	CF Data 15-8: The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
CF_D[7:0]	39 38 37 36 35 34 33 32	I/O8PD	CF Data 7-0: The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
CF_IORDY	56	IPU	IO Ready: This pin is active high input signal. This pin has an internally controlled weak pull-up resistor.
CF_nCD2	54	IPU	CF Card Detection2: This card detection pin is connected to the ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF_nCD1	53	IPU	CF Card Detection1: This card detection pin is connected to ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF_nRESET	59	O8	CF Hardware Reset: This pin is an active low hardware reset signal to CF device.
CF_nIOR	57	O8	CF IO Read: This pin is an active low read strobe signal for CF device.
CF_nIOW	58	O8	CF IO Write Strobe: This pin is an active low write strobe signal for CF device.
SmartMedia INTERFACE			
SM_nWP	74	O8PD	SM Write Protect: This pin is an active low write protect signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_ALE	73	O8PD	SM Address Strobe: This pin is an active high Address Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_CLE	75	O8PD	SM Command Strobe: This pin is an active high Command Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
SM_D[7:0]	72 71 70 69 68 67 66 65	I/O8PD	SM Data 7-0: These pins are the bi-directional data signal SM_D7-SM_D0. The bi-directional data signal has an internal weak pull-down resistor.
SM_nRE	81	08PU	SM Read Enable: This pin is an active low read strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nWE	82	O8PU	SM Write Enable: This pin is an active low write strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nWPS	76	IPU	SM Write Protect Switch: A write-protect seal is detected, when this pin is low. This pin has an internally controlled weak pull-up resistor.
SM_nB/R	77	I	SM Busy or Data Ready: This pin is connected to the BSY/RDY pin of the SM device. An external pull-up resistor is required on this signal. The pull-up resistor must be pulled up to the same power source that powers the SM/NAND flash device.
SM_nCE	83	O8PU	SM Chip Enable: This pin is the active low chip enable signal to the SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nCD	78	IPU	SM Card Detection: This is the card detection signal from SM device to indicate if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MEMORY STICK INTERFACE			

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
MS_BS	24	O8	MS Bus State: This pin is connected to the BS pin of the MS device. It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS_SDIO/MS_D0	19	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. Most significant bit (MSB) of each byte is transmitted first by either MSC or MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS_D1	20	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. This pin has internally controlled weak pull-up and pull-down resistors for various operational modes.
MS_D[3:2]	22 21	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS_INS	18	IPU	MS Card Insertion: This pin is the card detection signal from the MS device to indicate, if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MS_SCLK	23	O8	MS System CLK: This pin is an output clock signal to the MS device. The clock frequency is software configurable.
SD INTERFACE			
SD_DAT[3:0]	29 28 27 26	I/O8PU	SD Data 3-0: These are bi-directional data signals. These pins have internally controlled weak pull-up resistors.
SD_CLK	31	O8	SD Clock: This is an output clock signal to SD/MMC device. The clock frequency is software configurable.
SD_CMD	30	I/O8PU	SD Command: This is a bi-directional signal that connects to the CMD signal of SD/MMC device. This pin has an internally controlled weak pull-up resistor.
SD_nWP	25	IPD	SD Write Protected: This pin is an input signal with an internal weak pull-down. This pin has an internally controlled weak pull-down resistor.

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
USB INTERFACE			
USBDM USBDP	87 88	I/O-U	USB Bus Data: These pins connect to the USB bus data signals.
RBIAS	98	I	USB Transceiver Bias: A 12.0kΩ, ± 1.0% resistor is attached from VSSA to this pin, in order to set the transceiver's internal bias currents.
ATEST	99	AIO	Analog Test: This signal is used for testing the analog section of the chip and should be connected to VDDA33 for normal operation.
VDD18PLL	101		1.8v Power for the PLL
VSSPLL	104		PLL Ground Reference: Ground Reference for 1.8v PLL power
VDDA33	89		3.3v Analog Power
VSSA	86		Analog Ground Reference: Analog Ground Reference for 3.3v Analog Power.
XTAL1/ CLKIN	102	ICLKx	Crystal Input/External Clock Input: 24Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 24Mhz clock when a crystal is not used. **Note:** The 'MA[2:0] pins will be sampled while nRESET is asserted, and the value will be latched upon nRESET negation. This will determine the clock source and value.
XTAL2	103	OCLKx	Crystal Output: 24Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
MISC			
ACT_LED	114	I/O8	Media Activity LED: This active low output will blink if any media is accessed by the USB host.
VBUS	94	I/O8	VBUS Input: This pin should be connected to the USB bus VBUS signal through a 100KΩ resistor voltage divider to provide 2.5v when VBUS = 5.0v.
SD_nCD	110	I/O8	SD Card Detection: This is the card detection signal from SD socket to indicate if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MS_PWR	42	I/O8	MS Card Power drive of 3.3V @ 100mA.

<table>
<tr><th>SYMBOL</th><th>128-PIN VTQFP</th><th>BUFFER TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>CF_nPWR</td><td>105</td><td>I/O8</td><td>CF Card Power Control:

This active low output is intended to drive an external power control P-FET which will supply the CF card with power.</td></tr>
<tr><td>SM/xD_PWR</td><td>79</td><td>I/O8</td><td>SM / xD Card Power drive of 3.3V @ 100mA.</td></tr>
<tr><td>SD/MMC_PWR</td><td>44</td><td>I/O8</td><td>SD / MMC Card Power drive of 3.3V @ 200mA.</td></tr>
<tr><td>CLK_SEL[1:0]</td><td>92
93</td><td>I/O8</td><td>Clock Select:

These pins will select the maximum clock rate that the interface will operate at.

Table 5.1 CLK_SEL[1:0] Assignments
<table><tr><th>CLK_SEL1</th><th>CLK_SEL0</th><th>CLOCK RATE</th></tr><tr><td>X</td><td>1</td><td>SD/MMC and MS max clock is 15Mhz</td></tr><tr><td>0</td><td>0</td><td>SD/MMC max clock is 48Mhz; MS clock is set normally</td></tr><tr><td>1</td><td>0</td><td>SD/MMC max clock is 24Mhz; MS clock is set normally</td></tr></table></td></tr>
<tr><td>nRESET</td><td>115</td><td>IS</td><td>RESET input:

This active low signal is used by the system to reset the chip. The active low pulse should be at least 1µs wide.</td></tr>
<tr><td>nTEST[1:0]</td><td>95
96</td><td>I</td><td>TEST input:

These signals are used for testing the chip. User should normally tie them high externally, if the test function is not used.</td></tr>
<tr><td colspan="4">DIGITAL POWER, GROUNDS, and NO CONNECTS</td></tr>
<tr><td>VDD18</td><td>49
106</td><td></td><td>1.8v Digital Core Power:

+1.8V Core power

All VDD18 pins must be connected together on the circuit board.</td></tr>
<tr><td>VDD33</td><td>3
43
80
100
108
109</td><td></td><td>3.3v Power & Voltage Regulator Input:

3.3V Power & Regulator Input.

pins 100 & 108 supply 3.3V power to the internal 1.8V regulators.</td></tr>
<tr><td>VSS</td><td>15
16
47
84
85
97
112</td><td></td><td>Ground:

Ground Reference</td></tr>
</table>

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
NC	1 2 4 5 6 7 8 9 10 11 12 13 14 17 90 91 107 111 113 116 117 118 119 120 121 122 123 124 125 126 127 128		No Connect; pins must be left unconnected.

Notes:

- Hot-insertion capable card connectors are required for all flash media. It is required for SD connector to have Write Protect switch. This allows the chip to detect MMC card.
- VDD18 (Pin 106) and VDD18PLL (Pin 101) must have a 10uF +/-20% Low-ESR (equivalent series resistance) <0.1 ohm bypass capacitor to VSSA. These capacitors must be as close to these pins as possible.

5.2 Buffer Type Descriptions

Table 5.2 USB2226 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger
I/O8	Input/Output buffer with 8mA sink and 8mA source.
I/O8PU	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.

Table 5.2 USB2226 Buffer Type Descriptions (continued)

BUFFER	DESCRIPTION
I/O8PD	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
O8	Output buffer with 8mA sink and 8mA source.
O8PU	Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
O8PD	Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog Input/Output Defined in USB specification
AIO	Analog Input/Output

Chapter 6 DC Parameters

6.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
3.3V supply voltage	V_{DD33}, V_{DDA33}	-0.5	4.0	V	
Voltage on VBUS & USBDP/DM pins		-0.5	(3.3V supply voltage + 2) ≤ 6	V	
Voltage on MS_PWR, SD/MMC_PWR, SM/xD_PWR		-0.5	V_{DD33} + 0.3	V	When internal power FET operation of these pins is enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63V and T_A is less than 70°C.
Voltage on any signal pin		-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	V_{DD18} + 0.3	V	

Note: Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

6.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Operating Temperature	T_A	0	70	°C	
3.3V supply voltage	V_{DD33}, V_{DDA33}	3.0	3.6	V	
Voltage on VBUS & USBDP/DM pins		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: (3.3V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	V_{DD33}	V	
Voltage on XTAL1		-0.3	V_{DDA33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

Table 6.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I,IPU & IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		500		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	mA	V_{IN} = V_{DD33}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O8, O8PU, and O8PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -8mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 6.1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
I/O8, I/O8PU & I/O8PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} _ 0.4			V	I_{OH} = -8 mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 6.1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 6.2)						

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Integrated Power FETs for MS_PWR or SM/xD_PWR						
Output Current	I_{OUT}	100			mA	MS_PWR or SM/xD_PWR; $Vdrop_{FET}$ = 0.23V
Short Circuit Current Limit	I_{SC}			140	mA	MS_PWR or SM/xD_PWR; $Vout_{FET}$ = 0V
On Resistance	R_{DSON}			2.1	Ω	MS_PWR or SM/xD_PWR; I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	MS_PWR or SM/xD_PWR; C_{LOAD} = 10µF
Integrated Power FET for SD/MMC_PWR						
Output Current	I_{OUT}	200			mA	SD/MMC_PWR; $Vdrop_{FET}$ = 0.46V
Short Circuit Current Limit	I_{SC}			181	mA	SD/MMC_PWR; $Vout_{FET}$ = 0V
On Resistance	R_{DSON}			2.1	Ω	SD/MMC_PWR; I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	SD/MMC_PWR; C_{LOAD} = 10µF
Supply Current Unconfigured	I_{CCINIT}		55	80	mA	
Supply Current Active (Full Speed)	I_{CC}		75	90	mA	
Supply Current Active (High Speed)	I_{CC}		75	100	mA	
Supply Current Standby	I_{CSBY}		305	420	µA	

Note 6.1 Output leakage is measured with the current pins in high impedance.

Note 6.2 See Appendix A for USB DC electrical characteristics.

Note 6.3 The Maximum power dissipation parameters of the package should not be exceeded.

6.3 Capacitance

T_A = 25°C; fc = 1MHz; V_{DD18}, $V_{DD18PLL}$ = *1.8V*

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 7 Package Outlines

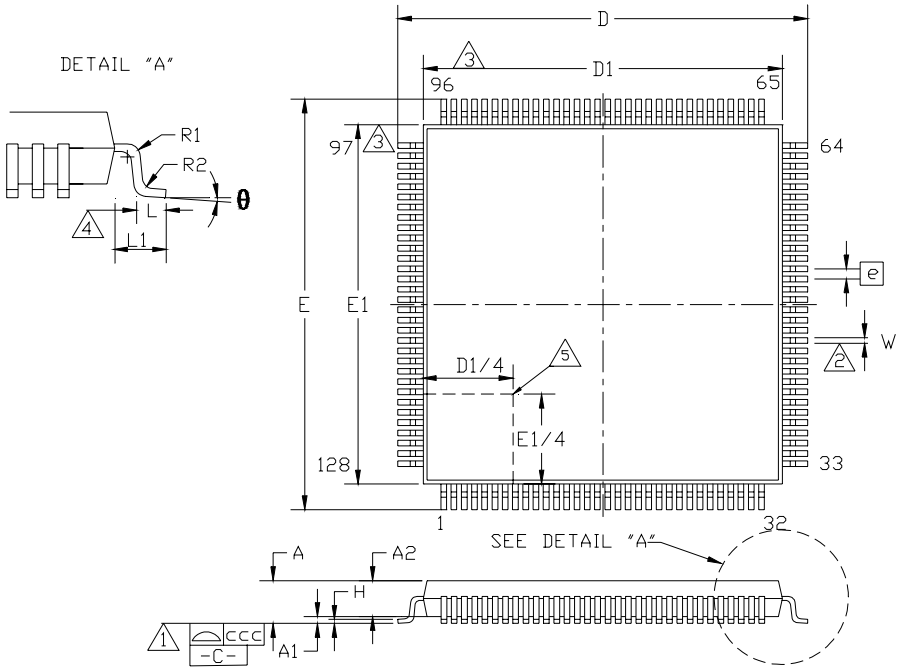

Figure 7.1 USB2226 128-Pin VTQFP Package Outline

Table 7.1 USB2226 128-Pin VTQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.035 mm maximum.
   Package body dimensions D1 and E1 do not include the mold protrusion.
3. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.