N S S D

(NAND Flash-based Solid State Disk)

Module Type
Product Data sheet
Version 1.1
Sep 2006

Document Title

SAMSUNG NAND Flash-based Solid State Disk

Revision History

Revision No	History	Draft Date	Remark
0.5	Initial issue	May.09.2006	Preliminary
1.0	Physical dimension was added(Slim 4/8/16GB) GND PAD was added on Slim 32GB Supporting SECURITY FEATURE Set Supporting SMART FEATURE Set Supporting HOST PROTECTED AREA FEATURE Set Identify Device Data was updated Software/Hardware Reset State Diagram was added	Aug.18.2006	Final
1.1	Misprint was modified(page 56) (In graph, R/$\overline{B}$ -> BSY) Product line-up was added(page 65) (A-die based Small 8/16GB) (Shared PCB based Slim 4/8/16/32GB)	Sep.27.2006	Final

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

1. General Description

The NSSD(Nand Flash-based Solid State Disk) of Samsung Electronics is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology for a storage media.
As the NSSD doesn't have a moving parts such as platter(disk) and head media, it gives a good solution in a sub. note PC and Tablet PC for a storage device with a high performance and a power consumption and a small form factor.
Also it gives rugged features in industrial PC with an extreme environment and an increased MTBF.
For an easy adoption, the NSSD has a same host interface with HDD and has a same physical dimension.

•Density
- 8GB,16GB,32GB NSSD are available

•Form Factor
- Small Type (56 x 48 x 3.8mm) : 8/16GB
- Slim Type (53.60 x 70.60 x 3.00mm) :32GB
  (53.60 x 70.60 x 2.50mm) : 4/8/16GB

•Host interface
- PIO Mode 0 to 4.
- Multiword DMA
- Up to ATA5 UDMA Mode4 (66MHz)

•Performance
- Host Interface : Max 66MB/s
- Sustained Data Read : Max 56MB/s
- Sustained Data Write : Max 32MB/s

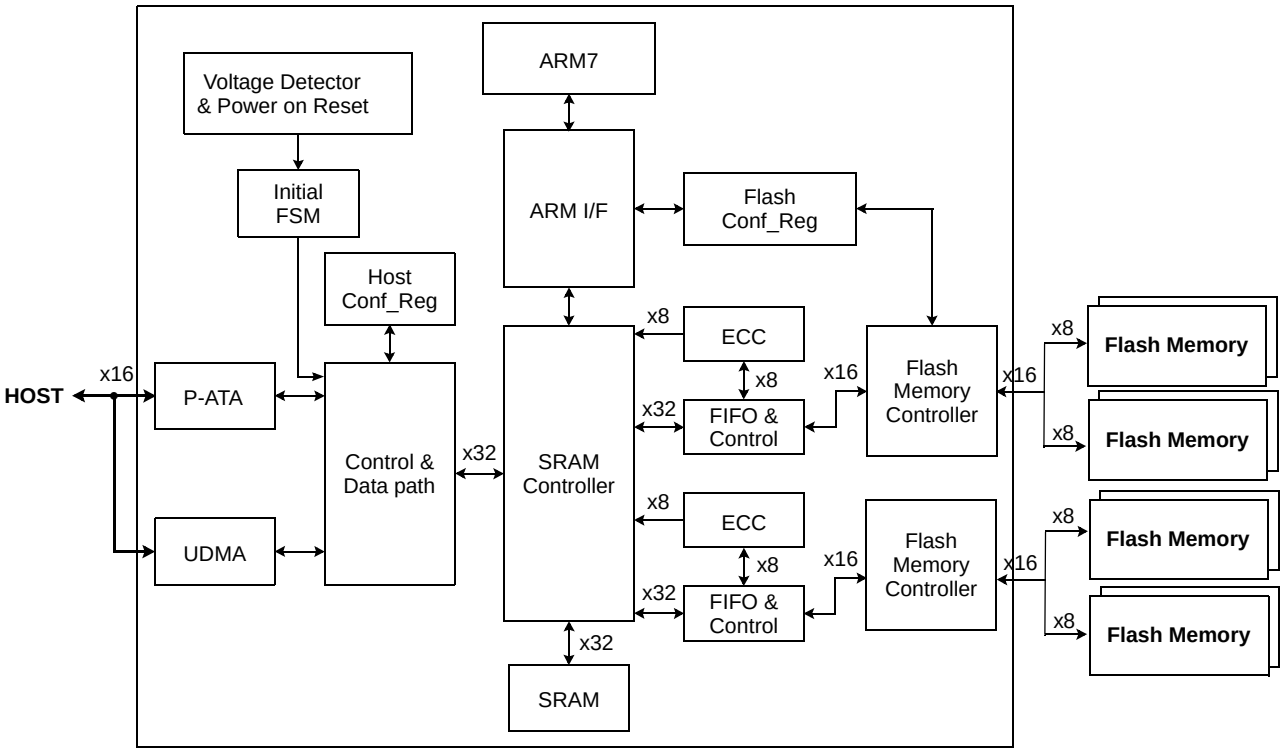
•Power consumption
- Active : Typical 200mA
- Idle : Typical 20mA
- Standby : Typical 20mA

•Temperature
- Operating : -25'C ~ 85'C

•Shock
- Operating : 1500G, duration 0.5ms, Half Sine Wave
- Vibration : 20G Peak, 10~2000Hz,(12Cycle/Axis)x3 Axis

•MTBF
- 1,000,000 Hours

•NSSD Functional Block Diagram



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2. Physical Specifications

2.1 Small Type Physical Dimensions (8/16GB)

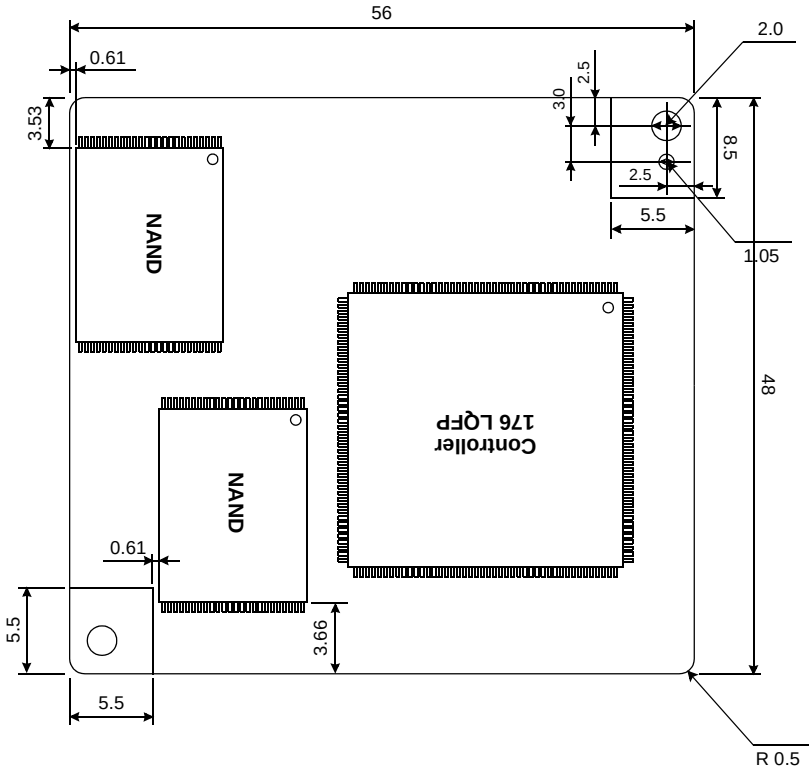


Figure 1. Small Type(8/16GB) Top

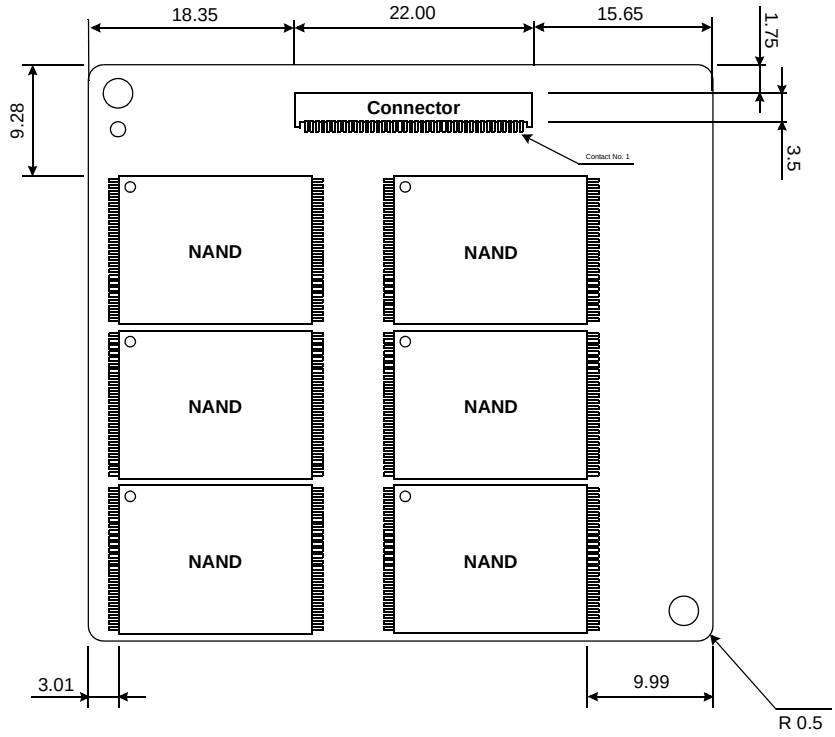


Figure 2. Small Type(8/16GB) Bottom

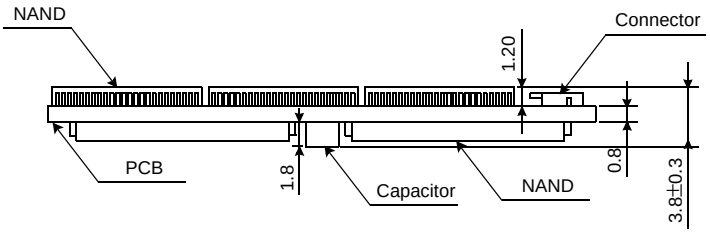


Figure 3. Small Type(8/16GB) Side

2.2 Slim Type Physical Dimensions (4/8/16GB)

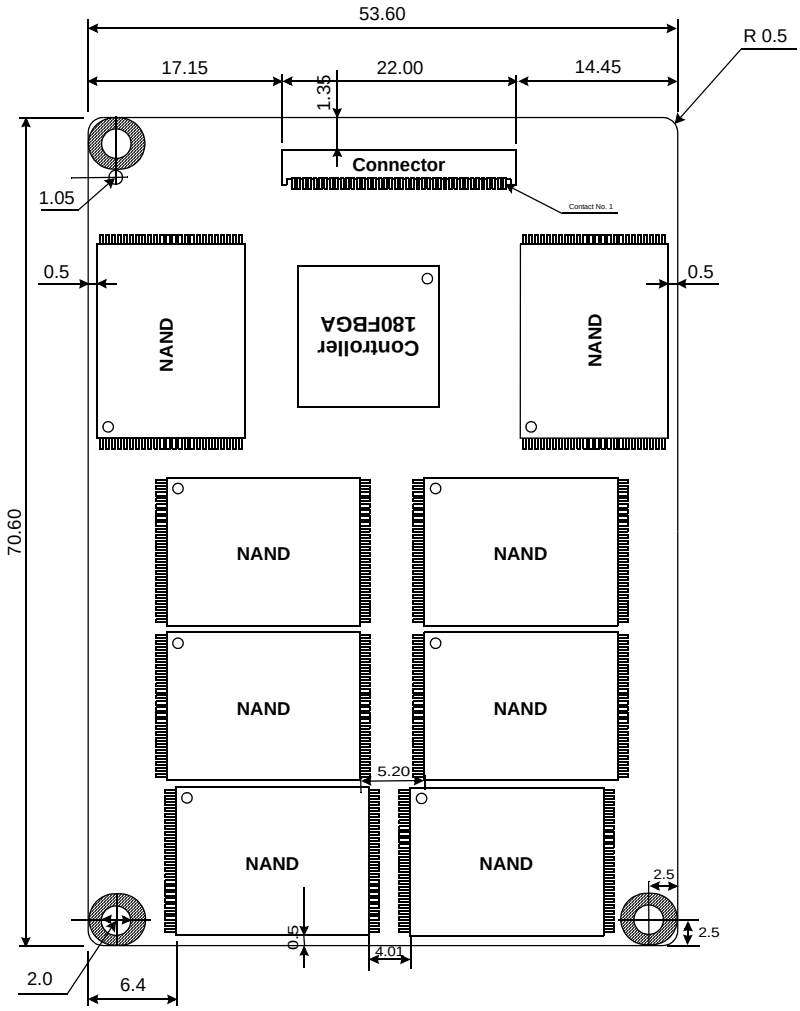


Figure 4. Slim Type(4/8/16GB) Top

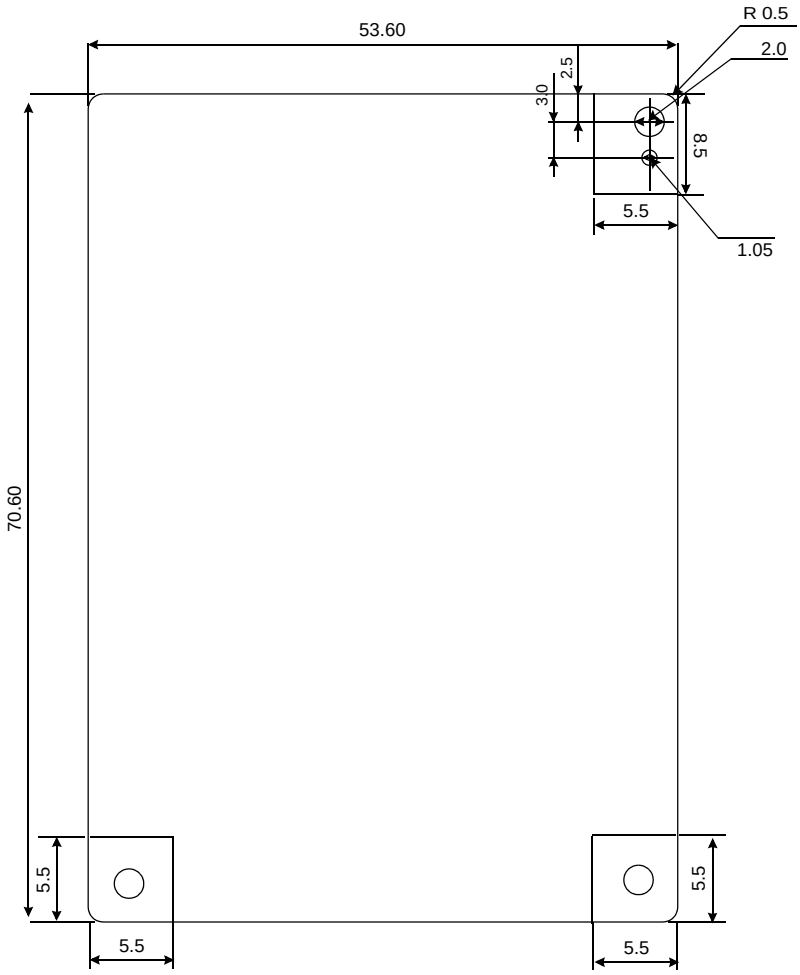


Figure 5. Slim Type(4/8/16) Bottom

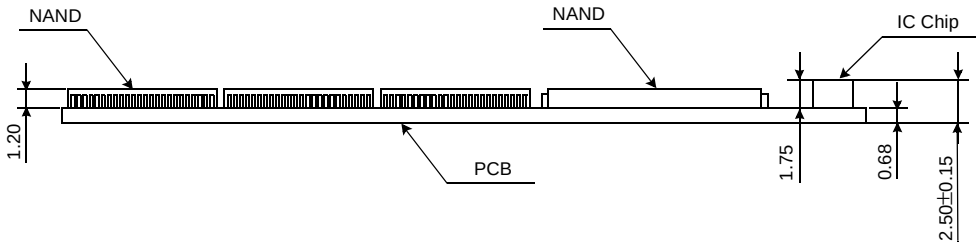


Figure 6. Slim Type(4/8/16GB) Side

2.3 Slim Type Physical Dimensions (32GB)

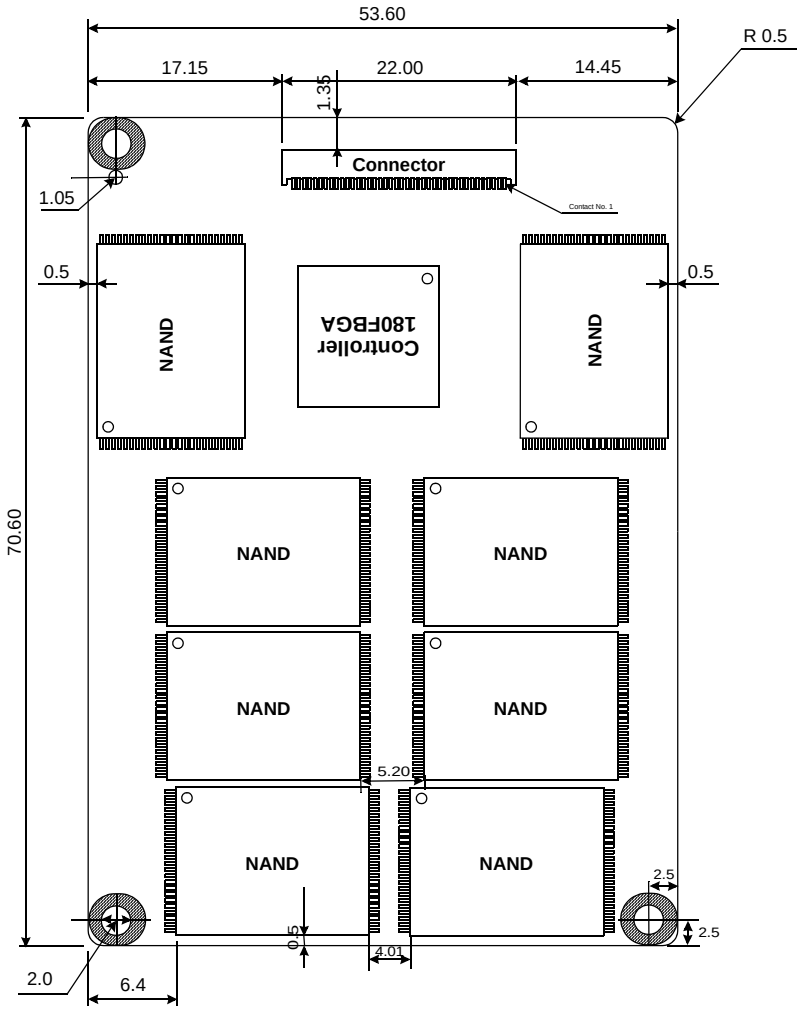


Figure 7. Slim Type(32GB) Top

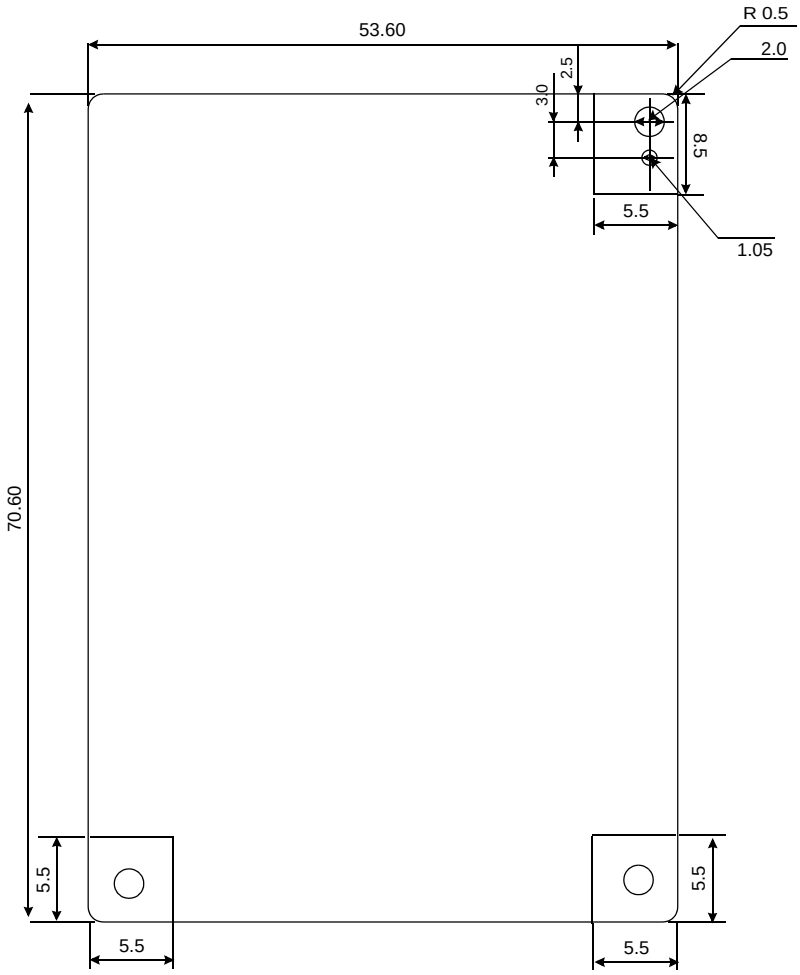


Figure 8. Slim Type(32GB) Bottom

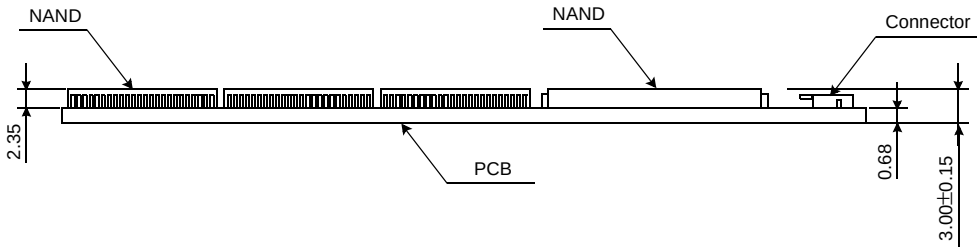


Figure 9. Slim Type(32GB) Side

3. Product Specifications

3.1 System Interface and Configuration

- PIO 0~4 mode,
- Up to ATA5 and UDMA mode4(Ultra DMA66)
- Fully compatible with ATA5 Specification

3.2 System Performance

(Sandra 2005, 32GB)

Read / Write	Performance(MB/s)
Random Read Sector	Max 56
Random Write Sector	Max 13
Sequential Read Sector	Max 56
Sequential Write Sector	Max 32

3.3 System Power Consumption

(32GB)

Current	Typical(mA)
Active	200
Idle	20
Standby	20

3.4 System Reliability

MTBF	1,000,000 Hours

3.5 Environmental Specifications

Features	Operating	Non-Operating
Temperature	-25'C ~ 85'C	-40'C ~ 85'C
Humidity	0'C to 55'C / 90~98% RH, 10cycles	
Vibration	20G Peak, 10 ~ 2000Hz, (12cycle / Axis) x3 Axis	
Shock	1500G, duration 0.5ms, Half Sine Wave	

4. Electrical Specification

4.1 ZIF Connector Dimensions

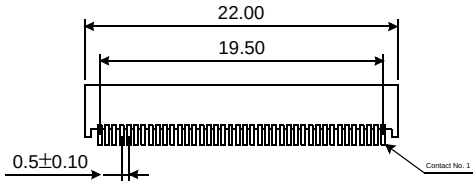


Figure 7. Connector Top

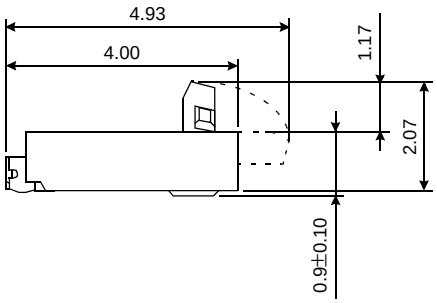


Figure 8. Connector Side

*ZIF: Zero Insertion Force

4.2 Pin Assignment

Pin No	Signals	Pin No	Signals
1	Reserved	21	GROUND
2	Reserved	22	DMARQ
3	$\overline{\text{RESET}}$	23	GROUND
4	GROUND	24	$\overline{\text{DIOW}}$
5	DD7	25	$\overline{\text{DIOR}}$
6	DD8	26	GROUND
7	DD6	27	IORDY
8	DD9	28	GROUND
9	DD5	29	$\overline{\text{DMACK}}$
10	DD10	30	INTRQ
11	DD4	31	DA1
12	DD11	32	$\overline{\text{PDIAG}}$
13	DD3	33	DA0
14	DD12	34	DA2
15	DD2	35	$\overline{\text{CS0}}$
16	DD13	36	$\overline{\text{CS1}}$
17	DD1	37	$\overline{\text{DASP}}$
18	DD14	38	3.3V
19	DD0	39	3.3V
20	DD15	40	Reserved

4.3 Signal Descriptions

"I" of I/O type represents an input signal from the device and "O" represents an output signal from the device.

Signal name	Pin NO	Type	Description
$\overline{\text{RESET}}$	3	I	This is a reset signal output from the host system and to be used for interface logic circuit.
DD0 - DD15	5-20	I/O	This is a 16bit bi-directional data bus. The lover 8 bits are used for register acess other that data register.
$\overline{\text{DIOW}}$	24	I	This rising edge of this Write Strobe signal clocks data from the host data bus into a register on the device.
STOP*			Assertion of this signal by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
$\overline{\text{DIOR}}$	25	I	Activating this Read Strobe signal enables data from a register on the device to be clocked onto the host data bus. The rising edge of this signal latches data at the host.
$\overline{\text{HDMARDY}}$*			This signal is a flow control signal for Ultra DMA Read. Host asserts this signal, and indicates that the host is ready to receive Ultra DMA read data.
HSTROBE*			This signal is Write data strobe signal from the host for an Ultra DMA Write. Both the rising and falling edge latch the data from DD(15:0) into the device.
IORDY	27	O	This signal is used to temporarily stop the host register access(read or write) when the device is not ready to respond to a data transfer request.
$\overline{\text{DDMARDY}}$*			This signal is flow control signal for Ultra DMA Write. Device asserts this signal, and indicates that the device is ready to receive Ultra DMA Write data.
DSTROBE*			This signal is the data in strobe signal from the device for an Ultra DMA Read. Both the rising and falling edge latch the data from DD(15:0) into the host.
INTRQ	30	O	This is an interrupt signal for the host system. This signal is asserted by a selected device when the nIEN bit in the Device Control Register is "0". In other cases, this signal should be a high impedance state.
DA0-2	31,33,34	I	This is a register address signal from the host system.
$\overline{\text{PDIAG}}$:CBLID*	32	I/O	The host shall wait until the power on or hardware reset sequence is complete for all devices on the cable;
$\overline{\text{CS0}}$	35	I	This device chip selection signal is used to select the Control Block Registers from the host system.
$\overline{\text{CS1}}$	36	I	This device chip selection signal is used to select the Command Block Registers from the host system.
$\overline{\text{DASP}}$	37	I/O	This signal indicates that a device is active when the power is turned on. Upon receipt of a command from the host, the device asserts this signal. At command completion, the device de-asserts this signal.
DMARQ	22	O	The device shall assert this signal, used for DMA data transfers between host and device, when it is ready to transfer data.
$\overline{\text{DMACK}}$	29	I	The host in response to DMARQ to either acknowledge that data has been accepted, or that data is available shall use this signal.
DEVADR	40	I	The device is configured as either Device 0(Master) or Device 1(Slave) depending upon the signal level of 40 pin DEVADR signal. - When used as Device 1(Master), DEVADR is open - When used as Device 1(Slave), the host shall have pull-up resistor. Recommended pull-up register is 10K ohm based on +3.3Vcc.

4.4 DC Characteristics

4.4.1 Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	-0.3 to 4.6	V
Input/Output Voltage	V_{IN}/V_{OUT}	3.8	V
DC Input Current	I_{IN}	+/- 200	mA
Storage Temperature	T_{STG}	-40 to 85	°C

4.4.2 Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	3.0 to 3.6	V
Input/Output Voltage	V_{IN}/V_{OUT}	3.0 to 3.6	V
Operating Temperature	T_{OPR}	-25 to 85	°C

4.4.3 Electrical Characteristics - Normal I/O

Vdd = 3.0 to 3.6(V), Ta = 25(°C), Vext = 5V ± 0.25V

Characteristics	Symbol	Test Condition		Min	Typ	Max	Unit
Input High Current	I_{IH}	$V_{IN} = V_{DD}$ Pull - Down	Normal Down	-10 10	- -	10 60	uA uA
Input Low Current	I_{IL}	$V_{IN} = V_{SS}$ Pull - Up	Normal Up	-10 -60	- -	10 -10	uA uA
Input High Voltage	V_{IH}	CMOS		2.0	-	-	V
Input Low Voltage	V_{IL}	CMOS		-	-	0.8	V
Output High Voltage	V_{OH}	6mA Buffer, I_{OH} = -6mA		2.4	-	-	V
Output Low Voltage	V_{OL}	6mA Buffer, I_{OL} = 6mA		-	-	0.4	V
Tri-state Output Leakage Current	I_{OZ}	$V_{OUT} = V_{DD}$ or V_{SS}		-10	-	10	uA

NOTE:
* Schmitt Trigger test condition : V_{DD} = 3.0 to 3.6(V), Ta = 25(°C)

Characteristic:
These DC parameters guarantee the I/O cell characteristic at the static state only, not at the dynamic state.

4.5 AC Characteristics

4.5.1 Register Transfers

Figure 1 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO mode 3 or 4 shall power-up in a PIO mode 0,1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 1 defines the minimum value that shall be placed in word 68.

Both hosts and devices shall support IORDY when PIO mode 3 or 4 are the currently selected mode of operation.

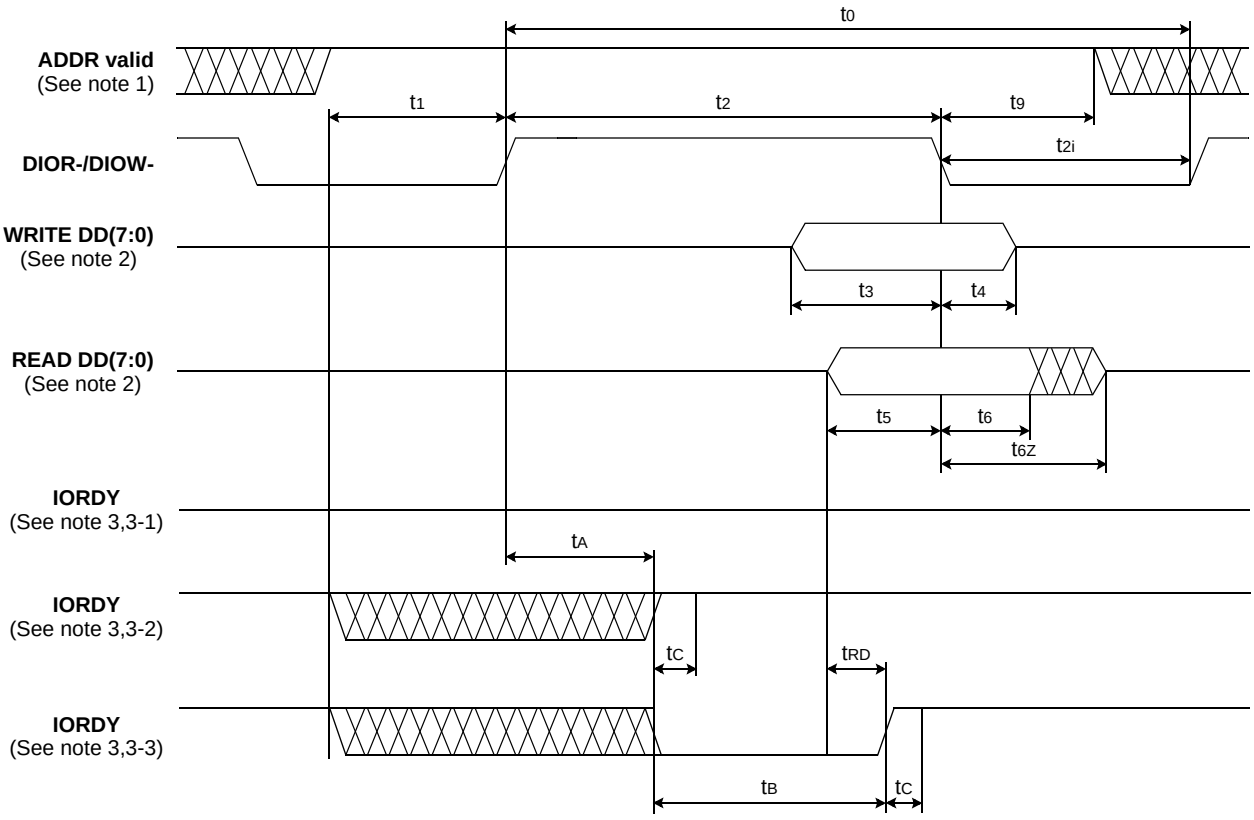


Figure 1. Register transfer to/from device.

NOTE:
1. Device address consists of signals CS0-, CS1- and DA(2:0)
2. Data consists of DD(7:0)
3. The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
   3-1. Device never negates IORDY, devices keeps IORDY released: no wait is generated.
   3-2. Device negates IORDY before t_A, but causes IORDY to be asserted before t_A.
   IORDY is released prior to negation and may be asserted for no more than 5ns before release: no wait generated.
   3-3. Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5ns before release: wait generated.
   The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.
4. DMACK- shall remain negated during a register transfer.

Table 1 - Register transfer to/from device

Register transfer timing parameters			Mode 0ns	Mode 1ns	Mode 2ns	Mode 3ns	Mode 4ns	Note
t_0	Cycle time	min	600	383	330	180	120	1,4,5
t_1	Address valid to DIOR-/DIOW- setup	min	70	50	30	30	25	
t_2	DIOR-/DIOW- pulse width 8bit	min	290	290	290	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	min	-	-	-	70	25	1
t_3	DIOW- data setup	min	60	45	30	30	20	
t_4	DIOW- data hold	min	30	20	15	10	10	
t_5	DIOR- data setup	min	50	35	20	20	20	
t_6	DIOR- data hold	min	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	max	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	min	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	min	0	0	0	0	0	
t_A	IORDY setup time		35	35	35	35	35	3
t_B	IORDY pulse width	max	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release	max	5	5	5	5	5	

NOTE:

1. t_0 is the minimum total cycle time, t_2 is the minimum DIOR-/DIOW- assertion time, and A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices INDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.
3. The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.
4. ATA/ATAPI standards prior to ATA/ATAPI-5 inadvertently specified an incorrect value for mode2 time t0 by utilizing the 16-bit PIO value.
5. Mode shall be selected no faster than the highest mode supported by the slowest device.

4.5.2 PIO Data Transfers

Figure 2 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power-up in a PIO mode 0,1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 2 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

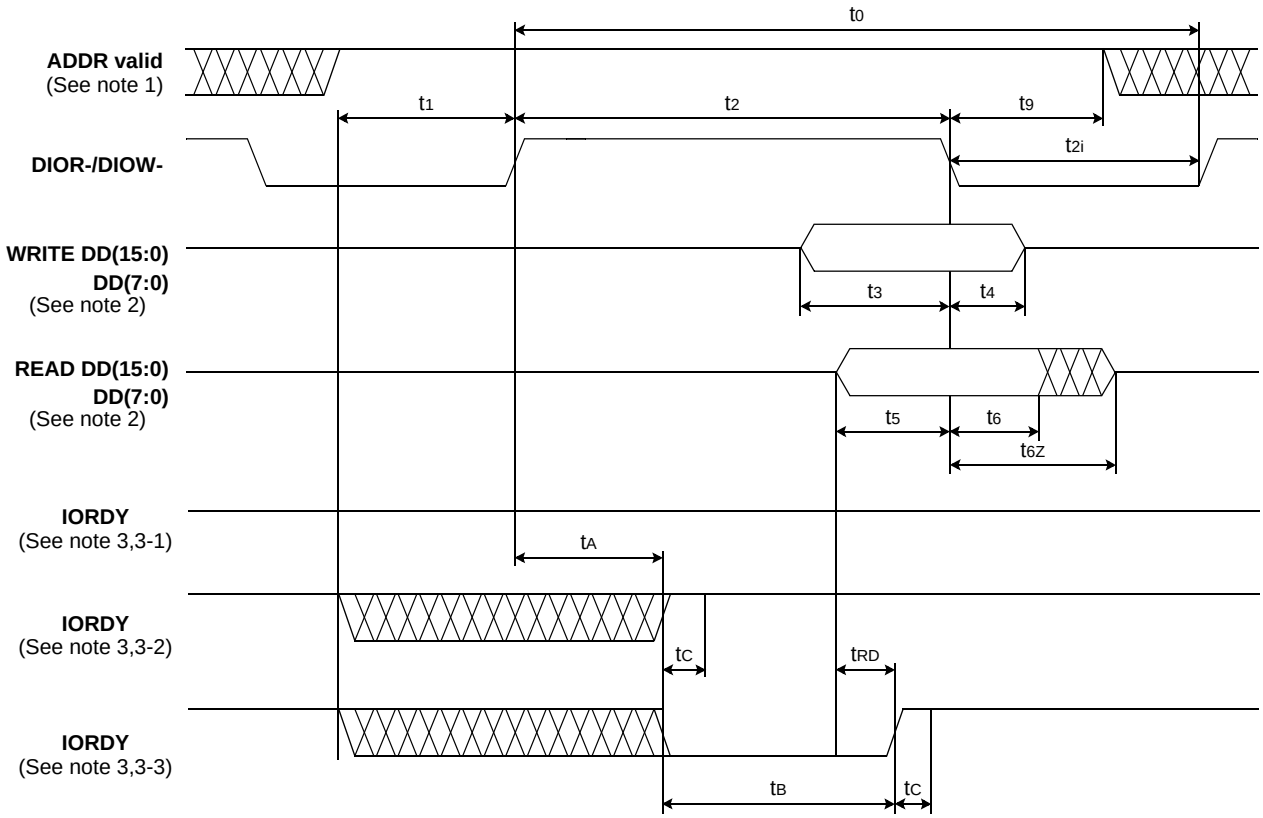


Figure 2. PIO data transfer to/from device.

NOTE:
1. Device address consists of signals CS0-, CS1- and DA(2:0)
2. Data consists of DD(15:0) for all devices except devices implementing the CFA feature set when 8-bit transfers is enabled. In that case, data consists of DD(7:0)
3. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
   3-1. Device never negates IORDY, devices keeps IORDY released: no wait is generated.
   3-2. Device negates IORDY before t_A, but causes IORDY to be asserted before t_A.
   IORDY is released prior to negation and may be asserted for no more than 5ns before release: no wait generated.
   3-3. Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5ns before release: wait generated.
   The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.
4. DMACK- shall be negated during a PIO data transfer.

Table 2 - PIO data transfer to/from device

PIO timing parameters			Mode 0ns	Mode 1ns	Mode 2ns	Mode 3ns	Mode 4ns	Note
t_0	Cycle time	min	600	383	240	180	120	1,4
t_1	Address valid to DIOR-/DIOW- setup	min	70	50	30	30	25	
t_2	DIOR-/DIOW-	min	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	min	-	-	-	70	25	1
t_3	DIOW- data setup	min	60	45	30	30	20	
t_4	DIOW- data hold	min	30	20	15	10	10	
t_5	DIOR- data setup	min	50	35	20	20	20	
t_6	DIOR- data hold	min	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	max	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	min	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	min	0	0	0	0	0	
t_A	IORDY setup time		35	35	35	35	35	3
t_B	IORDY pulse width	max	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release	max	5	5	5	5	5	

NOTE:
1. t_0 is the minimum total cycle time, t_2 is the minimum DIOR-/DIOW- assertion time, and t_{21} is the minimum DIOR-/DIOW- negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.
3. The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.
4. Mode may be selected at the highest mode for the device if CS(1:0) and AD(2:0) do not change between read or write cycles or selected at the highest mode supported by the slowest device if CS(1:0) or AD(2:0) do change between read or write cycles.

4.5.3 Multiword DMA Data Transfers

Figure 3 through Figure 6 define the timing associated with Multiword DMA transfers.

For Multiword DMA modes 1 and above, the minimum value of t_0 is specified by word 65 in the IDENTIFY DEVICE parameter list. Table 3 defines the minimum value that shall be placed in word 65.

Devices shall power-up with mode 0 as the default Multiword DMA mode.

Table 3 - Multiword DMA data transfer

Multiword DMA timing parameters			Mode 0ns	Mode 1ns	Mode 2ns	Note
t_0	Cycle time	min	480	150	120	see note
t_D	DIOR-/DIOW- asserted pulse width	min	215	80	70	see note
t_E	DIOR- data access	max	150	60	50	
t_F	DIOR- data hold	min	5	5	5	
t_G	DIOR-/DIOW-data setup	min	100	30	20	
t_H	DIOW- data hold	min	20	15	10	
t_I	DMACK to DIOR-/DIOW- data setup	min	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold	min	20	5	5	
t_{KR}	DIOR- negated pulse width	min	50	50	25	see note
t_{KW}	DIOW- negated pulse width	min	215	50	25	see note
t_{LR}	DIOR- to DMARQ delay	max	120	40	35	
t_{LW}	DIOW- to DMARQ delay	max	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW-	min	50	30	25	
t_N	CS(1:0) hold	min	15	10	10	
t_Z	DMACK- to read data released	max	20	25	25	

NOTE:
> t_0 is the minimum total cycle time, t_D is the minimum DIOR-/DIOW- assertion time, and t_K (t_{KR} or t_{Kw}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.

4.5.3.1 Initiating a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 50.

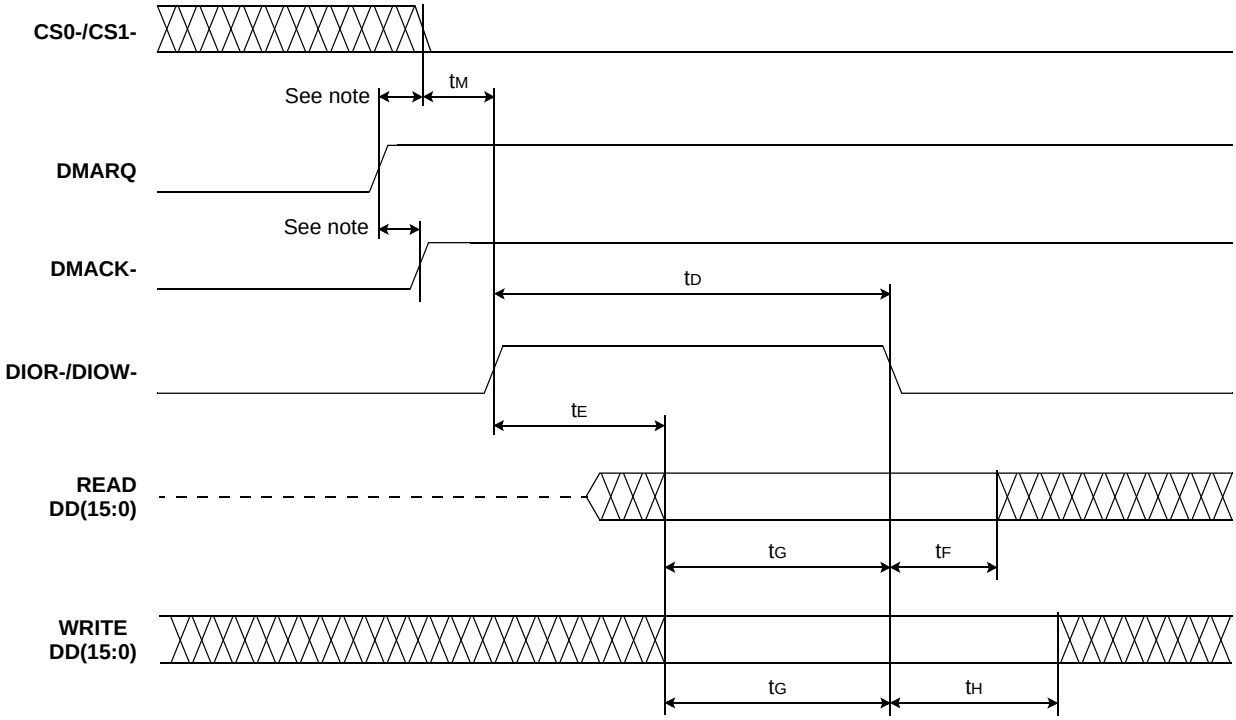


Figure 3. Initiating a Multiword DMA data transfer

NOTE:
The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maxium time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

4.5.3.2 Sustaining a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 50.

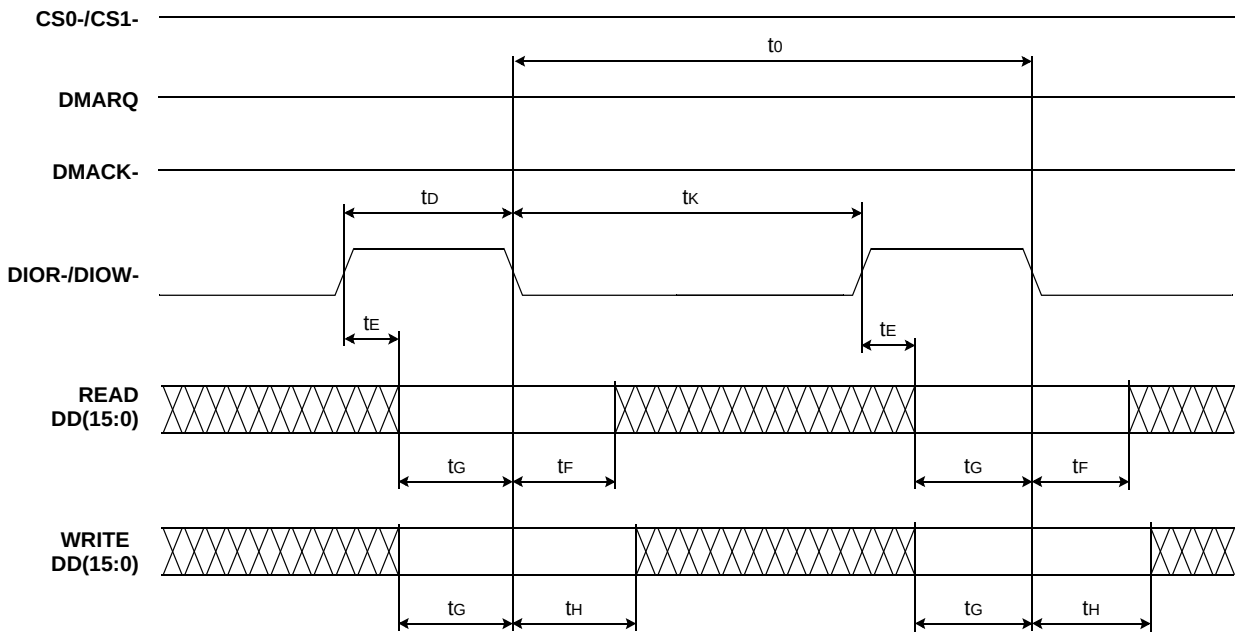


Figure 4. Sustaining a Multiword DMA data transfer

4.5.3.3 Device terminating a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 50.

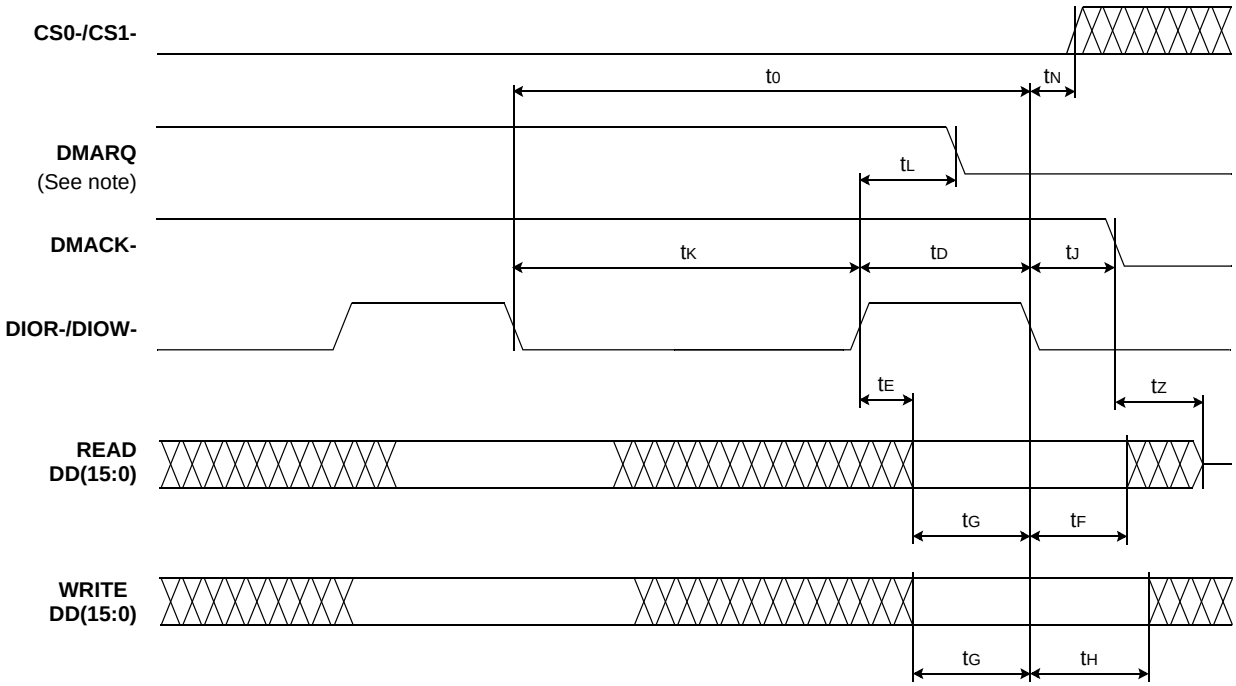


Figure 5. Device terminating a Multiword DMA data transfer

NOTE:
To terminate the data burst, the Host shall negate DMARQ within the tL of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the Host shall reassert DMARQ again at any later time to resume the DMA operation.

4.5.3.4 Host terminating a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 50.

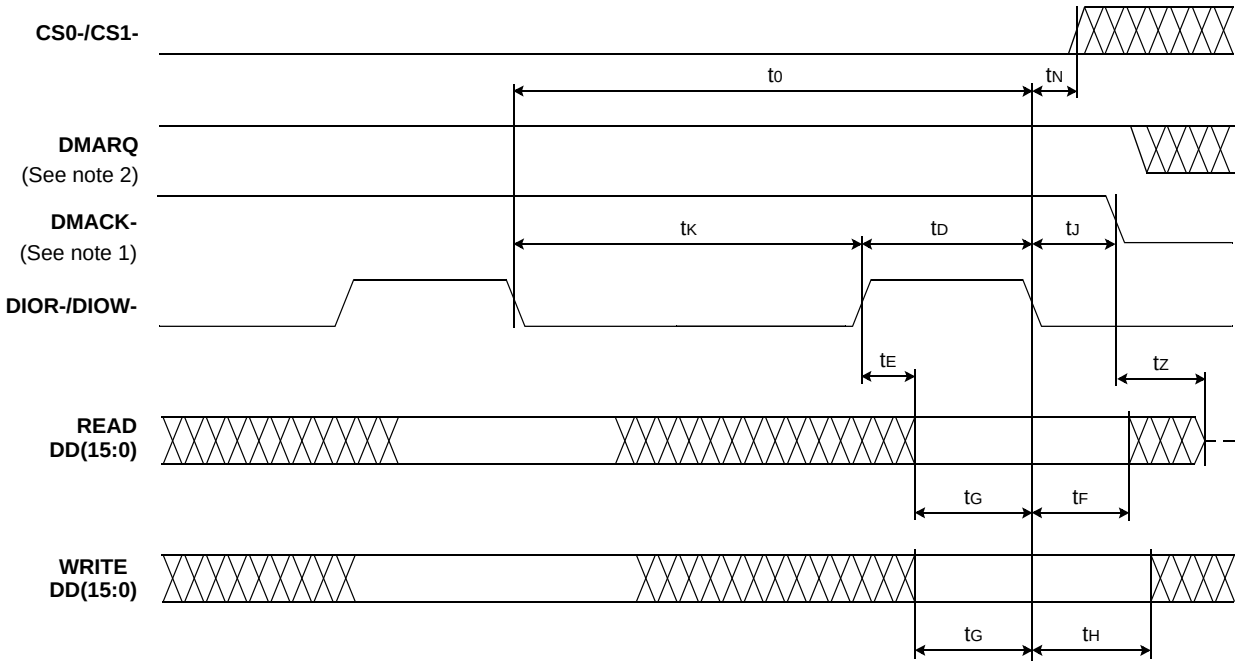


Figure 6. Host terminating a Multiword DMA data transfer

NOTE:

1. To terminate the transmission of a data burst, the host shall negate DMACK- within the specified time after a DIOR- or DIOW- pulse. No further DIOR- or DIOW- pulses shall be asserted for this burst.
2. If the device is able to continue the transfer of data, the Host may leave DMARQ asserted and wait for the host to reassert DMACK- or may negate DMARQ at any time after detecting that DMACK- has been negated.

4.5.4 Ultra DMA data burst

Figure 7 through Figure 16 define the timings associated with all phases of Ultra DMA bursts.
Table 4 contains the values for the timings for each of the Ultra DMA modes.

Table 4 - Ultra DMA data burst timing requirements

Name	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Comment (See Notes 1 and 2)
	min	max	min	max	min	max	min	max	min	max	
$t_{2CYCTYP}$	240		160		120		90		60		Typical sustained average two cycle time
t_{CYC}	112		73		54		39		25		Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	230		154		115		86		57		Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	15		10		7		7		5		Data setup time at recipient
t_{DH}	5		5		5		5		5		Data hold time at recipient
t_{DVS}	70		48		30		20		6		Data valid setup time at sender (from data valid until STROBE edge) (See Note 4)
t_{DVH}	6		6		6		6		6		Data valid hold time at sender (from STROBE edge until data may become invalid) (See Note 4)
t_{FS}	0	230	0	200	0	170	0	130	0	120	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	0	150	0	150	0	150	0	100	0	100	Limited interlock time (See Note 3)
t_{MLI}	20		20		20		20		20		Interlock time with minimum(See Note 3)
t_{UI}	0		0		0		0		0		Unlimited interlock time (See Note 3)
t_{AZ}		10		10		10		10		10	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	20		20		20		20		20		Minimum delay time required for output
t_{ZAD}	0		0		0		0		0		Drivers to assert or negate (from released)
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{SR}		50		30		20		NA		NA	STROBE-to-DMARDY- time (if DMARDY- is negated before this long after STROBE edge, the recipient shall receive no more than one additional data word)
t_{RFS}		75		70		60		60		60	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	160		125		100		100		100		Minimum time to assert STOP or negate DMARQ
t_{IORDYZ}		20		20		20		20		20	Maximum time before releasing IORDY
t_{ZIORDY}	0		0		0		0		0		Minimum time before driving STROBE (See Note 5)
t_{ACK}	20		20		20		20		20		Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

NOTE:
1. Timing parameters shall be measured at the connector of the sender or receiver to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after the negation of DMARDY-. Both STROBE and DMARDY- timing measurements are taken at the connector of the sender.
2. All timing measurement switching points(low to high and high to low) shall be taken at 1.5V.
3. t_{UI}, t_{MLI}, and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., either sender or recipient is waiting for the other to respond with a signal before proceeding. t_{UI} is an inlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
4. The test load for t_{DVS} and t_{DVH} shall be a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} shall be met for all capacitive loads from 15 to 40 pf where all signals have the same capacitive load value.
5. t_{ZIORDY} may be greater than t_{ENV} since the device has a pull up on IORDY- giving it a known state when released.

4.5.4.1 Initiating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

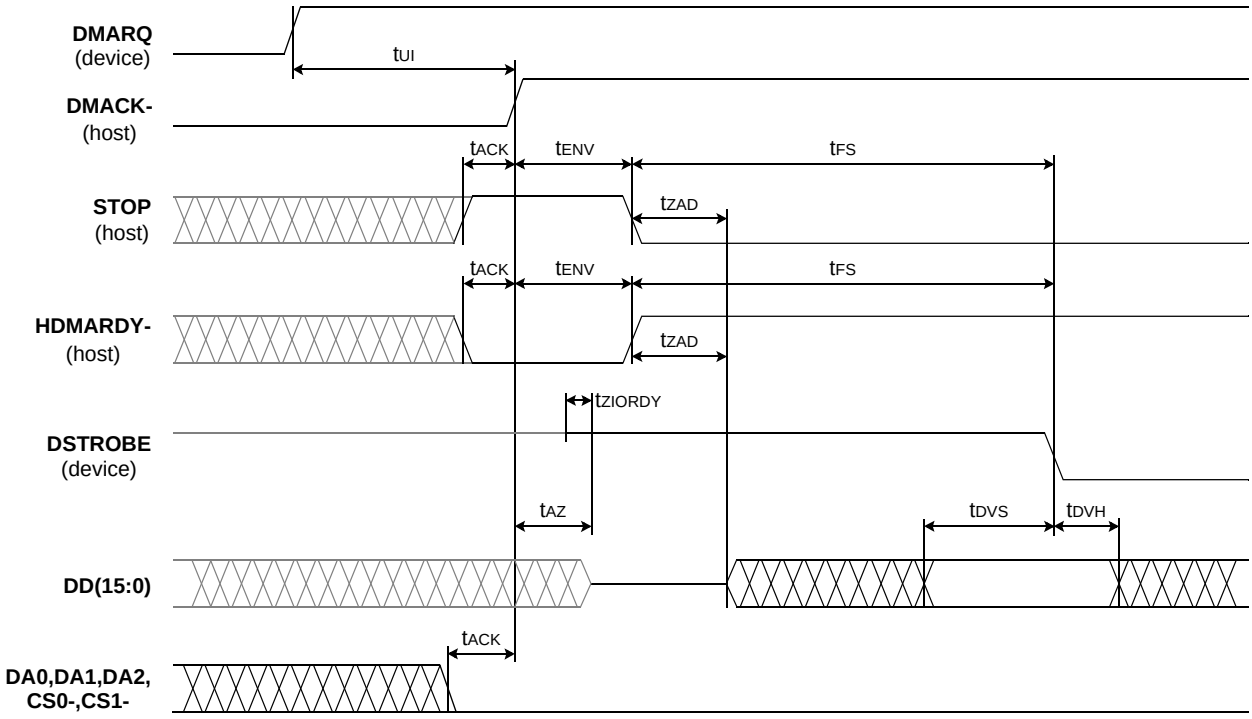


Figure 7. Initiating an Ultra DMA data-in burst

NOTE:
1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

4.5.4.2 Sustained Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

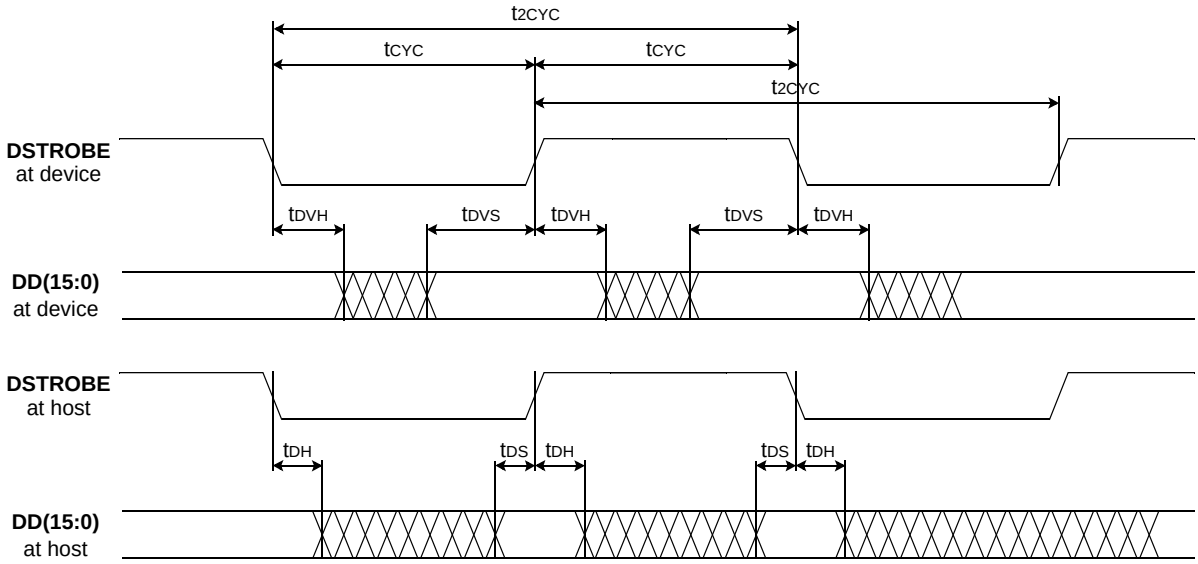


Figure 8. Sustained Ultra DMA data-in burst

NOTE:
1. DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

4.5.4.3 Host pausing an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

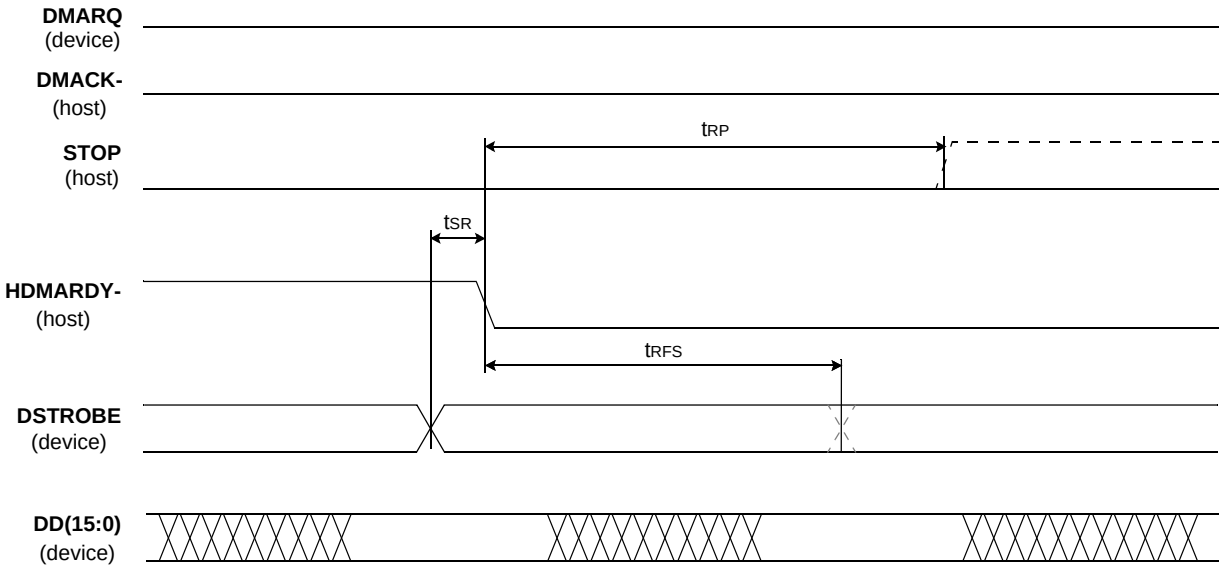


Figure 9. Host pausing an Ultra DMA data-in burst

NOTE:
1. The host mat assert STOP to request termination of the ultra DMA burst no sooner than tRP after HDMARDY- is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the Host.

4.5.4.4 Device terminating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

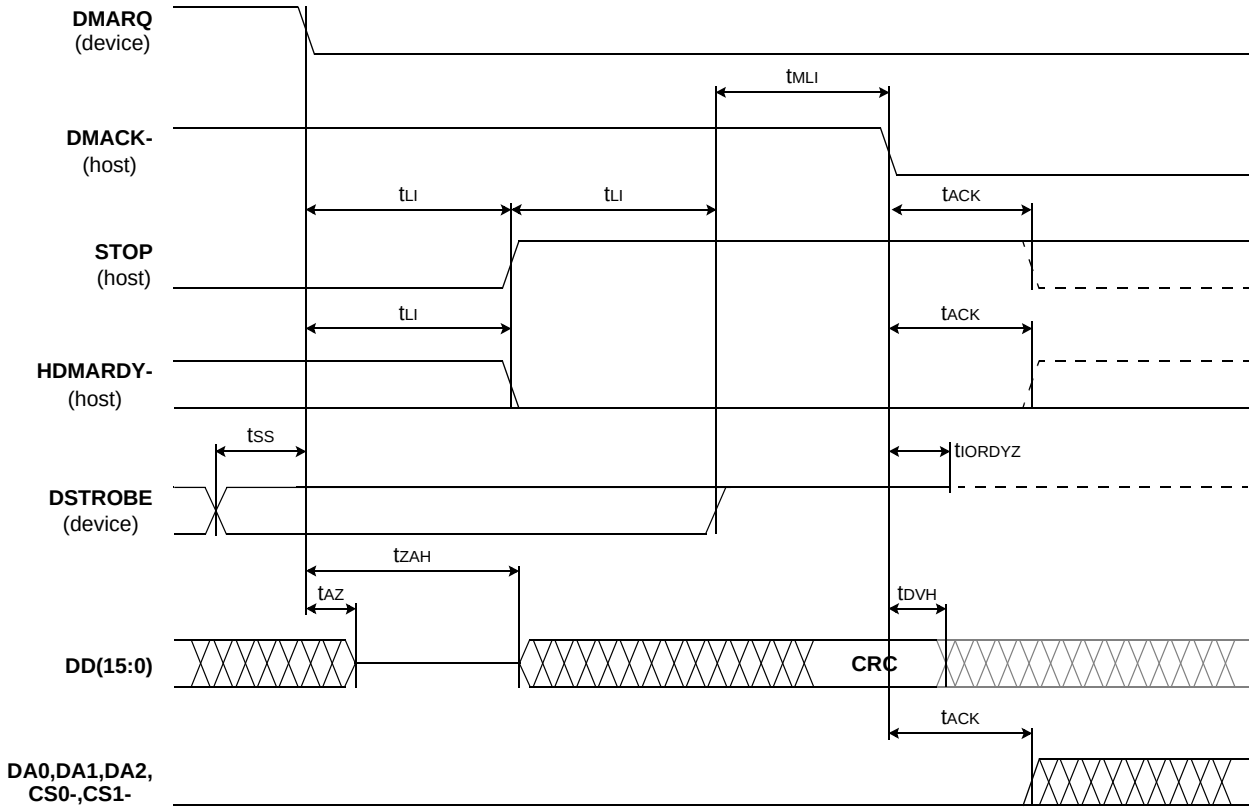


Figure 10. Device terminating an Ultra DMA data-in burst

NOTE:
1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

4.5.4.5 Host terminating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

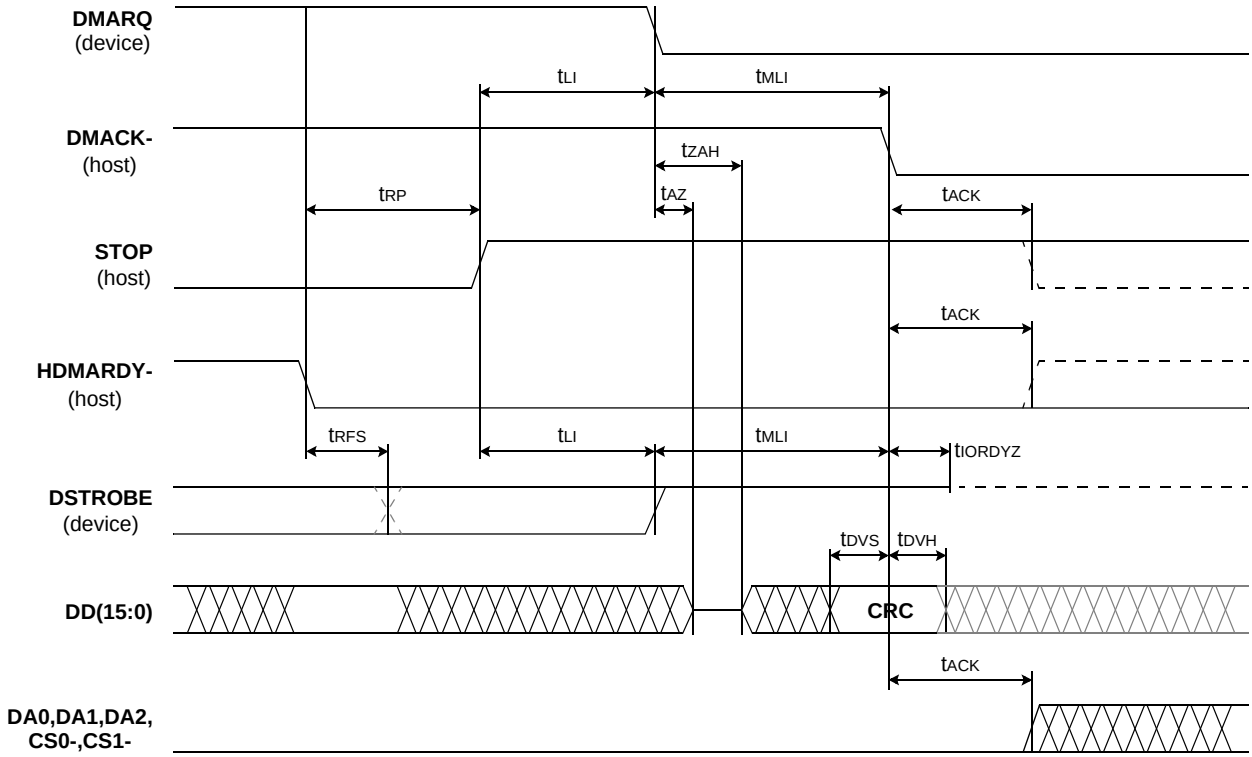


Figure 11. Host terminating an Ultra DMA data-in burst

NOTE:
1. The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

4.5.4.6 Initiating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

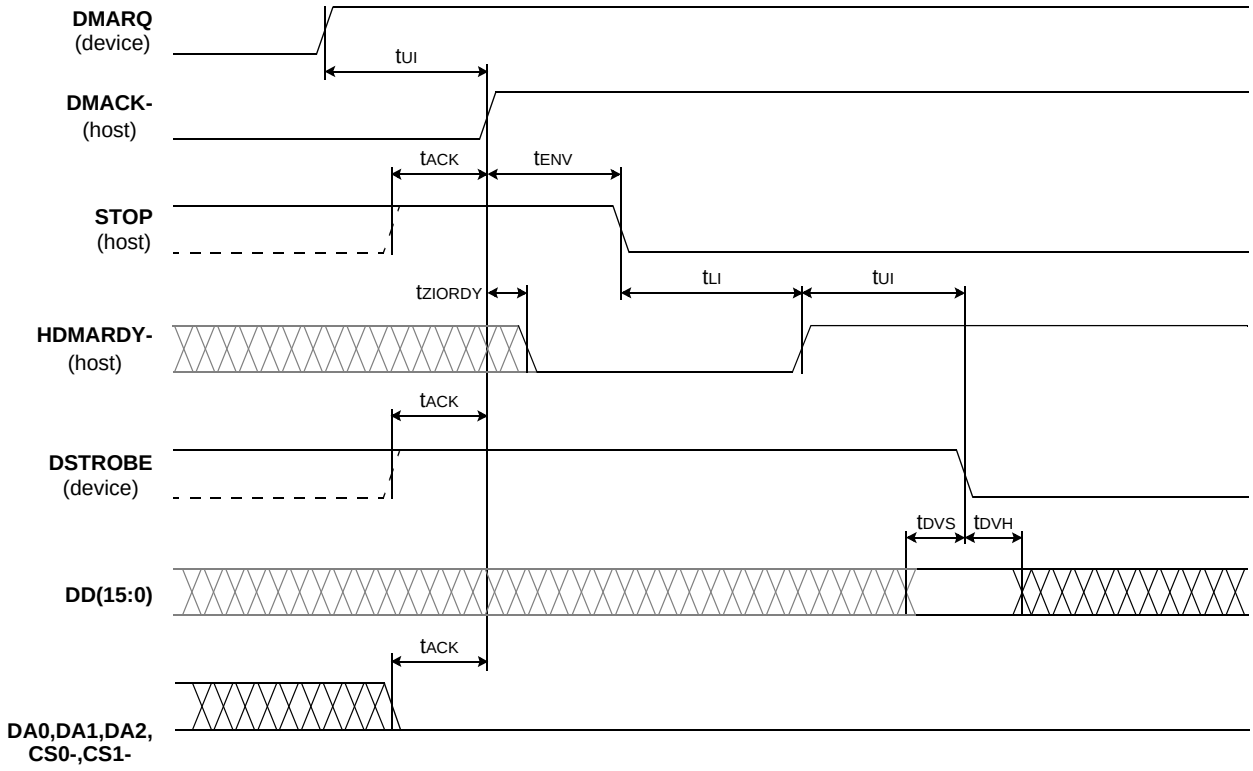


Figure 12. Initiating an Ultra DMA data-out burst

NOTE:
1. The definitions for the DIOW-:STOP,IORDY:DDMARDY-:DSTROBE and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

4.5.4.7 Sustained Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

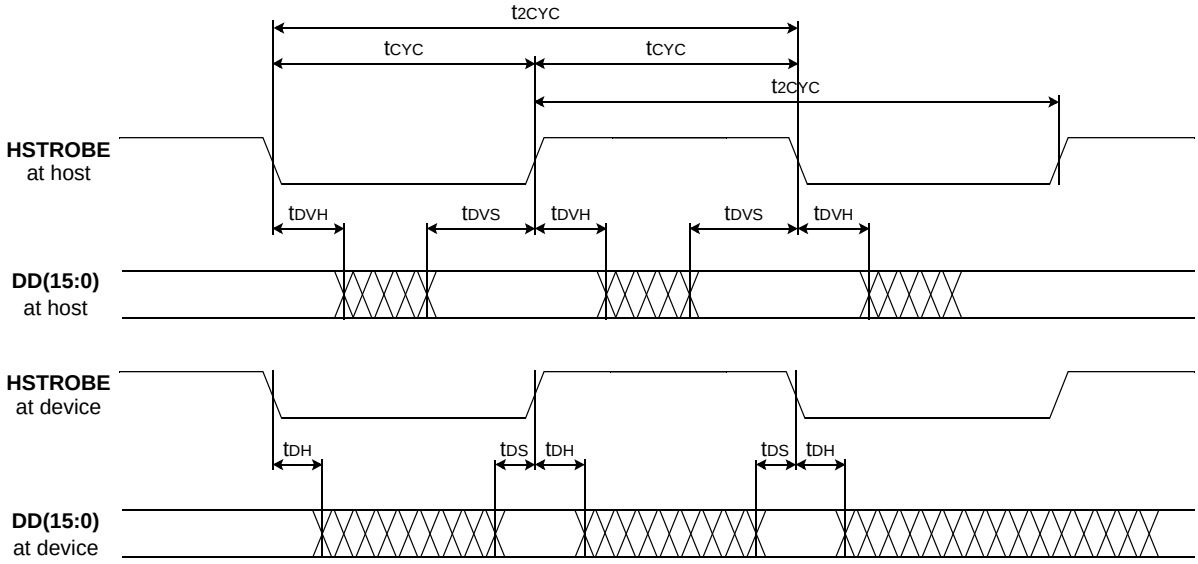


Figure 13. Sustained Ultra DMA data-out burst

NOTE:
1. DD(15:0) and HSTROBE signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

4.5.4.8 Device pausing an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

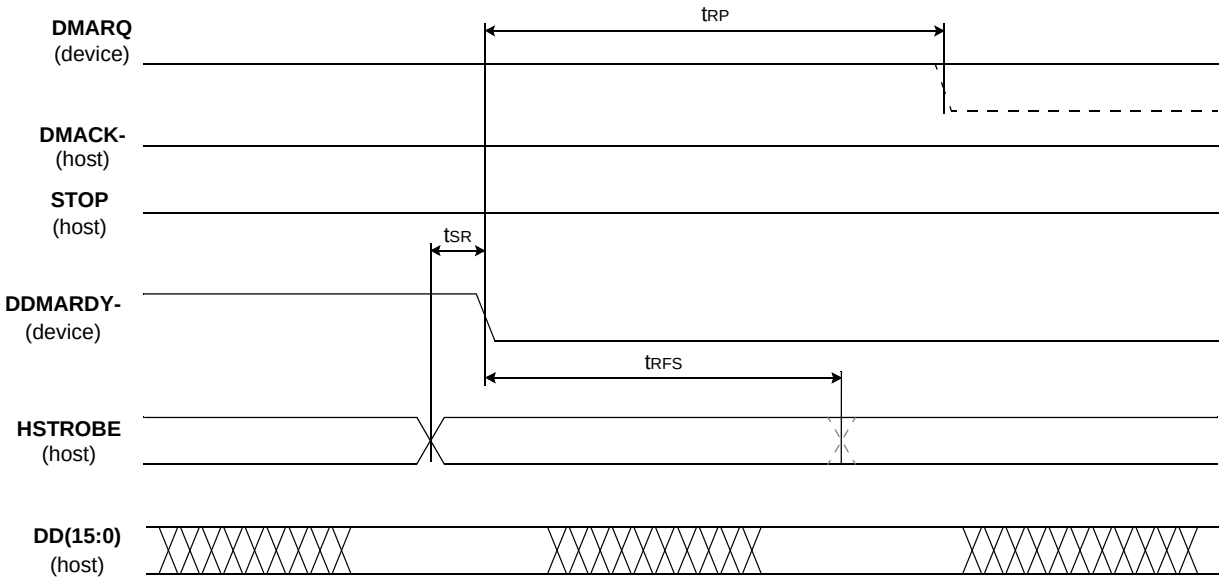


Figure 14. Device pausing an Ultra DMA data-out burst

NOTE:
1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner that t_{RP} after DDMARDY- is negated.
2. If the t_{SR} timing is not satisfied, the device may receive zero,one,or two more data words from the host.

4.5.4.9 Host terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

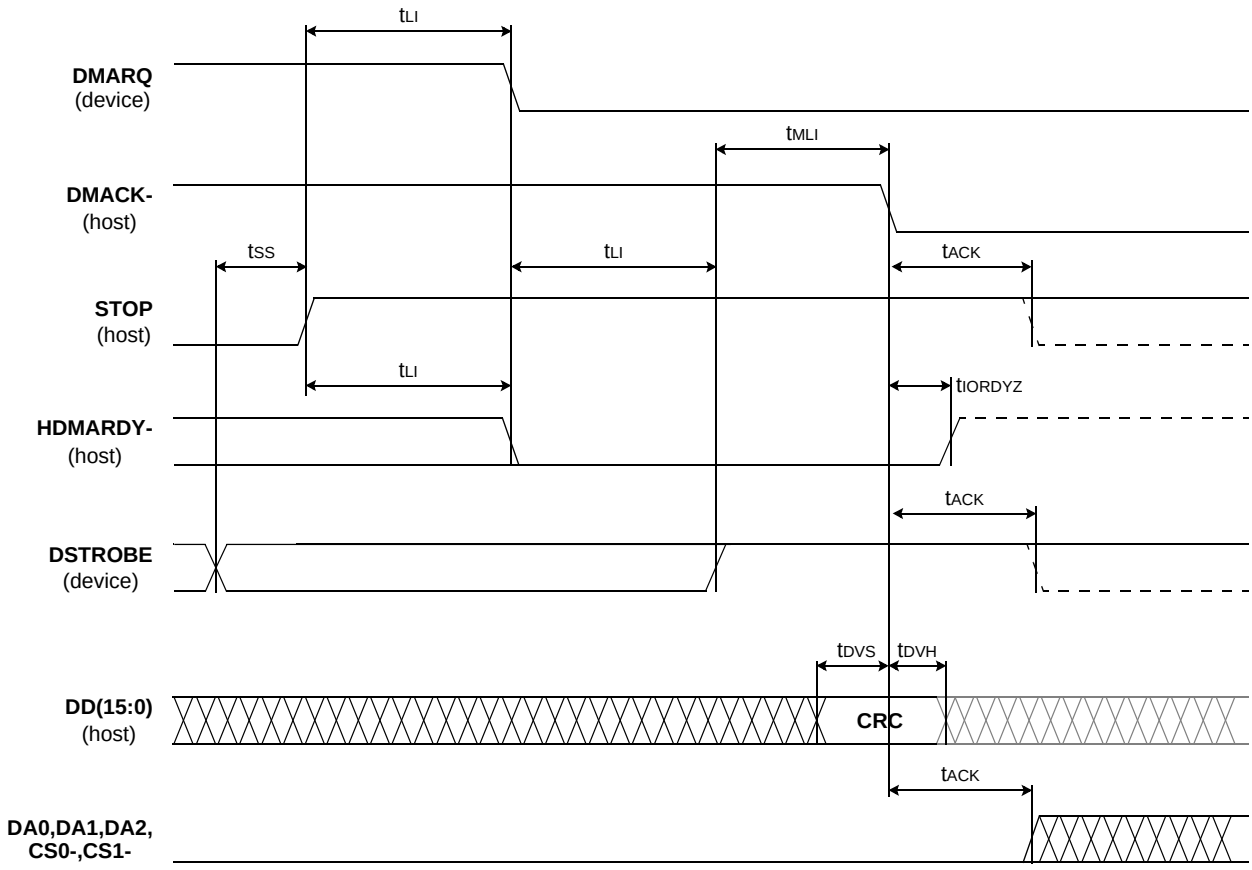


Figure 15. Host terminating an Ultra DMA data-out burst

NOTE:
1. The definitions for the DIOW-:STOP,IORDY:DDMARDY-:DSTROBE and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

4.5.4.10 Device terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 4.4.4

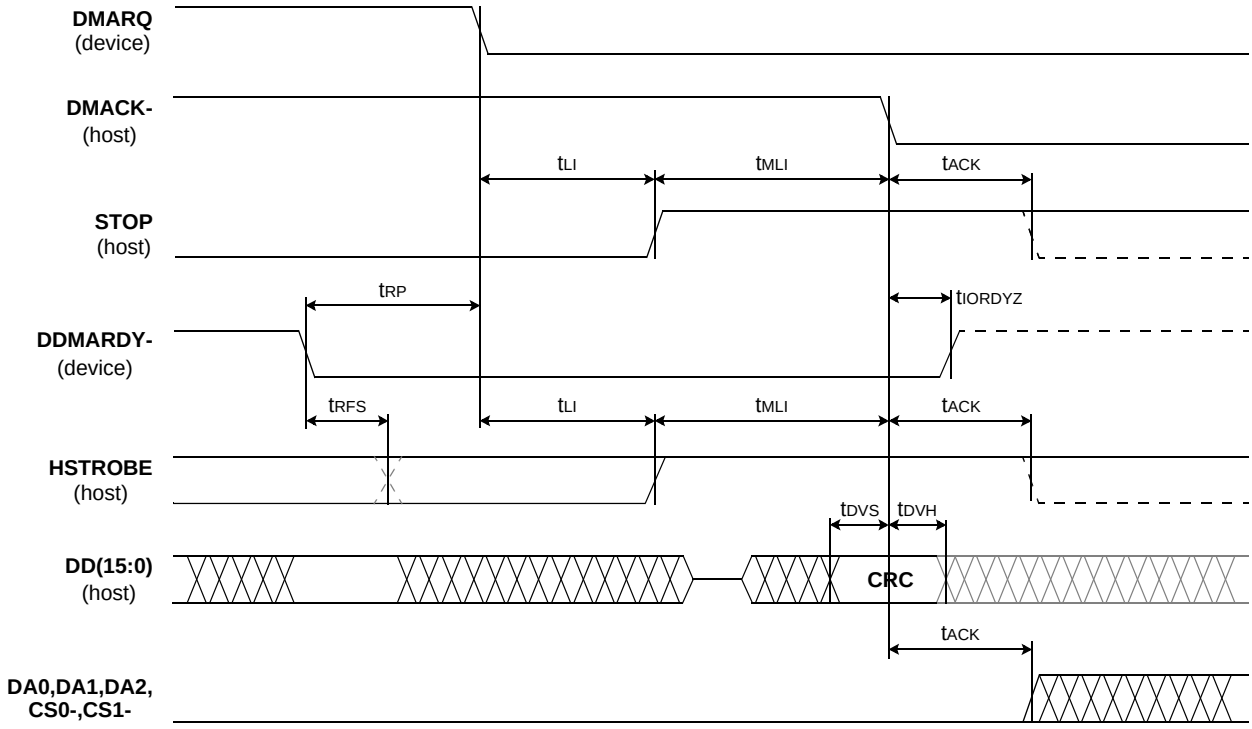


Figure 16. Device terminating an Ultra DMA data-out burst

NOTE:
1. The definitions for the DIOW-:STOP,IORDY:DDMARDY-:DSTROBE and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

5. ATA Registers

5.1 I/O Register Descriptions

Communication to or from the device is through registers addressed by the signals from the host(CS0-,CS1-, DA(2:0), DIOR-, and DIOW), CS0- and CS1- both asserted or negated is an invalid (not used) address except when both are negated during a DMA data transfer. When CS0- and CS1- are both asserted or both negated and a DMA transfer is not in progress, the device shall hold DD (15:0) in the released state and ignore transitions on DIOR- and DIOW-. When CS0- is negated and CS1- is asserted only DA (2:0) with a value of 6th is valid. During invalid combinations of assertion and negation of CS0-, CS1-, DA0, DA1, and DA2, a device shall keep DD(15:0) in the high impedance state and ignore transitions on DIOR- and DIOW-. Valid register addresses are described in the clauses defining the registers.

Address - the CS and DA address of the register.
Direction - indicates if the register is read/write, read only, or write only from the host.
Access restrictions - indicates when the register may be accessed.
Effect - indicates the effect of accessing the register.
Functional description - describes the function of the register.
Field/bit description - describes the content of the register.

5.2 Alternate Status Register

5.2.1 Address

CS1	CS0	DA2	DA1	DA0
A	N	A	A	N
A=asserted, N=negated				

5.2.2 Direction

This register is read only. If this address is written to by the host, the Device Control register is written.

5.2.3 Access Restrictions

When the BSY bit is set to one, the other bits in this register shall not be used. The entire contents of this register are not valid while the device is in Sleep mode.

5.2.4. Effect

Reading this register shall not clear a pending interrupt.

5.2.5 Functional Description

This register contains the same information as the Status register in the command block.

5.3 Command Register

5.3.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	A	N
A=asserted, N=negated				

5.3.2 Direction

This register is write only. If this address is read by the host, the Status register is read.

5.3.3 Access Restrictions

For all commands, this register shall only be written when BSY and DRQ are both cleared to zero and DMACK- is not asserted. If written when BSY or DRQ is set to one, the results of writing the Command register are indeterminate.

5.3.4 Effect

Command prcessing begins when this register is writte. The content of the Command Blcok registers become parameters of the command when this register is written. Writing this register clears any pending interrupt condition.

5.3.5 Functional description

This register contains the command code being sent to the device. Command execution begins immediately after this register is written.

5.3.6 Field/bit description

7	6	5	4	3	2	1	0
Command Code							

5.4 Cylinder High Register

5.4.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	N	A
A=asserted, N=negated				

5.4.2 Direction

This register is read/write.

5.4.3 Access Restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is noet asserted.
The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

5.4.4 Effect

The content of this register becomes a command parameter when the Comand register is written.

5.4.5 Functional description

The content of this register is command dependent

5.5 Cylinder Low Register

5.5.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	N	N
A=asserted, N=negated				

5.5.2 Direction

This register is read/write.

5.5.3 Access Restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted.
The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

5.5.4 Effect

The content of this register becomes a command parameter when the Command register is written.

5.5.5 Functional description

The content of this register is command dependent

5.6 Data Port

5.6.1 Address

When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16-bits wide.

CS1	CS0	DA2	DA1	DA0
N	N	X	X	X
A=asserted, N=negated, X=don't care				

5.6.2 Direction

This register is read/write.

5.6.3 Access Restrictions

This port shall be accessed for host DMA data transfers only when DMACK- and DMARQ are asserted.

5.6.4 Effect

The content of this register becomes a command parameter when the Command register is written. DMA out data transfers are processed by a series of reads to this port, each read transferring the data that follows the previous read. DMA in data transfers are processed by a series of writes to this port, each write transferring the data that follows the previous write. The results of a read during a DMA in or a write during a DMA out are indeterminate.

5.6.5 Functional description

The data port is 16-bits in width.

5.6.6 Field / bit description

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

5.7 Data Register

5.7.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	N	N
A=asserted, N=negated				

5.7.2 Direction

This register is read/write.

5.7.3 Access Restrictions

This register shall be accessed for host PIO data transfer only when DRQ is set to on and DMACK- is not asserted.
The contents of this register are not valid while a device is in the Sleep mode.

5.7.4 Effect

PIO out data transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO in data transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a PIO in or a write during a PIO out are indeterminate.

5.7.5 Functional description

The data port is 16-bits in width. When a CFA device is in 8-bit PIO data transfer mode this register is 8-bits wide using only DD7 to DD0.

5.7.6 Field / bit description

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

5.8 Device Control Register

5.8.1 Address

CS1	CS0	DA2	DA1	DA0
A	N	A	A	N
A=asserted, N=negated				

5.8.2 Direction

This register is write only. If this address is read by the host, the Alternate Status register is read.

5.8.3 Access Restrictions

This register shall only be written when DMACK- is not asserted.

5.8.4 Effect

The content of this register shall take effect when written.

5.8.5 Functional description

This register allows a host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When the Device Control Register is written, both devices respond to the write regardless of which device is selected. When the SRST bit is set to one, both devices shall perform the software reset protocol.
The device shall respond to the SRST bit when in the SLEEP mode.

5.8.6 Field / bit description

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved.
- SRST is the host software reset bit.
- nIEN is the enable bit for the device Assertion of INTRQ to the host. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer and shall be asserted or negated by the device as appropriate. When the nIEN bit is set to one, or the device is not selected, the INTRQ signal shall be in a high impedance state.
- Bit 0 shall be cleared to zero.

5.9 Device / Head Register

5.9.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	A	N
A=asserted, N=negated				

5.9.2 Direction

This register is read/write.

5.9.3 Access Restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted.
The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate.

5.9.4 Effect

The DEV bit becomes effective when this register is written by the host or the signature is set by the device. All other bits in this register become a command parameter when the Command register is written.

5.9.5 Functional description

But 4, DEV, in this register selects the device. Other bits in this register are command dependent.

5.9.6 Field / bit description

The content of this register shall take effect when written.

7	6	5	4	3	2	1	0
Obsolete	#	Obsolete	DEV	#	#	#	#

NOTE:
Some hosts set these bits to one. Devices shall ignore these bits.

- Obsolete:These bits are obsolete.
- #:The content of these bits is command dependent
- DEV: Device select. Cleared to zero selects Device 0. Set to one selects Device1.

5.10 Error Register

5.10.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	N	A
A=asserted, N=negated				

5.10.2 Direction

This register is read only. If this address is written to by the host, the Features register is written.

5.10.3 Access Restrictions

The contents of this register shall be valid when BSY and DRQ equal zero and ERR equals one.
The contents of this register shall be valid upon completion of power-on, or after a hardware or software reset, or after command completion of an EXECUTE DEVICE DIAGNOSTICS. The contents of this register are not valid while a devcie is in the Sleep mode.

5.10.4 Effect

None.

5.10.5 Functional description

This register contains status for the current command.
Following a power-on, a hardware or software reset, or command completion of an EXECUTE DEVICE DIAGNOSTIC, this register contains a diagnostic code. At command description of any command except EXECUTE DEVICE DIAGNOSTIC, the contents of this register are valid when the ERR bit is set to one in the Status Register.

5.10.6 Field / bit description

7	6	5	4	3	2	1	0
#	#	#	#	#	ABRT	#	#

• Bit 2: ABRT(command aborted) is set to one to indicate the requested command has been command aborted because the command code or a command parameter is invalid or some other error has occurred.
•#: The content of this bit is command dependent

5.11 Features Register

5.11.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	N	A
A=asserted, N=negated				

5.11.2 Direction

This register is write only. If this address is read by the host, the Error register is read.

5.11.3 Access Restrictions

This register shall be written only when BSY and DRQ equal zero and DMACK- is not asserted. If this register is written when BSY or DRQ is set to one, the result is indeterminate.

5.11.4 Effect

The content of this register becomes a command parameter when the Command register is written.

5.11.5 Functional description

The content of this register is command dependent.

5.12 Sector Count Register

5.12.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	A	N
A=asserted, N=negated				

5.12.2 Direction

This register is read/write.

5.12.3 Access Restrictions

This register shall be written only when BSY and DRQ equal zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of the this register are not valid while a device is in the Sleep mode.

5.12.4 Effect

The content of this register becomes a command parameter when the Command register is written.

5.12.5 Functional description

The content of this register is command dependent.

5.13 Sector Number Register

5.13.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	N	A	A
A=asserted, N=negated				

5.13.2 Direction

This register is read/write.

5.13.3 Access Restrictions

This register shall be written only when BSY and DRQ equal zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of the this register are not valid while a device is in the Sleep mode.

5.13.4 Effect

The content of this register becomes a command parameter when the Command register is written.

5.13.5 Functional description

The content of this register is command dependent.

5.14 Status Register

5.14.1 Address

CS1	CS0	DA2	DA1	DA0
N	A	A	A	A
A=asserted, N=negated				

5.14.2 Direction

This register is read only. If this address is written to by the host, the Command register is written.

5.14.3 Access Restrictions

The contents of this register, except for BSY, shall be ignored when BSY is set to one. BSY is valid at all times. The contents of this register are not valid while a device is in the Sleep mode.

5.14.4 Effect

Reading this register when an interrupt is pending causes the interrupt pending to be cleared. The host should not read the Status Register when an interrupt is expected as this may clear the interrupt pending before the INTRQ can be recognized by the host.

5.14.5 Functional description

The register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device.

5.14.6 Field / bit description

7	6	5	4	3	2	1	0
BSY	DRDY	#	#	DRQ	Obsolete	Obsolete	ERR

5.14.6.1 BSY(Busy)

BSY is set to one to indicate that device is busy. After the host has written the Command Register the device shall have either the BSY bit set to one, or the DRQ bit set to one, until command completion or the device has performed a bus release for an overlapped command.

The BSY bit shall be set to one by the device :
1) after either the negation of RESET- or the setting of the SRST bit to one in the Device Control Regitster;
2) after writing the Command Register if the DRQ bit is not set to one;
3) between blocks of a data transfer during PIO data-in commands before the DRQ bit is cleared to zero;
4) After the transfer of a data block during PIO data-out commands before the DRQ bit is cleared to zero;
5) during the data transfer of DMA commands either the BSY bit, the DRQ bit, or both shall be set to one;

NOTE:
The BSY bit may be set to one and then cleared to zero so quickly, that host detection of the BSY bit being set to one is not certain.

When BSY is set to one, the device has control of the Command Block Registers and;
1) a write to a Command Block Register by the host shall be ignored by the device except for writing DEVICE
RESET command;
2) a read from a Command Block register by the host will most likely yield invalid contents except for the BSY bit itself.

The BSY bit shall be cleared to zero by the device:
1)after setting DRQ to one to indicate is ready to transfer data;
2) at command completion;
3) upon releasing the bus for an overlapped command;
4) when the device is ready to accept commands that do not require DRDY during a power on, hardware or software reset.

When BSY is cleared to zero, the host has control of the Command Block registers, the device shall:
1) not set DRQ to one;
2) not change ERR bit;
3) not change the content of any other Command Block Register;
4) set the SERV bit to one when ready to continue an overlapped command that has been bus released.

5.14.6.2 DRDY(Device ready)

The DRDY bit shall be set to one by the device :
1) when the device is capable of accepting all commands for devices

When the DRDY bit is set to one :
1) the device shall accept and attempt to execute all implemented commands;
2) devices that implement the Power Management feature set shall maintain the DRDY bit set to one when they are in the Idle or Standby modes.

5.14.6.3 Command dependent

The use of bits marked with # are command dependent. Bit 4 was formerly the DSC(Device Seek Complete) bit.

5.14.6.4 DRQ(Data request)

DRQ indicates that the device is ready to transfer a word of data between the host and the device. After the host has written the Command Register the device shall either set the BSY bit to one or the DRQ bit to one, until command completion or the device has performed a bus release for an overlapped command.

The DRQ bit shall be set to one by the device :
1) when BSY is set to one and data is ready for PIO transfer;
2) during the data transfer of DMA commands either the BSY bit, the DRQ bit, or both shall be set to one.

When the DRQ bit is set to one, the host may :
1) transfer data via PIO mode;
2) transfer data via DMA mode if DMARQ and DMACK- are asserted.

The DRQ bit shall be cleared to zero, the host may :
1) transfer data via DMA mode if DMARQ and DMACK- are asserted and BSY is set to one.

5.14.6.5 Obsolete bits

Some bits in this register were defined in previous ATA standards but have been declared obsolete in this spec
These bits are labeled "obsolete".

5.14.6.6 ERR(Error)

ERR indicates that an error occurred during execution of the previous command.

The ERR bit shall be set to one by the device :
1) when BSY or DRQ is set to one and an error occurs in the executing command.

When the ERR bit is set to one :
1) the bits in the Error register shall be valid;
2) the device shall not change the contents of the following registers until a new command has been accepted, the SRST bit is set to one or RESET- is asserted :

- Error Register
- Cylinder High/Low Register
- Sector Count Register
- Sector Number Register
- Device / Head Register

The ERR bit shall be cleared to zero by the device :
1) when a new command is written to the Command Register;
2) when the SRST bit is set to one;
3) when the RESET- signal is asserted.

When the ERR bit is cleared to zero at the end of a command:
1) the content of the Error Register shall be ignored by the host.

6. Command Descriptions

6.1 Supporting ATA Command Set

Command Name	Command Code	Command Name	Command Code
RECALIBRATE	10h	IDLE	E3h
READ SECTOR(S)	20h	READ BUFFER	E4h
WRITE SECTOR(S)	30h	CHECK POWER MODE	E5h
READ VERIFY SECTOR(S)	40h	SLEEP	E6h
SEEK	70h	FLUSH CACHE	E7h
EXECUTE DEVICE DIAGNOSTIC	90h	WRITE BUFFER	E8h
INITIALIZE DEVICE PARAMETERS	91h	IDENTIFY DEVICE	ECh
SMART*1	B0h	SET FEATURES*2	EFh
READ MULTIPLE	C4h	SECURITY SET PASSWORD	F1h
WRITE MULTIPLE	C5h	SECURITY UNLOCK	F2h
SET MULTIPLE MODE	C6h	SECURITY ERASE PREPARE	F3h
READ DMA	C8h	SECURITY ERASE UNIT	F4h
WRITE DMA	CAh	SECURITY FREEZE LOCK	F5h
STANDBY IMMEDIATE	E0h	SECURITY DISABLE PASSWORD	F6h
IDLE IMMEDIATE	E1h	READ NATIVE MAX ADDRESS	F8h
STANBY	E2h	SET MAX*3	F9h

*1 : Refer to 6.3.1

*2 : Refer to 6.5.1

*3 : Refer to 6.6.1

6.2 SECURITY FEATURE Set

The Security mode features allow the host to implement a securtity password system to prevent unauthorized access to the disk drive.

6.2.1 SECURITY mode default setting

The NSSD is shipped with master password set to 20h value(ASCII blanks) and the lock function disabled.
The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enableing the lock function.

6.2.2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on

6.2.3 SECURITY mode operation from power-on

In locked mode, the NSSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

6.2.4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data.
However, the drive can be unlocked using the master password.

If the user password is lost and Maxium security level is set, it is impossible to access data.
However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

The execution time of SECURITY ERASE UNIT command is shown below.
- 32GB NSSD : 60 seconds
- 16GB NSSD : 30 seconds

6.3 SMART FEATURE Set

6.3.1 Sub Command Set

SMART			
READ DATA	D0h	READ LOG	D5h
READ ATTRIBUTE THRESHOLDS	D1h	ENABLE OPERATIONS	D8h
ENABLE/DISABLE AUTOSAVE	D2h	DISABLE OPERATIONS	D9h
SAVE ATTRIBUTE VALUES	D3h	RETURN STATUS	DAh
EXECUTE OFF-LINE IMMIDIATE	D4h	CHANGE THRESHOLD SECTOR SIZE	E0h

6.3.2 SMART Data Structure(READ DATA(D0h))

Byte	F/V	Descriptions
0~1	X	Revision code
2~3	X	Valid Information Count
4~7	V	Total number of sectors for replacement
8~11	V	Number of sectors actually replaced
12~15	X	Number of sectors initially mapped out
16~19	V	Threshold sector size [default value :19000h(50MB)]
19~361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364~365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time(in minutes)
373	F	Extended self-test routine recommended polling time(in minutes)
374-385	R	Reserved
386-510	X	Vendor specific
511	V	Data structure checksum

Key :
F=the content of the byte is fixed and does not change.
V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.
X=the content of the byte is vendor specific and may be fixed or variable.
R=the content of the byte is reserved and shall be zero.

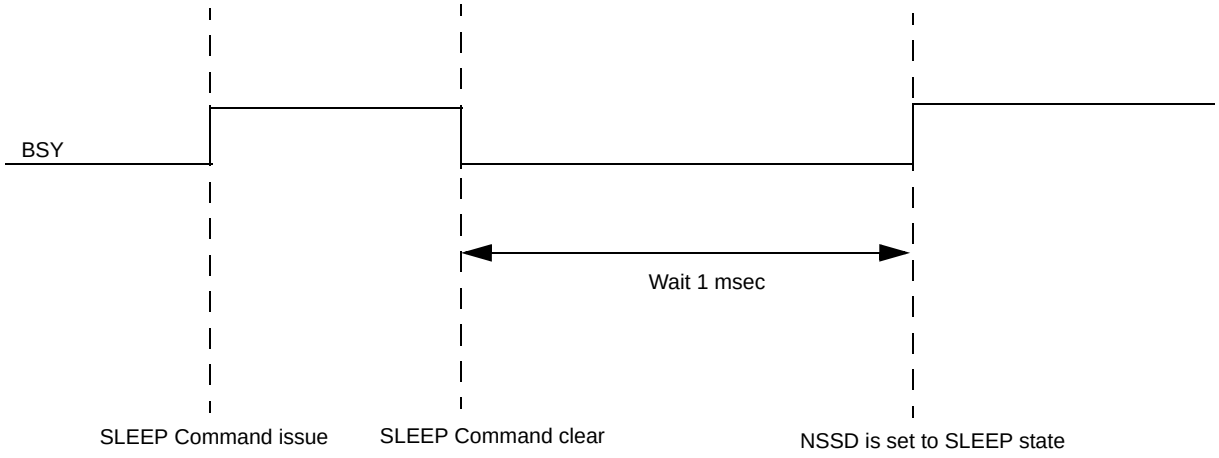
6.3.3 Threshold Sector Size

Threshold Sector Size is an predefined value that makes the waring message if the number of reserved sector size is below this value. The status can be read from Cylinder Register by READ DATA(D0h) command.
Deafult value of the Cylinder Register has C24Fh, but if the number of reserved sector size is below the Treshold Sector Size, the Cylinder Register has 2CF4h.
In order to change the Threshold Sector Size, should be set the changed value in Sector Count Register with CHANGE THRESHOLD SECTOR SIZE (E0h) command.

※ Sector Count Register value (unit : MB, Range : 0~199)

6.4 BSY Status in SLEEP Command

In SLEEP command, NSSD takes 1ms to get into SLEEP state.
During this period, all the command operation is prohibitted.
The status Register value is D0h after getting into SLEEP state.



6.5 SET FEATURES

6.5.1 SET FEATURES Register Value

SET FEATURES	
ENABLE WRITE CACHE	02h
SET TRANSFER MODE	03h
DISABLE WRITE CACHE	82h

Default settings after power on are Data transfer mode of Ultra DMA mode 4, PIO mode 4 and write cache enabled.

6.6 SET MAX

6.6.1 SET MAX FEATURES Register Value

Each of SET MAX commands is identified by the value placed in the Feature register.
Below table shows these Features register values.

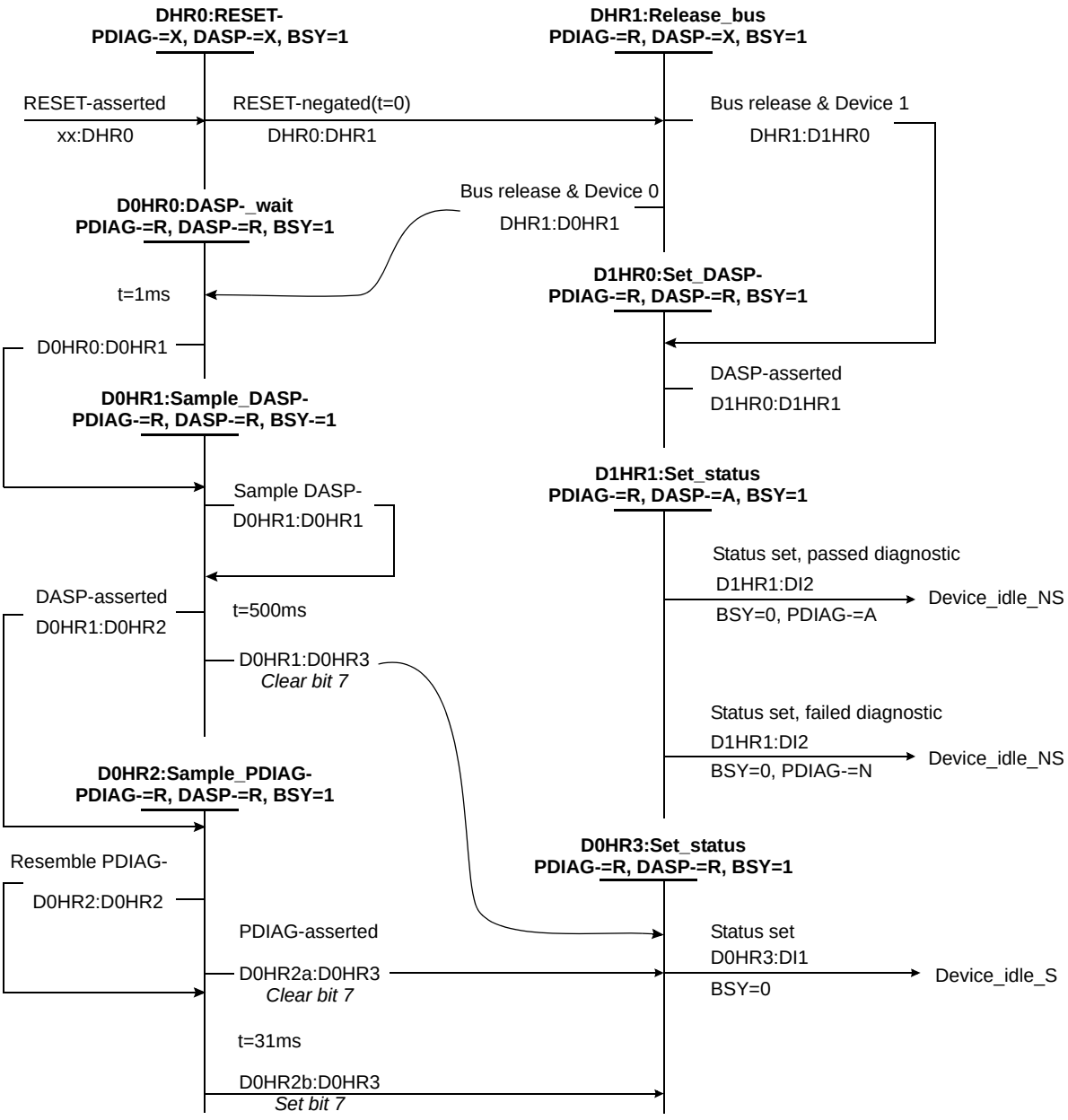
SET MAX	
SET MAX ADDRESS	01h
SET MAX SET PASSWORD	02h
SET MAX LOCK	03h
SET MAX FREEZE LOCK	04h
SET MAX UNLOCK	05h

6.7 Identify Device Data

Word	16GB	32GB	Description
0	0x0040	0x0040	General information
1	0x3FFF	0x3FFF	Number of logical cylinders
2	0x0000	0x0000	Specific configuration
3	0x0010	0x0010	Number of logical heads
4 - 5	0x0000	0x0000	Retired
6	0x003F	0x003F	Number of logical sectors per logical track
7 - 8	0x0000	0x0000	Reserved
9	0x0000	0x0000	Retired
10 -19	0xXXXX	0xXXXX	Serial number(20 ASCII characters)
20 - 21	0x0000	0x0000	Retired
22	0x0000	0x0000	Obsolete
23 - 26	0xXXXX	0xXXXX	Firmware revision(8 ASCII characters)
27- 46	0xXXXX	0xXXXX	Model number
47	0x8010	0x8010	Number of sectors on multiple commands
48	0x0000	0x0000	Reserved
49	0x2B00	0x2B00	Capabilities
50	0x4000	0x4000	Capabilities
51 - 52	0x0000	0x0000	Obsolete
53	0x0007	0x0007	Reserved
54	0x3FFF	0x3FFF	Number of current logical cylinders
55	0x0010	0x0010	Number of current logical heads
56	0x003F	0x003F	Number of current logical sectors per track
57	0xFC10	0xFC10	Current capacity in sectors
58	0x00FB	0x00FB	
59	0x0110	0x0110	Multiple sector setting
60	0x0000	0x0000	Total number of user addressable sectors(LBA mode only)
61	0x01E8	0x03D0	
62	0x0000	0x0000	Obsolete
63	0x0007	0x0007	Multi-word DMA transfer
64	0x0003	0x0003	Flow control PIO transfer modes supported
65	0x0078	0x0078	Minimum Multiword DMA transfer cycle time per word
66	0x0078	0x0078	Manufacturer's recommended Multiword DMA transfer cycle time per word
67	0x00F0	0x00F0	Minimum PIO transfer cycle time without flow control
68	0x0078	0x0078	Minimum PIO transfer cycle time with IORDY flow control
69 - 74	0x0000	0x0000	Reserved
75	0x0000	0x0000	No DMA QUEUED command Supports
76 - 79	0x0000	0x0000	Reserved
80	0x003C	0x003C	ATA5 rev3
81	0x0013	0x0013	
82	0x342B	0x342B	Command set supported
83	0x4101	0x4101	Command set supported
84	0x4000	0x4000	Command set/feature supported extension
85	0x3428	0x3428	Command set/feature enabled
86	0x4101	0x4101	Command set/feature enabled
87	0x4000	0x4000	Command set/feature default
88	0x101F	0x101F	Ultra DMA transfer

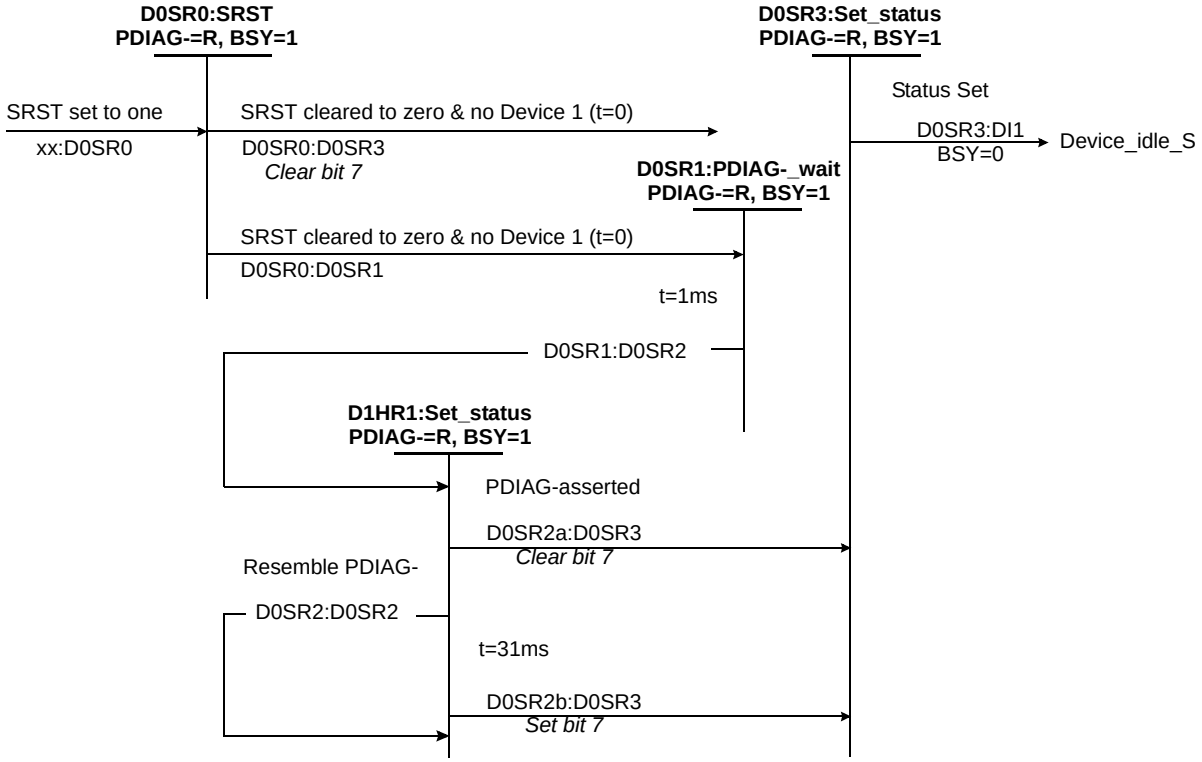
Word	16GB	32GB	Description
89 - 91	0x0000	0x0000	Reserved
92	0xFFFE	0XFFFE	Master Password Revision Code
93	0x2040	0x2040	Hardware reset result
94 - 126	0x0000	0x0000	Reserved
127	0x0000	0x0000	Removable Media Status Notification feature set support
128	0x0001	0x0001	Security status
129 - 159	0x0000	0x0000	Vendor specific
160 - 254	0x0000	0x0000	Reserved
255	0x0000	0x0000	Integrity word

6.8 Hardware Reset State Diagram



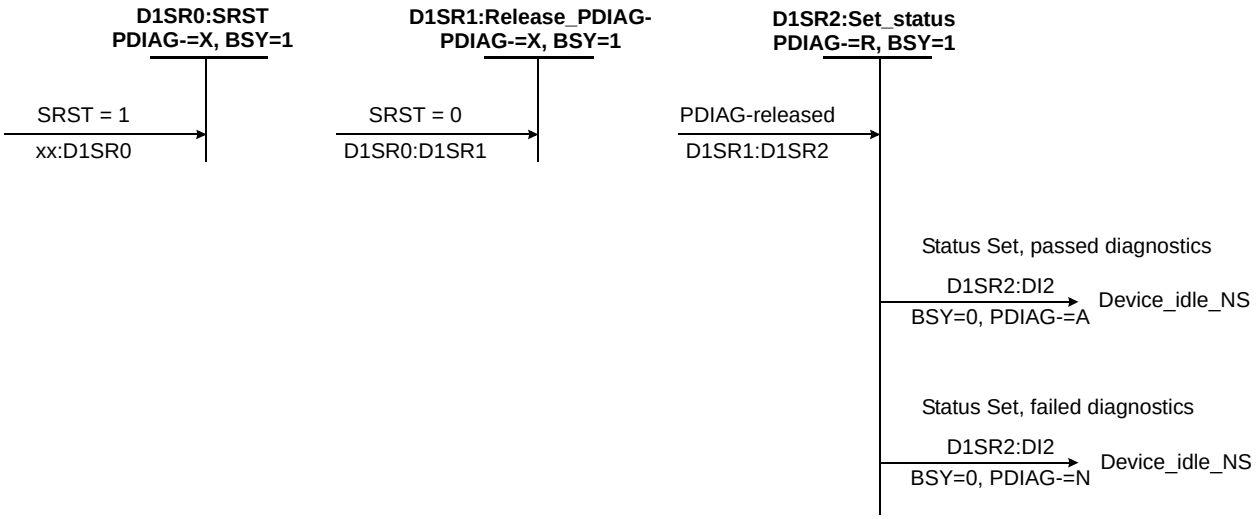
BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
V	0	0	0	0	0	R	R	V	V

6.9 Software Reset State Diagram



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
V	0	0	0	0	0	R	R	V	R

Device0 : software reset state diagram



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
V	0	0	0	0	0	R	R	V	R

Device 1 : software reset state diagram

7. Ordering Information

M C X X X X X X X X X X - X X X X X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Module: M

2. Card: C

3~4. Flash Density

4G : 4G
8D: 8G DDP
AQ : 16G QDP
BO : 32G(16G QDP*2)

5. Feature

E : NSSD

6~8. NSSD Density

04G : 4G Byte
08G : 8G byte
16G : 16G Byte
32G : 32G Byte

9. NSSD Type

6 : NSSD Type1(56x48)
Q : NSSD Type2(54x71)

10. Component Generation

M : 1st Generation
A : 2nd Generation
B : 3rd Generation
C : 4th Generation
D : 5th Generation

11. Flash Package

P : TSOP1(LF)

12. PCB Revision AND Production Site

P : None(STS)
Q : 1st Rev.(STS)
R : 2nd Rev.(STS)

13. " - "

14. Packing Type

M : Module Type

15. Controller

X : S4LD166X01(LQFP)
W : S4LD166X01(FBGA)

16. Controller Firmware Revision

A : None
B : 1st Rev.
C : 2nd Rev.
D : 3rd Rev.
Z : None(No Cont.)

17 ~ 18. Customer Grade

" Customer List Reference "

8. Product Line-up

M-die Based

Part Number	Density	Type	Remark
MCAQE16G6MPP-MXA	16GB	Small	
MCBOE32GQMPQ-MWA	32GB	Slim	

A-die Based

Part Number	Density	Type	Remark
MC8DE08G6APP-MXA	08GB	Small	
MCAQE16G6APP-MXA	16GB	Small	
MCBOE32GQAPQ-MWA	32GB	Slim	
MC4GE04GQAPR-MWA	4GB	Slim	Will be available end of 2006 year. R code(12th) means shared PCB.
MC8DE08GQAPR-MWA	8GB	Slim	
MCAQE16GQAPR-MWA	16GB	Slim	
MCBOE32GQAPR-MWA	32GB	Slim	