

IS61NLP25672/IS61NVP25672 IS61NLP51236/IS61NVP51236 IS61NLP102418/IS61NVP102418



256K x 72, 512K x 36 and 1M x 18 18Mb, PIPELINE 'NO WAIT' STATE BUS SRAM

ADVANCE INFORMATION

DECEMBER 2002

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 119-ball PBGA, 165-ball PBGA and 209-ball (x72) PBGA packages
- Power supply:
NVP: $V_{\text{DD}} 2.5\text{V} (\pm 5\%), V_{\text{DDQ}} 2.5\text{V} (\pm 5\%)$
NLP: $V_{\text{DD}} 3.3\text{V} (\pm 5\%), V_{\text{DDQ}} 3.3\text{V}/2.5\text{V} (\pm 5\%)$
- JTAG Boundary Scan for PBGA packages
- Industrial temperature available

DESCRIPTION

The 18 Meg 'NLP/NVP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 256K words by 72 bits, 512K words by 36 bits and 1M words by 18 bits, fabricated with ISSI's advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{\text{CKE}}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{\text{WE}}$ is LOW. Separate byte enables allow individual bytes to be written.

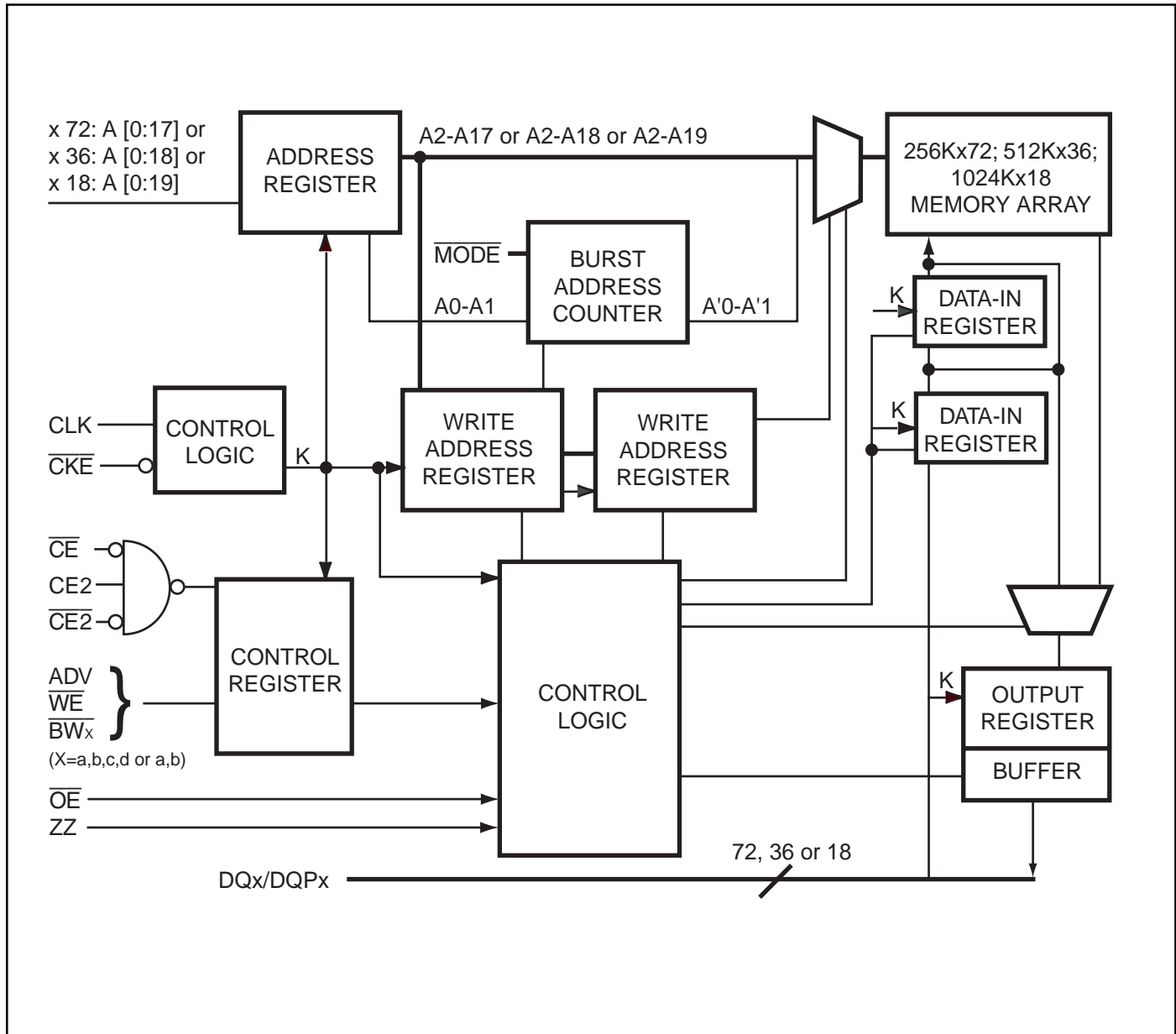
A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

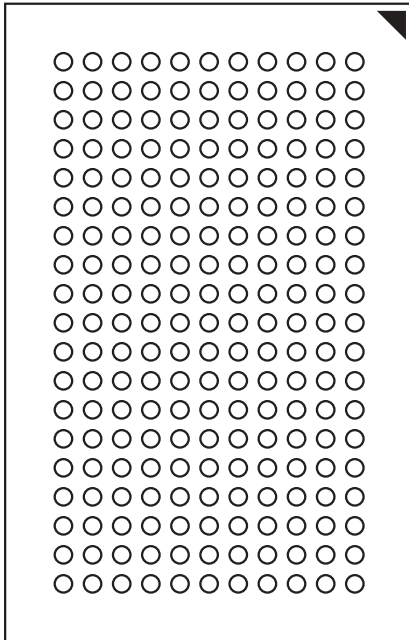
FAST ACCESS TIME

| Symbol | Parameter | -250 | -200 | Units |
|--------|-------------------|------|------|-------|
| tkQ | Clock Access Time | 2.6 | 3.1 | ns |
| tkC | Cycle Time | 4 | 5 | ns |
| | Frequency | 250 | 200 | MHz |

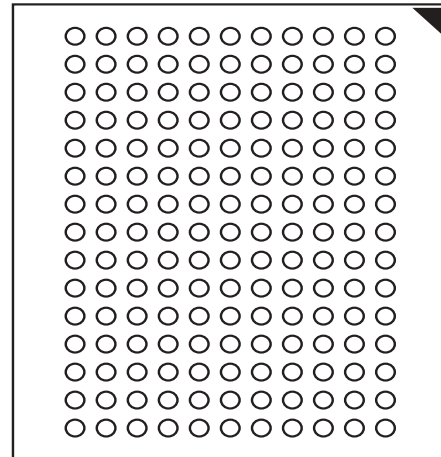
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BLOCK DIAGRAM

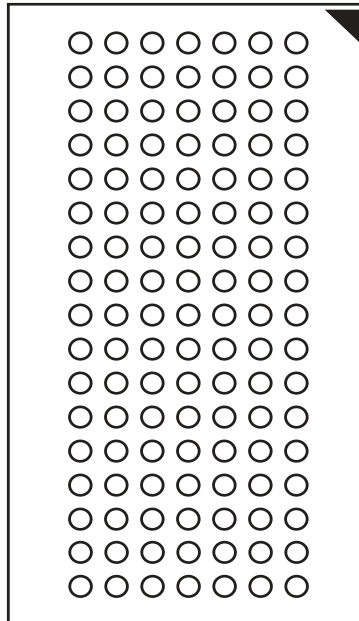




Bottom View
209-Ball, 14 mm x 22 mm BGA
1 mm Ball Pitch, 11 x 19 Ball Array



Bottom View
165-Ball, 13 mm x 15mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array



Bottom View
119-Ball, 14 mm x 22 mm BGA
1 mm Ball Pitch, 7 x 17 Ball Array

PIN CONFIGURATION — 256K X 72, 209-Ball PBGA (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|------|------------------|------------------|-----|------------------|-----|------------------|------------------|------|------|
| A | DQg | DQg | A | CE2 | A | ADV | A | $\overline{CE2}$ | A | DQb | DQb |
| B | DQg | DQg | \overline{BWc} | \overline{BWg} | NC | \overline{WE} | A | \overline{BWb} | \overline{BWf} | DQb | DQb |
| C | DQg | DQg | \overline{BWh} | \overline{BWd} | NC | \overline{CE} | NC | \overline{BWe} | \overline{BWa} | DQb | DQb |
| D | DQg | DQg | VSS | NC | NC | \overline{OE} | NC | NC | VSS | DQb | DQb |
| E | DQPg | DQpc | VDDQ | VDDQ | VDD | VDD | VDD | VDDQ | VDDQ | DQPf | DQPb |
| F | DQc | DQc | VSS | VSS | VSS | NC | VSS | VSS | VSS | DQf | DQf |
| G | DQc | DQc | VDDQ | VDDQ | VDD | NC | VDD | VDDQ | VDDQ | DQf | DQf |
| H | DQc | DQc | VSS | VSS | VSS | NC | VSS | VSS | VSS | DQf | DQf |
| J | DQc | DQc | VDDQ | VDDQ | VDD | NC | VDD | VDDQ | VDDQ | DQf | DQf |
| K | NC | NC | CLK | NC | VSS | \overline{CKE} | VSS | NC | NC | NC | NC |
| L | DQh | DQh | VDDQ | VDDQ | VDD | NC | VDD | VDDQ | VDDQ | DQa | DQa |
| M | DQh | DQh | VSS | VSS | VSS | NC | VSS | VSS | VSS | DQa | DQa |
| N | DQh | DQh | VDDQ | VDDQ | VDD | NC | VDD | VDDQ | VDDQ | DQa | DQa |
| P | DQh | DQh | VSS | VSS | VSS | ZZ | VSS | VSS | VSS | DQa | DQa |
| R | DQPd | DQPh | VDDQ | VDDQ | VDD | VDD | VDD | VDDQ | VDDQ | DQPa | DQPe |
| T | DQd | DQd | VSS | NC | NC | MODE | NC | NC | VSS | DQe | DQe |
| U | DQd | DQd | NC | A | NC | A | NC | A | NC | DQe | DQe |
| V | DQd | DQd | A | A | A | A1 | A | A | A | DQe | DQe |
| W | DQd | DQd | TMS | TDI | A | A0 | A | TDO | TCK | DQe | DQe |

11 x 19 Ball BGA—14 x 22 mm² Body—1 mm Ball Pitch

PIN DESCRIPTIONS

| Symbol | Pin Name |
|--|---|
| A | Synchronous Address Inputs |
| A0, A1 | Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus. |
| ADV | Synchronous Burst Address Advance |
| \overline{BWa} - \overline{BWh} | Synchronous Byte Write Enable |
| \overline{CE} , $\overline{CE2}$, CE2 | Synchronous Chip Enable |
| CLK | Synchronous Clock |
| \overline{CKE} | Clock Enable |
| DQx | Synchronous Data Input/Output |
| DQPx | Parity Data I/O |

| | |
|----------------------|---|
| VSS | Ground |
| MODE | Burst Sequence Selection |
| \overline{OE} | Output Enable |
| TCK, TDI TDO, TMS | JTAG Pins |
| VDD | 3.3V/2.5V Power Supply |
| VDDQ | Isolated Output Buffer Supply: 3.3V/2.5V |
| \overline{WE} | Write Enable |
| ZZ | Snooze Enable |

PIN CONFIGURATION — 512K x 36, 165-Ball PBGA (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|-----------------|------------------|------------------|------------------|------------------|------------------|-----------------|------------------|-----|------|
| A | NC | A | \overline{CE} | \overline{BWc} | \overline{BWb} | $\overline{CE2}$ | \overline{CKE} | ADV | A | A | NC |
| B | NC | A | CE2 | \overline{BWd} | \overline{BWa} | CLK | \overline{WE} | \overline{OE} | A | A | NC |
| C | DQPc | NC | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | DQPb |
| D | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| E | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| F | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| G | DQc | DQc | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQb | DQb |
| H | NC | V _{DD} | NC | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | NC | NC | ZZ |
| J | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| K | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| L | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| M | DQd | DQd | V _{DDQ} | V _{DD} | V _{SS} | V _{SS} | V _{SS} | V _{DD} | V _{DDQ} | DQa | DQa |
| N | DQPd | NC | V _{DDQ} | V _{SS} | NC | NC | NC | V _{SS} | V _{DDQ} | NC | DQPd |
| P | NC | NC | A | A | TDI | A1* | TDO | A | A | A | NC |
| R | MODE | NC | A | A | TMS | A0* | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|--------------------------|--|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| \overline{WE} | Synchronous Read/Write Control Input |
| CLK | Synchronous Clock |
| \overline{CKE} | Clock Enable |
| \overline{CE} | Synchronous Chip Select |
| $\overline{CE2}$ | Synchronous Chip Select |
| CE2 | Synchronous Chip Select |
| \overline{BWx} (x=a-d) | Synchronous Byte Write Inputs |
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |

| | |
|----------------------|---|
| MODE | Burst Sequence Selection |
| TCK, TDI TDO, TMS | JTAG Pins |
| V _{DD} | 3.3V/2.5V Power Supply |
| NC | No Connect |
| DQx | Data Inputs/Outputs |
| DQPx | Parity Data I/O |
| V _{DDQ} | Isolated output Power Supply 3.3V/2.5V |
| V _{SS} | Ground |

119-PIN PBGA PACKAGE CONFIGURATION— 512K x 36 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|------|------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| A | VDDQ | A | A | A | A | A | VDDQ |
| B | NC | CE2 | A | ADV | A | $\overline{\text{CE2}}$ | NC |
| C | NC | A | A | VDD | A | A | NC |
| D | DQc | DQPc | Vss | NC | Vss | DQPb | DQb |
| E | DQc | DQc | Vss | $\overline{\text{CE}}$ | Vss | DQb | DQb |
| F | VDDQ | DQc | Vss | $\overline{\text{OE}}$ | Vss | DQb | VDDQ |
| G | DQc | DQc | $\overline{\text{BWc}}$ | A | $\overline{\text{BWb}}$ | DQb | DQb |
| H | DQc | DQc | Vss | $\overline{\text{WE}}$ | Vss | DQb | DQb |
| J | VDDQ | VDD | NC | VDD | NC | VDD | VDDQ |
| K | DQd | DQd | Vss | CLK | Vss | DQa | DQa |
| L | DQd | DQd | $\overline{\text{BWd}}$ | NC | $\overline{\text{BWa}}$ | DQa | DQa |
| M | VDDQ | DQd | Vss | $\overline{\text{CKE}}$ | Vss | DQa | VDDQ |
| N | DQd | DQd | Vss | A1* | Vss | DQa | DQa |
| P | DQd | DQPd | Vss | A0* | Vss | DQPa | DQa |
| R | NC | A | MODE | VDD | NC | A | NC |
| T | NC | NC | A | A | A | NC | ZZ |
| U | VDDQ | TMS | TDI | TCK | TDO | NC | VDDQ |

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|---------------------------------|--|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| ADV | Synchronous Burst Address Advance/ Load |
| $\overline{\text{WE}}$ | Synchronous Read/Write Control Input |
| CLK | Synchronous Clock |
| $\overline{\text{CKE}}$ | Clock Enable |
| $\overline{\text{CE}}$ | Synchronous Chip Select |
| $\overline{\text{CE2}}$ | Synchronous Chip Select |
| CE2 | Synchronous Chip Select |
| $\overline{\text{BWx}}$ (x=a-d) | Synchronous Byte Write Inputs |

| | |
|------------------------|--------------------------|
| $\overline{\text{OE}}$ | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| TCK, TDO | JTAG Pins |
| TMS, TDI | |
| VDD | Power Supply |
| Vss | Ground |
| NC | No Connect |
| DQa-DQd | Data Inputs/Outputs |
| DQPa-Pd | Parity Data I/O |
| VDDQ | Output Power Supply |

165-PIN PBGA PACKAGE CONFIGURATION— 1024K x 18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------------------|-----------------|-----------------|-------------------|-------------------|-------------------|------------------|-----------------|------|-----------------|------------------|
| A | NC | A | \overline{CE} | \overline{BW}_b | NC | \overline{CE}_2 | \overline{CKE} | ADV | A | A | A |
| B | NC | A | CE2 | NC | \overline{BW}_a | CLK | \overline{WE} | \overline{OE} | A | A | NC |
| C | NC | NC | VDDQ | Vss | Vss | Vss | Vss | Vss | VDDQ | NC | DQP _a |
| D | NC | DQ _b | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | NC | DQ _a |
| E | NC | DQ _b | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | NC | DQ _a |
| F | NC | DQ _b | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | NC | DQ _a |
| G | NC | DQ _b | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | NC | DQ _a |
| H | NC | VDD | NC | VDD | Vss | Vss | Vss | VDD | NC | NC | ZZ |
| J | DQ _b | NC | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQ _a | NC |
| K | DQ _b | NC | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQ _a | NC |
| L | DQ _b | NC | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQ _a | NC |
| M | DQ _b | NC | VDDQ | VDD | Vss | Vss | Vss | VDD | VDDQ | DQ _a | NC |
| N | DQP _b | NC | VDDQ | Vss | NC | NC | NC | Vss | VDDQ | NC | NC |
| P | NC | NC | A | A | TDI | A ₁ * | TDO | A | A | A | NC |
| R | MODE | NC | A | A | TMS | A ₀ * | TCK | A | A | A | A |

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|---------------------------|--|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| ADV | Synchronous Burst Address Advance/Load |
| \overline{WE} | Synchronous Read/Write Control Input |
| CLK | Synchronous Clock |
| \overline{CKE} | Clock Enable |
| \overline{CE} | Synchronous Chip Select |
| \overline{CE}_2 | Synchronous Chip Select |
| CE2 | Synchronous Chip Select |
| \overline{BW}_x (x=a,b) | Synchronous Byte Write Inputs |
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |

| | |
|----------------------|---|
| MODE | Burst Sequence Selection |
| TCK, TDI TDO, TMS | JTAG Pins |
| VDD | 3.3V/2.5V Power Supply |
| NC | No Connect |
| DQ _x | Data Inputs/Outputs |
| DQP _x | Parity Data I/O |
| VDDQ | Isolated output Power Supply 3.3V/2.5V |
| Vss | Ground |

119-PIN PBGA PACKAGE CONFIGURATION— 1M x 18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|------|------|------------------|------------------|------------------|------------------|------|
| A | VDDQ | A | A | A | A | A | VDDQ |
| B | NC | CE2 | A | ADV | A | $\overline{CE}2$ | NC |
| C | NC | A | A | VDD | A | A | NC |
| D | DQb | NC | Vss | NC | Vss | DQPa | NC |
| E | NC | DQb | Vss | \overline{CE} | Vss | NC | DQa |
| F | VDDQ | NC | Vss | \overline{OE} | Vss | DQa | VDDQ |
| G | NC | DQb | $\overline{BW}b$ | A | Vss | NC | DQa |
| H | DQb | NC | Vss | \overline{WE} | Vss | DQa | NC |
| J | VDDQ | VDD | NC | VDD | NC | VDD | VDDQ |
| K | NC | DQb | Vss | CLK | Vss | NC | DQa |
| L | DQb | NC | Vss | NC | $\overline{BW}a$ | DQa | NC |
| M | VDDQ | DQb | Vss | \overline{CKE} | Vss | NC | VDDQ |
| N | DQb | NC | Vss | A1* | Vss | DQa | NC |
| P | NC | DQPb | Vss | A0* | Vss | NC | DQa |
| R | NC | A | MODE | VDD | NC | A | NC |
| T | NC | A | A | NC | A | A | ZZ |
| U | VDDQ | TMS | TDI | TCK | TDO | NC | VDDQ |

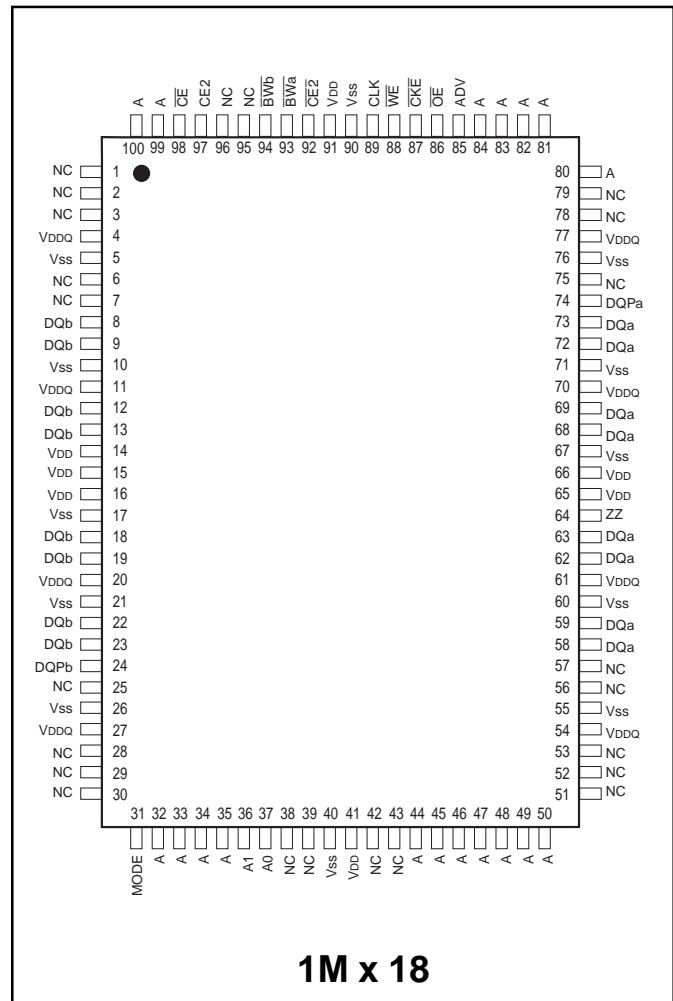
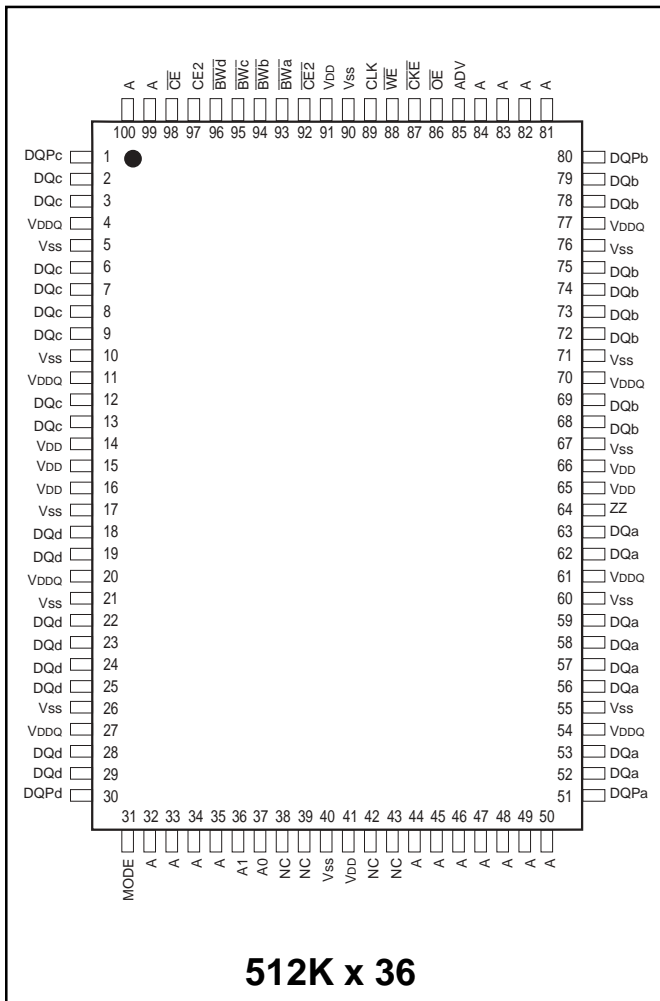
Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|--------------------------|--|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| ADV | Synchronous Burst Address Advance/ Load |
| \overline{WE} | Synchronous Read/Write Control Input |
| CLK | Synchronous Clock |
| \overline{CKE} | Clock Enable |
| \overline{CE} | Synchronous Chip Select |
| $\overline{CE}2$ | Synchronous Chip Select |
| CE2 | Synchronous Chip Select |
| $\overline{BW}x$ (x=a,b) | Synchronous Byte Write Inputs |

| | |
|-----------------|--------------------------|
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| TCK, TDO | JTAG Pins |
| TMS, TDI | |
| VDD | Power Supply |
| Vss | Ground |
| NC | No Connect |
| DQa-DQb | Data Inputs/Outputs |
| DQPa-Pb | Parity Data I/O |
| VDDQ | Output Power Supply |

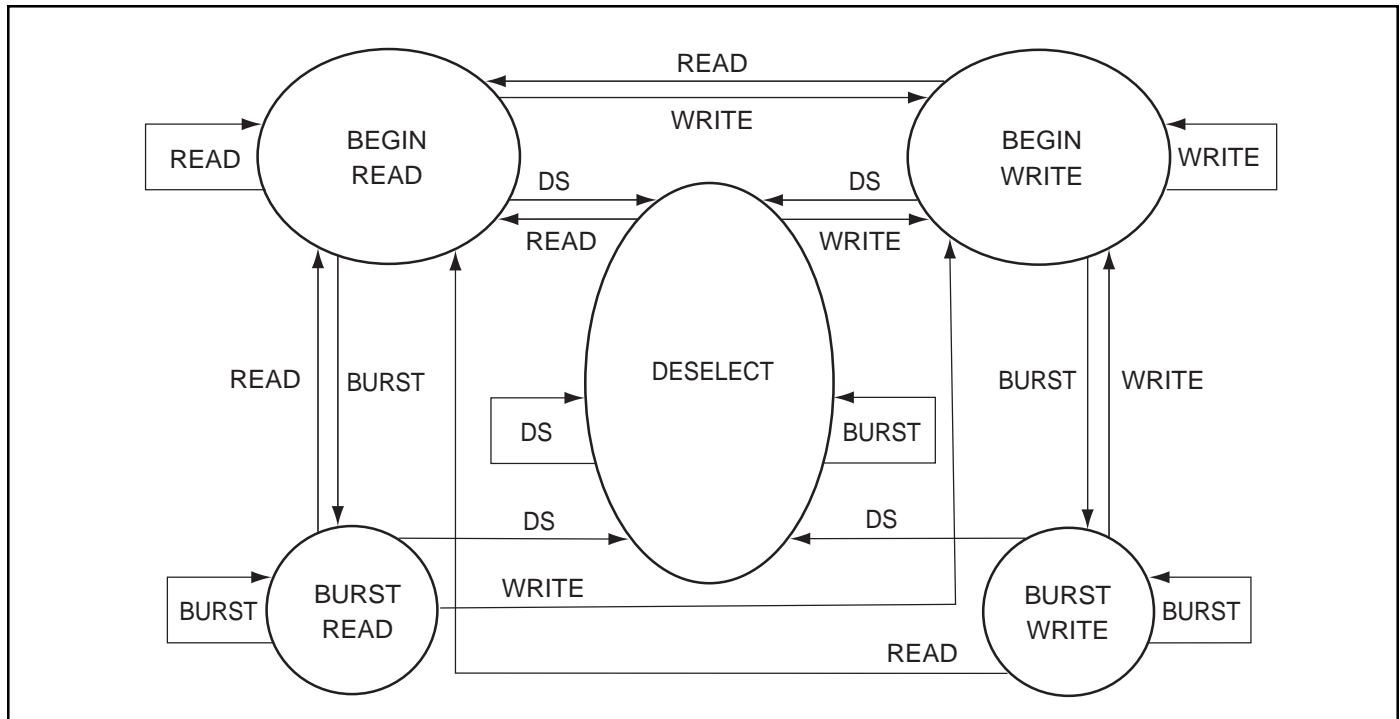
PIN CONFIGURATION
100-Pin TQFP



PIN DESCRIPTIONS

| | | | |
|-------------------------------------|---|--|---|
| A0, A1 | Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus. | \overline{CE} , $CE2$, $\overline{CE2}$ | Synchronous Chip Enable |
| A | Synchronous Address Inputs | \overline{OE} | Output Enable |
| CLK | Synchronous Clock | DQa-DQd | Synchronous Data Input/Output |
| ADV | Synchronous Burst Address Advance | DQPa-DQPd | Parity Data I/O |
| \overline{BWA} - \overline{BWD} | Synchronous Byte Write Enable | MODE | Burst Sequence Selection |
| \overline{WE} | Write Enable | VDD | +3.3V/2.5V Power Supply |
| \overline{CKE} | Clock Enable | VSS | Ground for output Buffer |
| VSS | Ground for Core | VDDQ | Isolated Output Buffer Supply: +3.3V/2.5V |
| NC | Not Connected | ZZ | Snooze Enable |

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE⁽¹⁾

| Operation | Address Used | \overline{CE} | CE2 | $\overline{CE2}$ | ADV | \overline{WE} | $\overline{BW_x}$ | \overline{OE} | \overline{CKE} | CLK |
|-----------------------|------------------|-----------------|-----|------------------|-----|-----------------|-------------------|-----------------|------------------|-----|
| Not Selected | N/A | H | X | X | L | X | X | X | L | ↑ |
| Not Selected | N/A | X | L | X | L | X | X | X | L | ↑ |
| Not Selected | N/A | X | X | H | L | X | X | X | L | ↑ |
| Not Selected Continue | N/A | X | X | X | H | X | X | X | L | ↑ |
| Begin Burst Read | External Address | L | H | L | L | H | X | L | L | ↑ |
| Continue Burst Read | Next Address | X | X | X | H | X | X | L | L | ↑ |
| NOP/Dummy Read | External Address | L | H | L | L | H | X | H | L | ↑ |
| Dummy Read | Next Address | X | X | X | H | X | X | H | L | ↑ |
| Begin Burst Write | External Address | L | H | L | L | L | L | X | L | ↑ |
| Continue Burst Write | Next Address | X | X | X | H | X | L | X | L | ↑ |
| NOP/Write Abort | N/A | L | H | L | L | L | H | X | L | ↑ |
| Write Abort | Next Address | X | X | X | H | X | H | X | L | ↑ |
| Ignore Clock | Current Address | X | X | X | X | X | X | X | H | ↑ |

Notes:

- "X" means don't care.
- The rising edge of clock is symbolized by ↑
- A continue deselect cycle can only be entered if a deselect cycle is executed first.
- $\overline{WE} = L$ means Write operation in Write Truth Table.
 $\overline{WE} = H$ means Read operation in Write Truth Table.
- Operation finally depends on status of asynchronous pins (\overline{ZZ} and \overline{OE}).

ASYNCHRONOUS TRUTH TABLE⁽¹⁾

| Operation | ZZ | \overline{OE} | I/O STATUS |
|------------|----|-----------------|-------------|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

| Operation | \overline{WE} | \overline{BWa} | \overline{BWb} |
|-----------------|-----------------|------------------|------------------|
| READ | H | X | X |
| WRITE BYTE a | L | L | H |
| WRITE BYTE b | L | H | L |
| WRITE ALL BYTES | L | L | L |
| WRITE ABORT/NOP | L | H | H |

Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

| Operation | \overline{WE} | \overline{BWa} | \overline{BWb} | \overline{BWc} | \overline{BWd} |
|-----------------|-----------------|------------------|------------------|------------------|------------------|
| READ | H | X | X | X | X |
| WRITE BYTE a | L | L | H | H | H |
| WRITE BYTE b | L | H | L | H | H |
| WRITE BYTE c | L | H | H | L | H |
| WRITE BYTE d | L | H | H | H | L |
| WRITE ALL BYTES | L | L | L | L | L |
| WRITE ABORT/NOP | L | H | H | H | H |

Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x72)

| Operation | \overline{WE} | $\overline{Bw_a}$ | $\overline{Bw_b}$ | $\overline{Bw_c}$ | $\overline{Bw_d}$ | $\overline{Bw_e}$ | $\overline{Bw_f}$ | $\overline{Bw_g}$ | $\overline{Bw_h}$ |
|-----------------|-----------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| READ | H | X | X | X | X | X | X | X | X |
| WRITE BYTE a | L | L | H | H | H | H | H | H | H |
| WRITE BYTE b | L | H | L | H | H | H | H | H | H |
| WRITE BYTE c | L | H | H | L | H | H | H | H | H |
| WRITE BYTE d | L | H | H | H | L | H | H | H | H |
| WRITE BYTE e | L | H | H | H | H | L | H | H | H |
| WRITE BYTE f | L | H | H | H | H | H | L | H | H |
| WRITE BYTE g | L | H | H | H | H | H | H | L | H |
| WRITE BYTE h | L | H | H | H | H | H | H | H | L |
| WRITE ALL BYTES | L | L | L | L | L | L | L | L | L |
| WRITE ABORT/NOP | L | H | H | H | H | H | H | H | H |

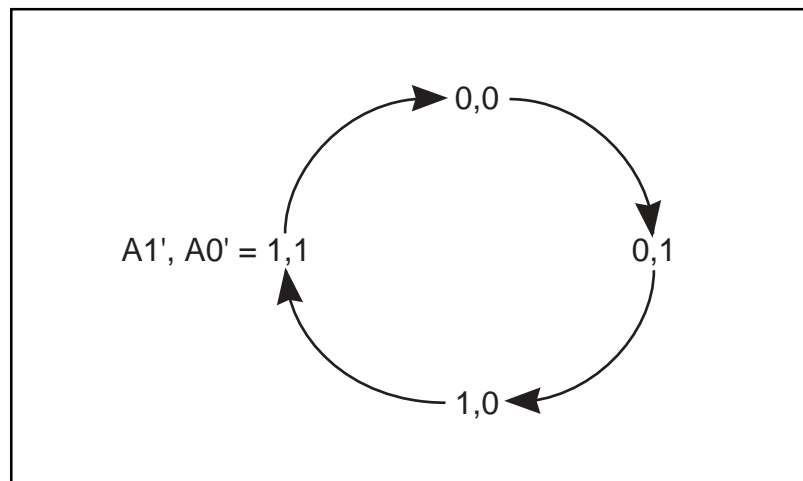
Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---------------------------|----------------------------|----------------------------|----------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|--------------------------------|------|
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _D | Power Dissipation | 1.6 | W |
| I _{OUT} | Output Current (per I/O) | 100 | mA |
| V _{IN} , V _{OUT} | Voltage Relative to V _{SS} for I/O Pins | -0.5 to V _{DDQ} + 0.3 | V |
| V _{IN} | Voltage Relative to V _{SS} for for Address and Control Inputs | -0.3 to 4.6 | V |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLPx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

OPERATING RANGE (IS61NVPx)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | 3.3V | | 2.5V | | Unit |
|-----------------|------------------------|--|------|-----------------------|------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -4.0 mA (3.3V) I _{OH} = -1.0 mA (2.5V) | 2.4 | — | 2.0 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V) | — | 0.4 | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | 1.7 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.7 | V |
| I _{LI} | Input Leakage Current | V _{SS} ≤ V _{IN} ≤ V _{DD} ⁽¹⁾ | -5 | 5 | -5 | 5 | μA |
| I _{LO} | Output Leakage Current | V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , $\overline{OE} = V_{IH}$ | -5 | 5 | -5 | 5 | μA |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | Temp. range | x18 | -250 MAX | | | -200 MAX | | | Unit |
|------------------|-----------------------------|--|--------------|------------|-------------|------------|------------|-------------|------------|----|------|
| | | | | | x36 | x72 | x18 | x36 | x72 | | |
| I _{CC} | AC Operating Supply Current | Device Selected, $\overline{OE} = V_{IH}$, ZZ ≤ V _{IL} , All Inputs ≤ 0.2V or ≥ V _{DD} - 0.2V, Cycle Time ≥ t _{kc} min. | Com. Ind. | 500 550 | 500 550 | 600 650 | 500 550 | 500 550 | 550 600 | mA | |
| I _{SB} | Standby Current TTL Input | Device Deselected, V _{DD} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} , ZZ ≤ V _{IL} , f = Max. | Com. Ind. | 150 — | 150 — | 150 — | 150 150 | 150 150 | 150 150 | mA | |
| I _{SB1} | Standby Current CMOS Input | Device Deselected, V _{DD} = Max., V _{IN} ≤ V _{SS} + 0.2V or ≥ V _{DD} - 0.2V f = 0 | Com. Ind. | 100 — | 100 — | 100 — | 100 115 | 100 115 | 100 115 | mA | |
| I _{SB2} | Sleep Mode | ZZ > V _{IH} | Com. Ind. | 60 — | 60 — | 60 — | 60 75 | 60 75 | 60 75 | mA | |

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} - 0.2V.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

3.3V I/O OUTPUT LOAD EQUIVALENT

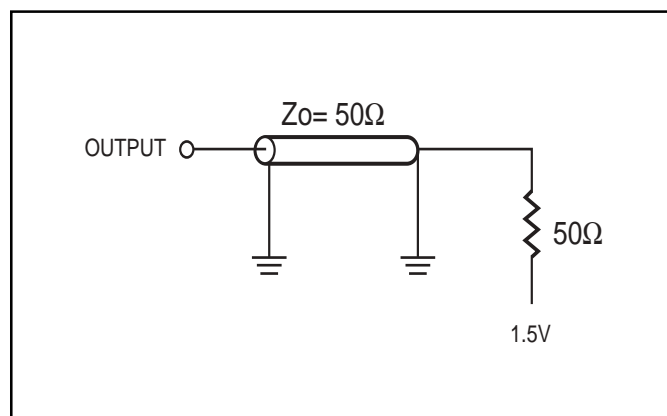


Figure 1

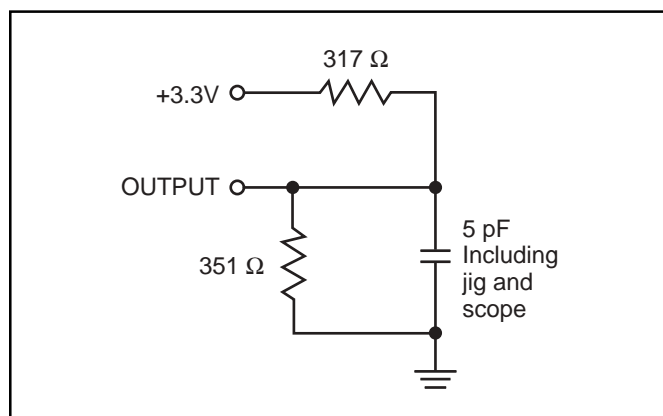


Figure 2

2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| Output Load | See Figures 3 and 4 |

2.5V I/O OUTPUT LOAD EQUIVALENT

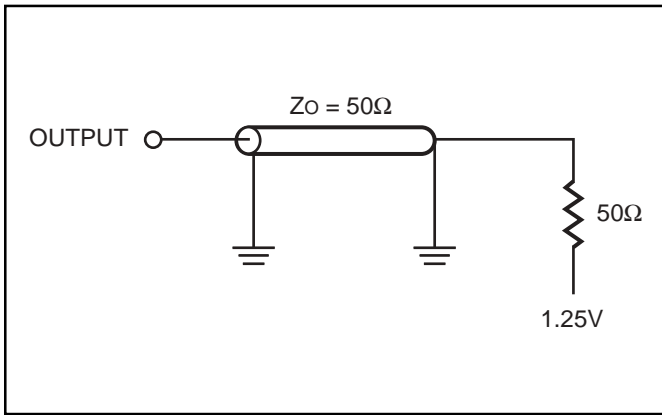


Figure 3

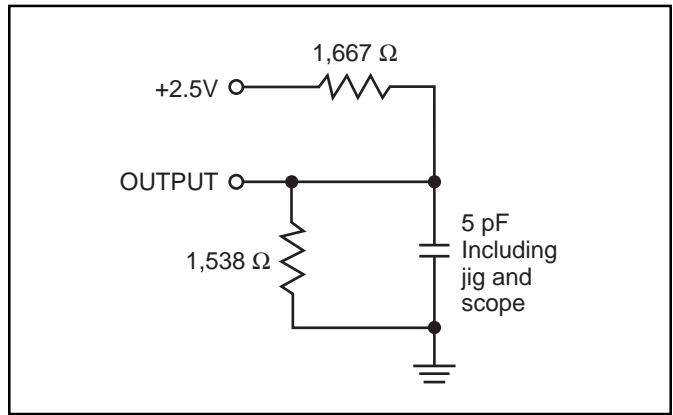


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -250 | | -200 | | Unit |
|--|---------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| fmax | Clock Frequency | — | 250 | — | 200 | MHz |
| t _{κC} | Cycle Time | 4.0 | — | 5 | — | ns |
| t _{κH} | Clock High Time | 1.7 | — | 2 | — | ns |
| t _{κL} | Clock Low Time | 1.7 | — | 2 | — | ns |
| t _{κQ} | Clock Access Time | — | 2.6 | — | 3.1 | ns |
| t _{κQX⁽²⁾} | Clock High to Output Invalid | 0.8 | — | 1.5 | — | ns |
| t _{κQLZ^(2,3)} | Clock High to Output Low-Z | 0.8 | — | 1 | — | ns |
| t _{κQHZ^(2,3)} | Clock High to Output High-Z | — | 2.6 | — | 3.0 | ns |
| t _{OEQ} | Output Enable to Output Valid | — | 2.6 | — | 3.1 | ns |
| t _{OE_LZ^(2,3)} | Output Enable to Output Low-Z | 0 | — | 0 | — | ns |
| t _{OE_HZ^(2,3)} | Output Disable to Output High-Z | — | 2.6 | — | 3.0 | ns |
| t _{AS} | Address Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{WS} | Read/Write Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{CES} | Chip Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{SE} | Clock Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{ADVS} | Address Advance Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{DS} | Data Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{AH} | Address Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{HE} | Clock Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{WH} | Write Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{CEH} | Chip Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{ADVH} | Address Advance Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{DH} | Data Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{PDS} | ZZ High to Power Down | — | 2 | — | 2 | cyc |
| t _{PUS} | ZZ Low to Power Down | — | 2 | — | 2 | cyc |

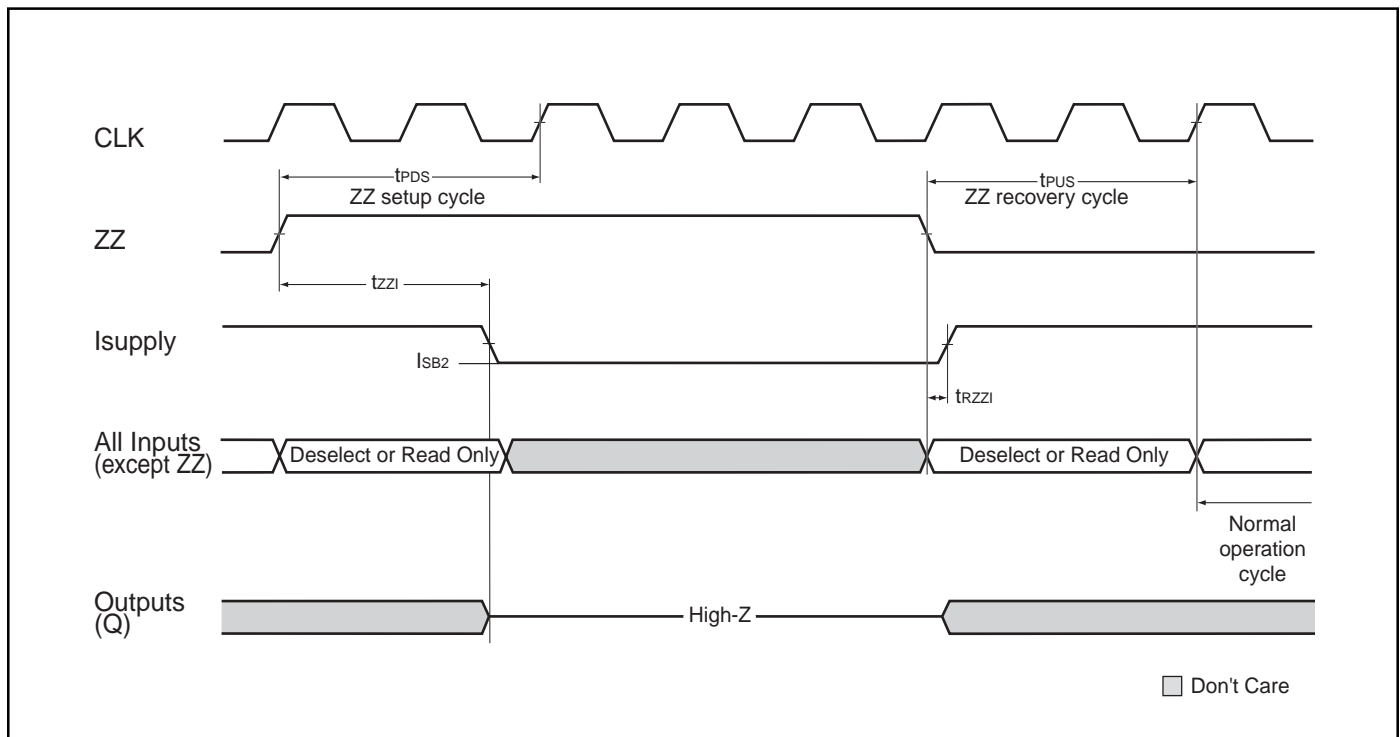
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

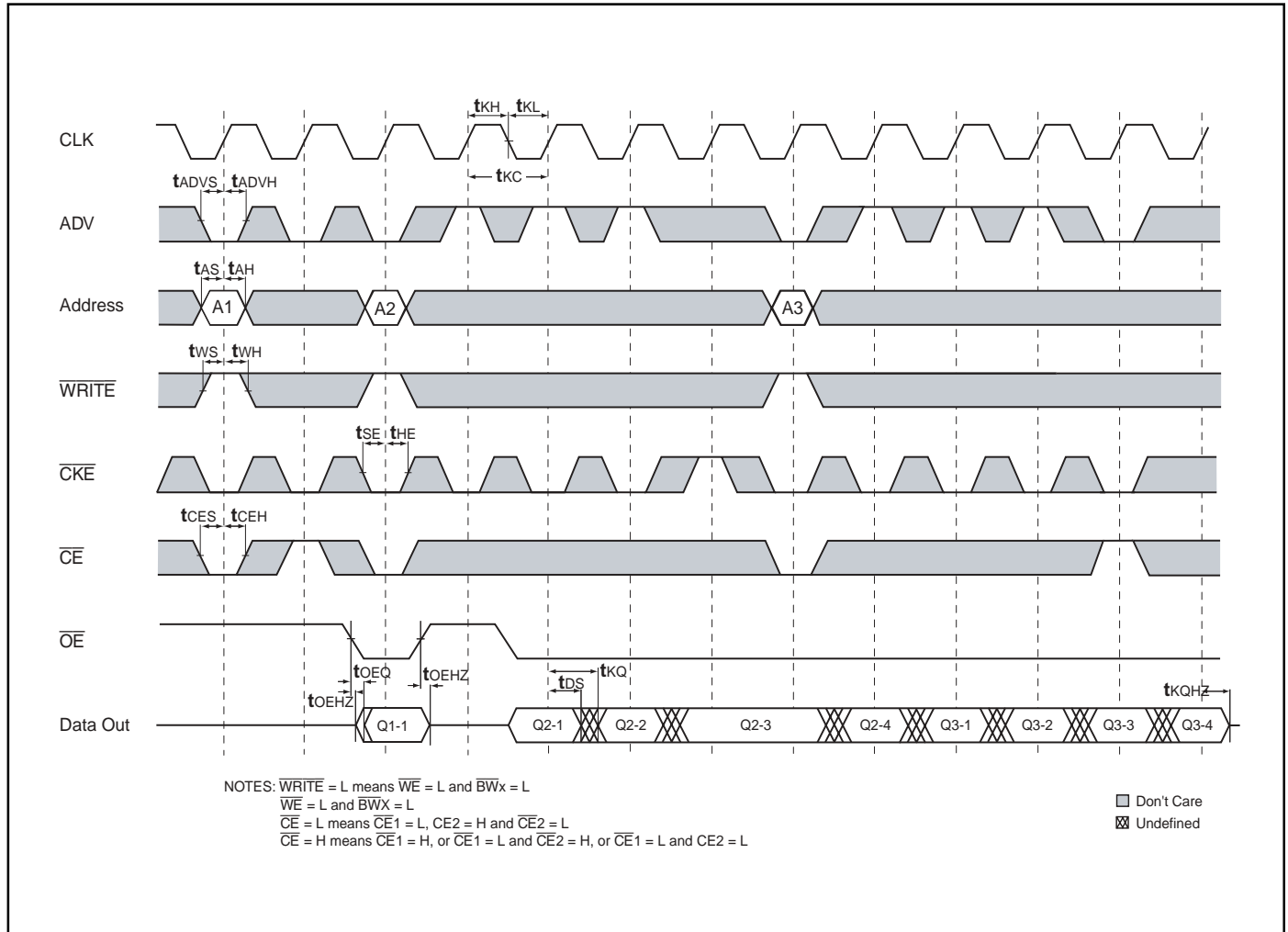
SLEEP MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|-------------------|-----------------------------------|----------------------|------|------|-------|
| I _{SB2} | Current during SLEEP MODE | ZZ ≥ V _{IH} | | 60 | mA |
| t _{PDS} | ZZ active to input ignored | | 2 | | cycle |
| t _{PUS} | ZZ inactive to input sampled | | 2 | | cycle |
| t _{ZZI} | ZZ active to SLEEP current | | 2 | | cycle |
| t _{TRZI} | ZZ inactive to exit SLEEP current | | 0 | | ns |

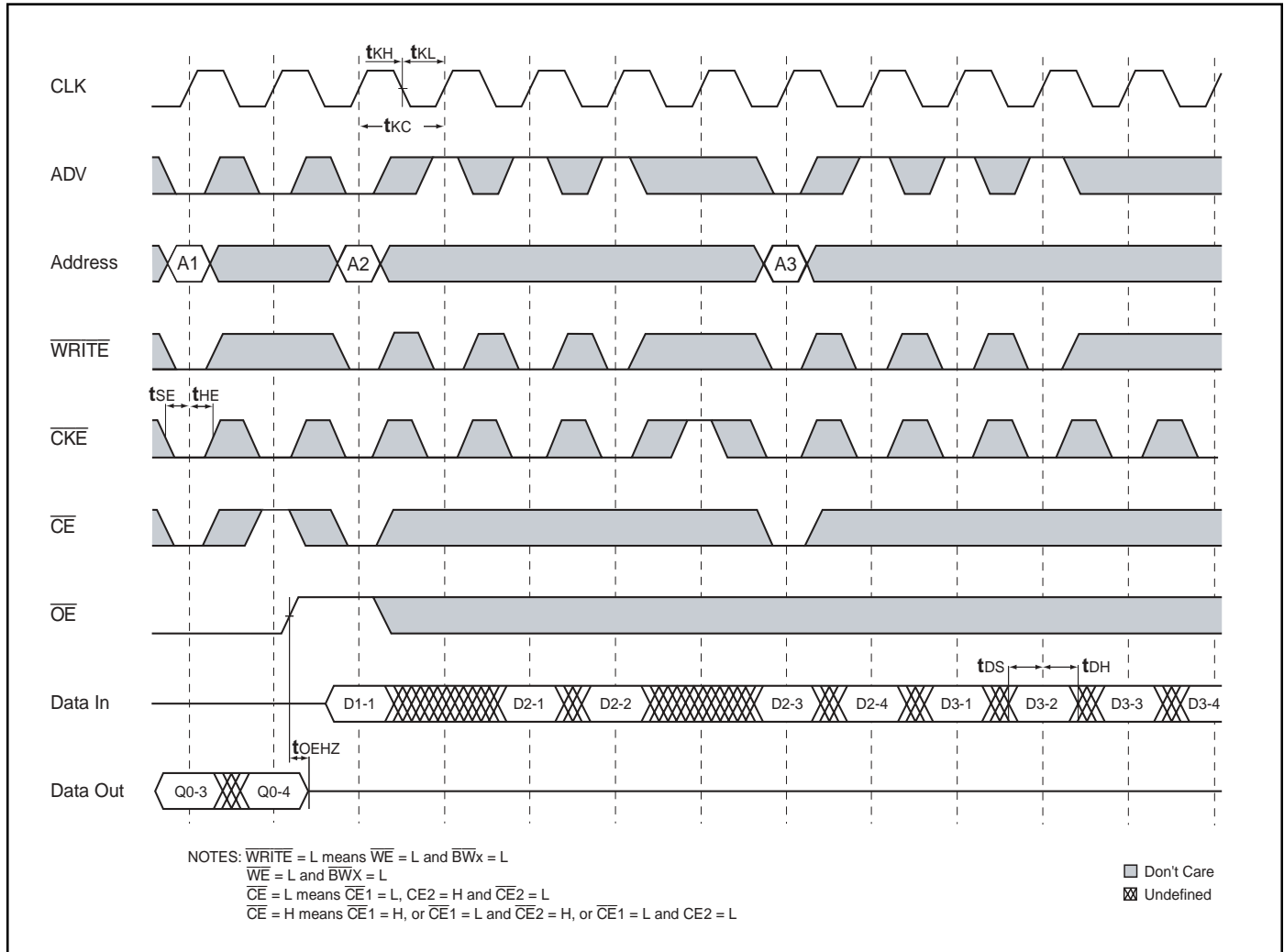
SLEEP MODE TIMING



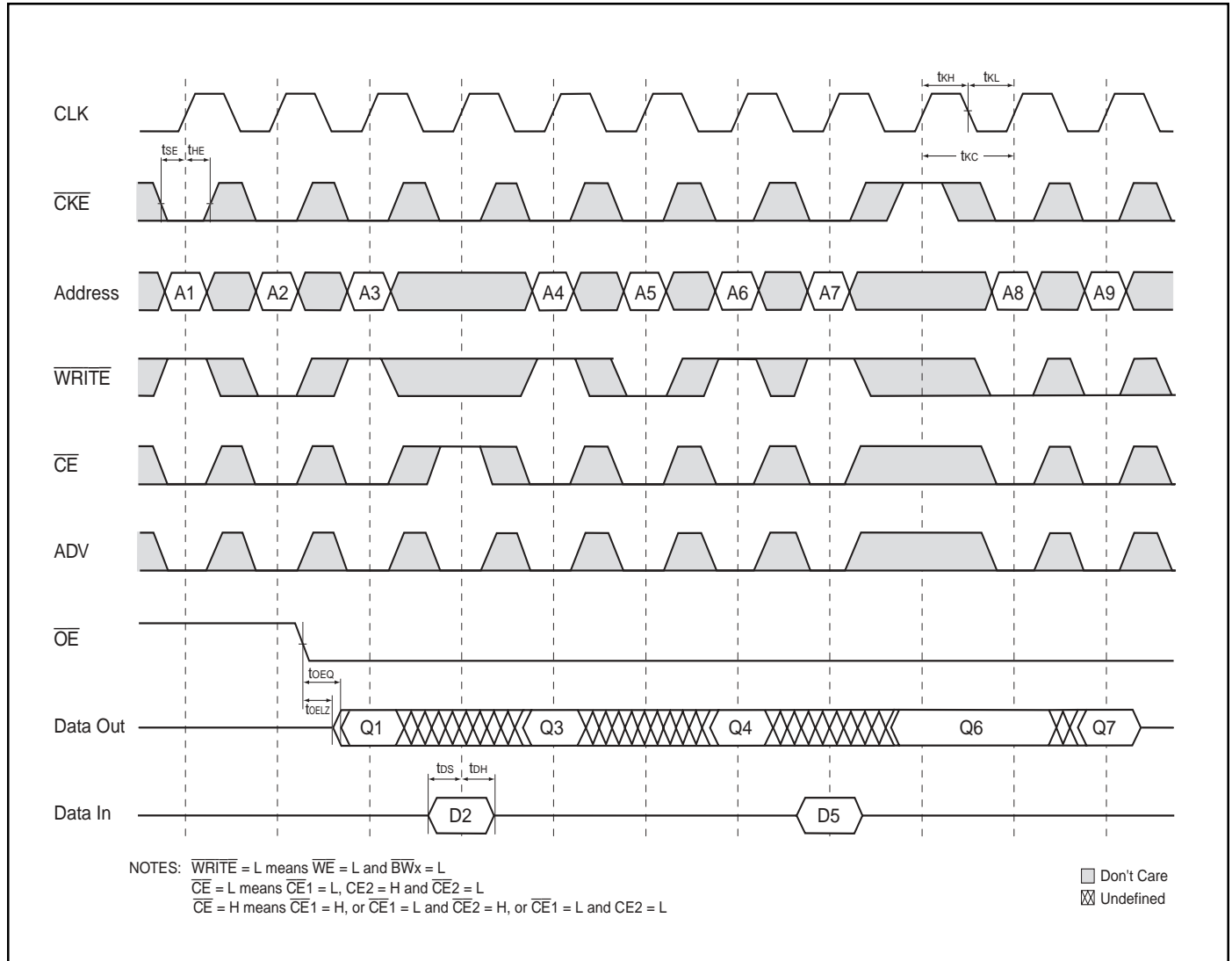
READ CYCLE TIMING



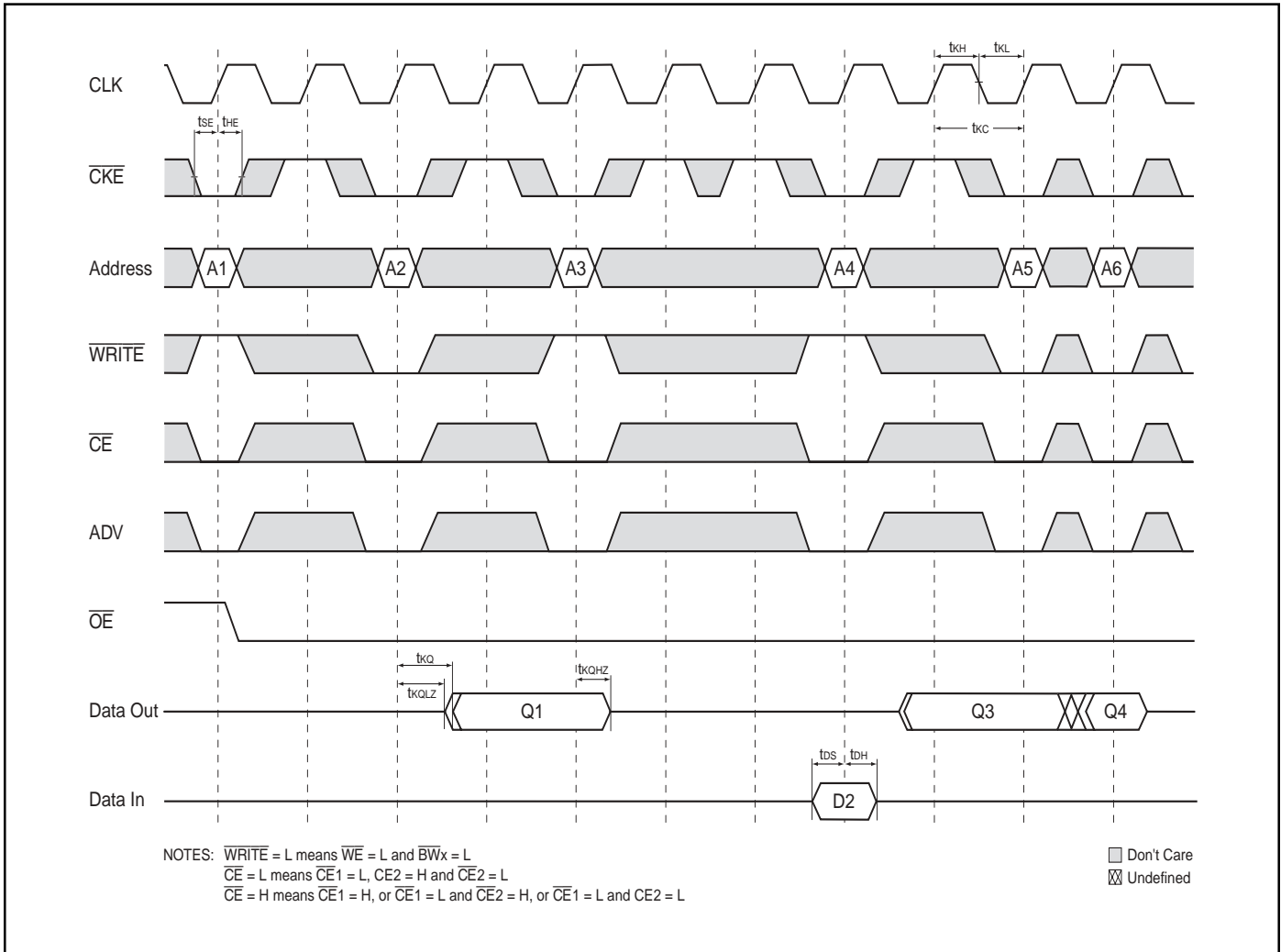
WRITE CYCLE TIMING



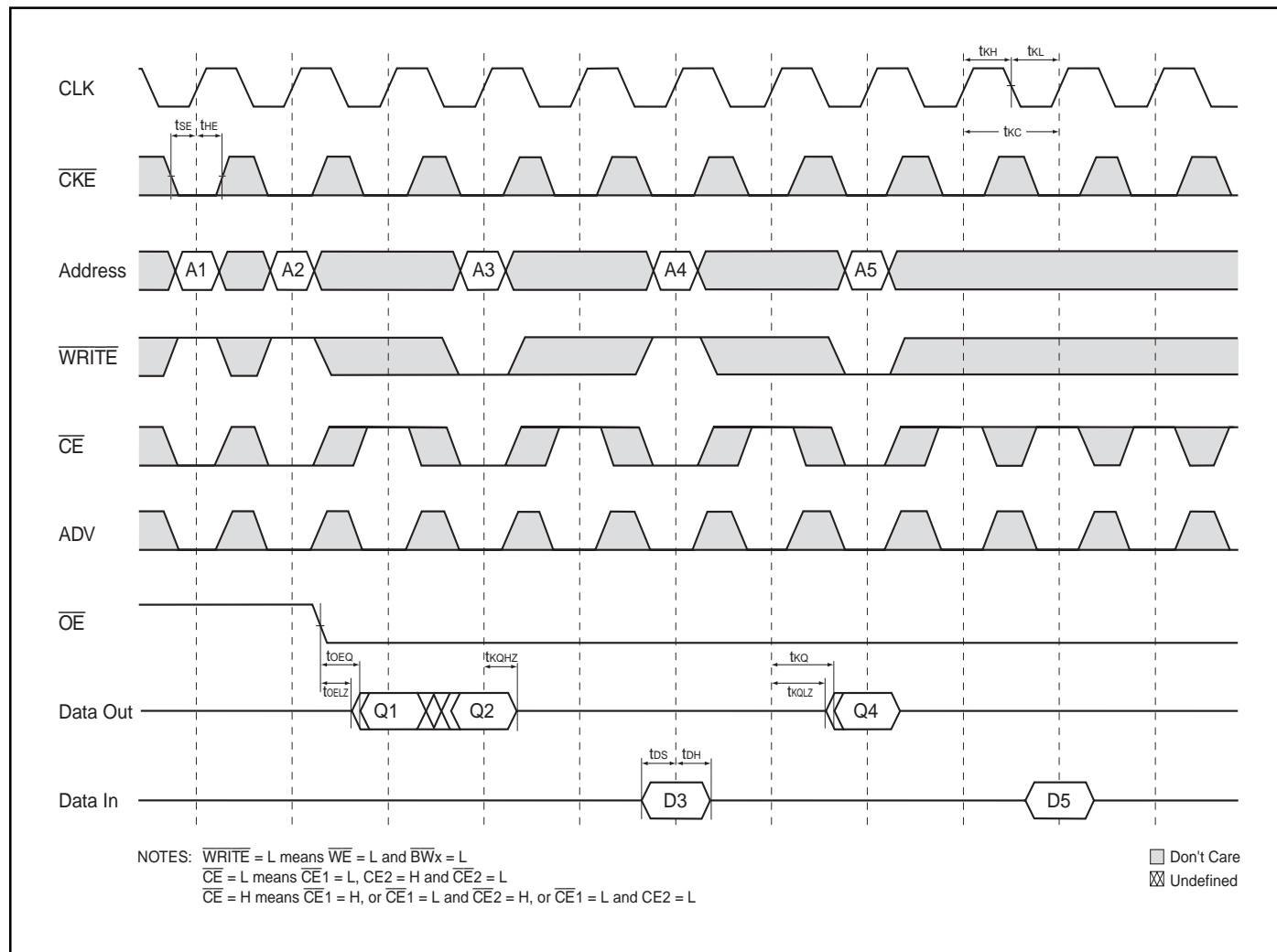
SINGLE READ/WRITE CYCLE TIMING



CKE OPERATION TIMING



\overline{CE} OPERATION TIMING



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The IS61NLP and IS61NVP have a serial boundary scan Test Access Port (TAP) in the PBGA package only. (Not available in TQFP package.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

DISABLING THE JTAG FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{CC} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

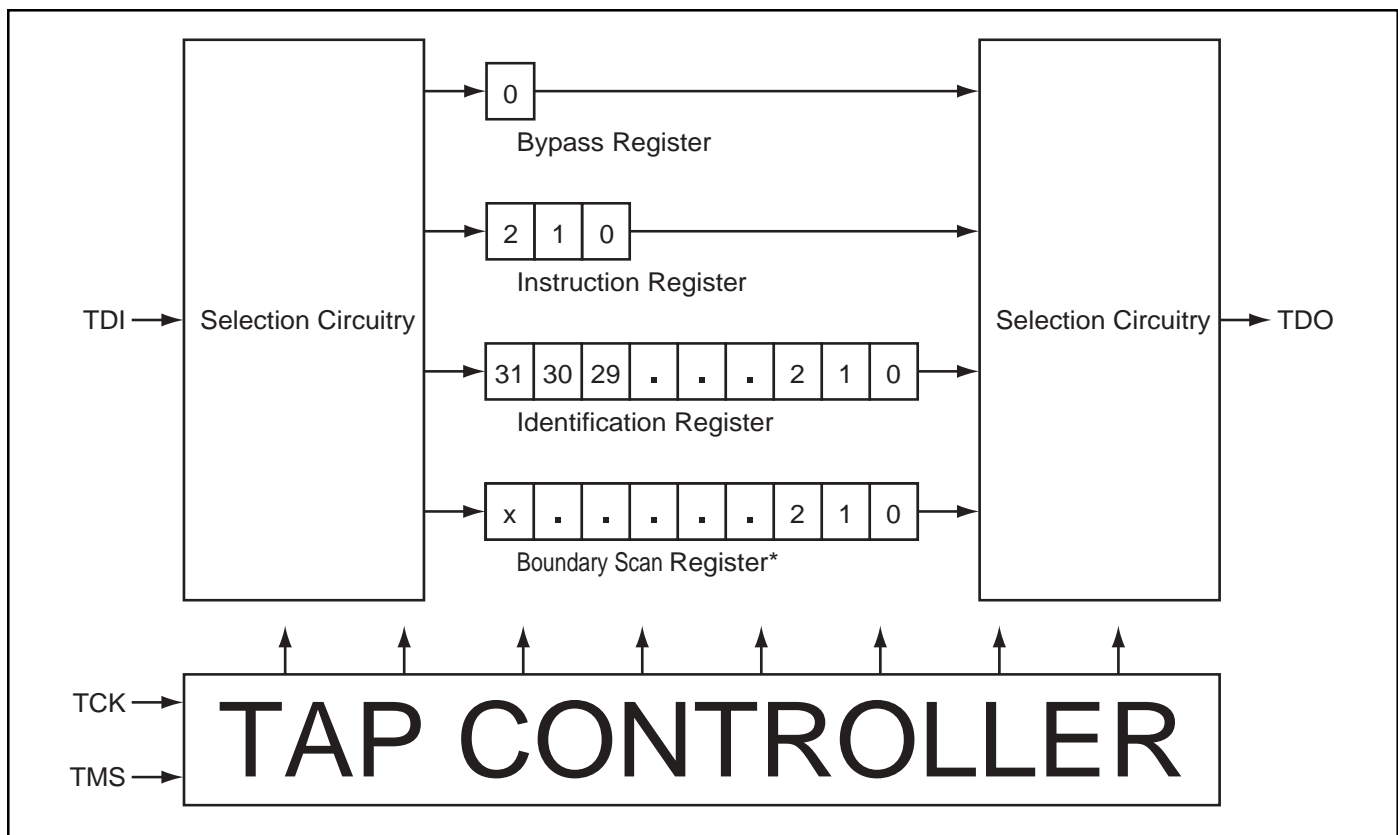
TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register

is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

| Register Name | Bit Size (x18) | Bit Size (x36) | Bit Size (x72) |
|---------------|----------------|----------------|----------------|
| Instruction | 3 | 3 | 3 |
| Bypass | 1 | 1 | 1 |
| ID | 32 | 32 | 32 |
| Boundary Scan | 75 | 75 | TBD |

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

IDENTIFICATION REGISTER DEFINITIONS

| Instruction Field | Description | 256K x 72 | 512K x 36 | 1M x 18 |
|--------------------------|--|------------|-------------|-------------|
| Revision Number (31:28) | Reserved for version number. | xxxx | xxxx | xxxx |
| Device Depth (27:23) | Defines depth of SRAM. 512K or 1M | 00110 | 00111 | 01000 |
| Device Width (22:18) | Defines width of the SRAM.x72, x36 or x18 | 00101 | 00100 | 00011 |
| ISSI Device ID (17:12) | Reserved for future use. | xxxx | xxxxx | xxxxx |
| ISSI JEDEC ID (11:1) | Allows unique identification of SRAM vendor. | 0011010101 | 00011010101 | 00011010101 |
| ID Register Presence (0) | Indicate the presence of an ID register. | 1 | 1 | 1 |

TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE-Z

The SAMPLE-Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

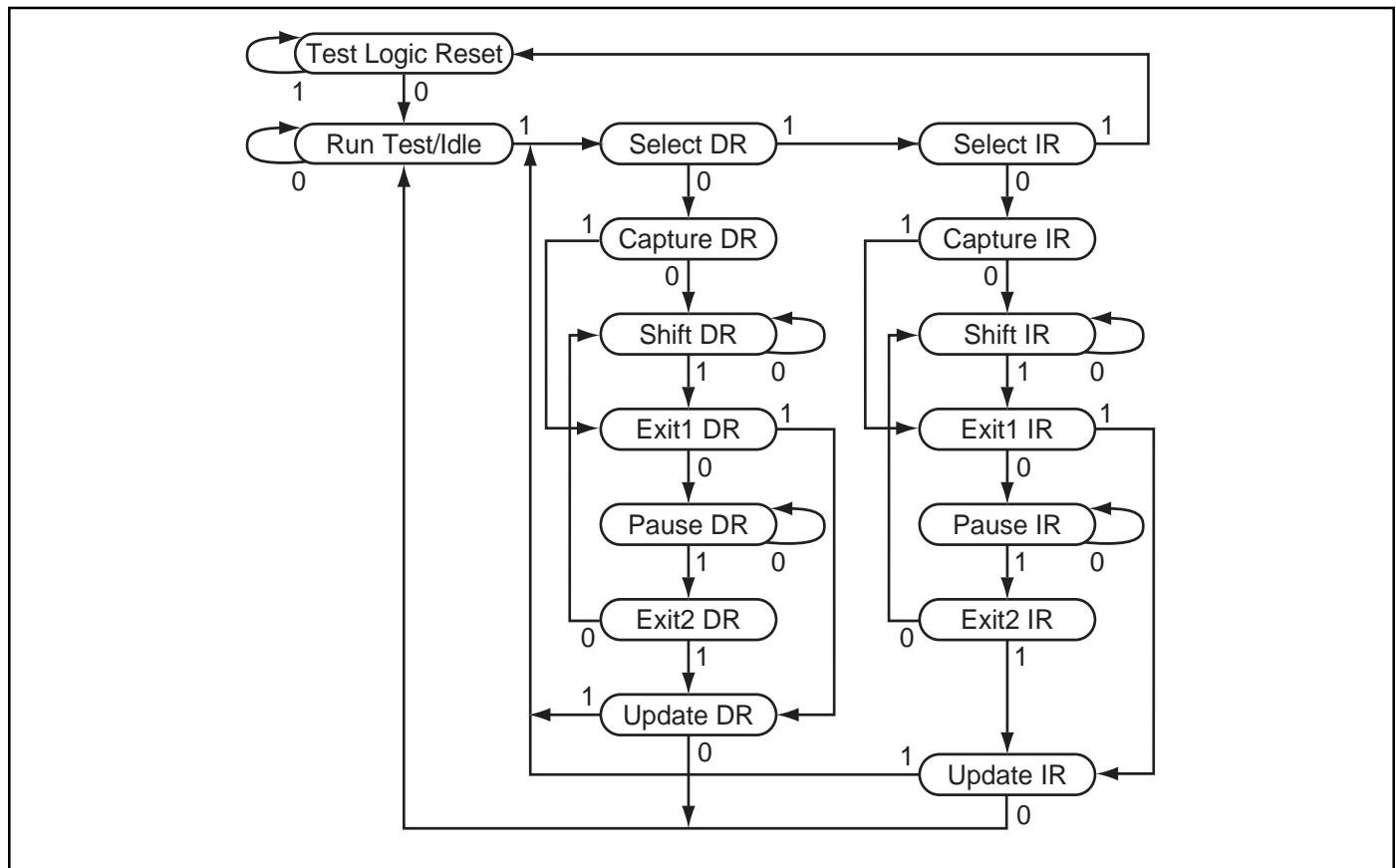
RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

INSTRUCTION CODES

| Code | Instruction | Description |
|------|----------------|--|
| 000 | EXTEST | Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant. |
| 001 | IDCODE | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation. |
| 010 | SAMPLE-Z | Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state. |
| 011 | RESERVED | Do Not Use: This instruction is reserved for future use. |
| 100 | SAMPLE/PRELOAD | Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant. |
| 101 | RESERVED | Do Not Use: This instruction is reserved for future use. |
| 110 | RESERVED | Do Not Use: This instruction is reserved for future use. |
| 111 | BYPASS | Places the bypass register between TDI and TDO. This operation does not affect SRAM operation. |

TAP CONTROLLER STATE DIAGRAM



TAP Electrical Characteristics Over the Operating Range^(1,2)

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------------|-----------------------|---|------|----------------------|-------|
| V _{OH1} | Output HIGH Voltage | I _{OH} = -2.0 mA | 1.7 | — | V |
| V _{OH2} | Output HIGH Voltage | I _{OH} = -100 μA | 2.1 | — | V |
| V _{OL1} | Output LOW Voltage | I _{OL} = 2.0 mA | — | 0.7 | V |
| V _{OL2} | Output LOW Voltage | I _{OL} = 100 μA | — | 0.2 | V |
| V _{IH} | Input HIGH Voltage | | 1.7 | V _{DD} +0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.7 | V |
| I _X | Input Leakage Current | V _{SS} ≤ V _I ≤ V _{DDQ} | -10 | 10 | μA |

Notes:

- All Voltage referenced to Ground.
- Overshoot: V_{IH} (AC) ≤ V_{DD} +1.5V for t ≤ t_{TCYC}/2,
 Undershoot: V_{IL} (AC) ≤ 0.5V for t ≤ t_{TCYC}/2,
 Power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

TAP AC ELECTRICAL CHARACTERISTICS^(1,2) (OVER OPERATING RANGE)

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|-------------------------------|------|------|------|
| t _{TCYC} | TCK Clock cycle time | 100 | — | ns |
| f _{TF} | TCK Clock frequency | — | 10 | MHz |
| t _{TH} | TCK Clock HIGH | 40 | — | ns |
| t _{TL} | TCK Clock LOW | 40 | — | ns |
| t _{TMSS} | TMS setup to TCK Clock Rise | 10 | — | ns |
| t _{TDIS} | TDI setup to TCK Clock Rise | 10 | — | ns |
| t _{CS} | Capture setup to TCK Rise | 10 | — | ns |
| t _{TMSh} | TMS hold after TCK Clock Rise | 10 | — | ns |
| t _{TDIH} | TDI Hold after Clock Rise | 10 | — | ns |
| t _{CH} | Capture hold after Clock Rise | 10 | — | ns |
| t _{TDOV} | TCK LOW to TDO valid | — | 20 | ns |
| t _{TDOX} | TCK LOW to TDO invalid | 0 | — | ns |

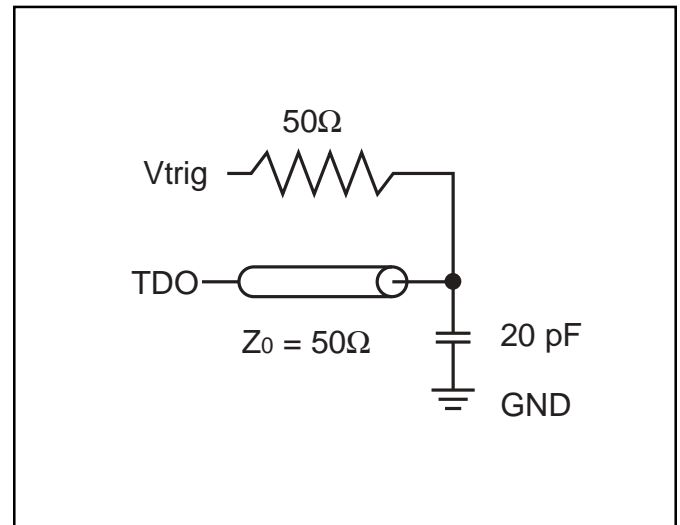
Notes:

- Both t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
- Test conditions are specified using the load in TAP AC test conditions. t_r/t_f = 1 ns.

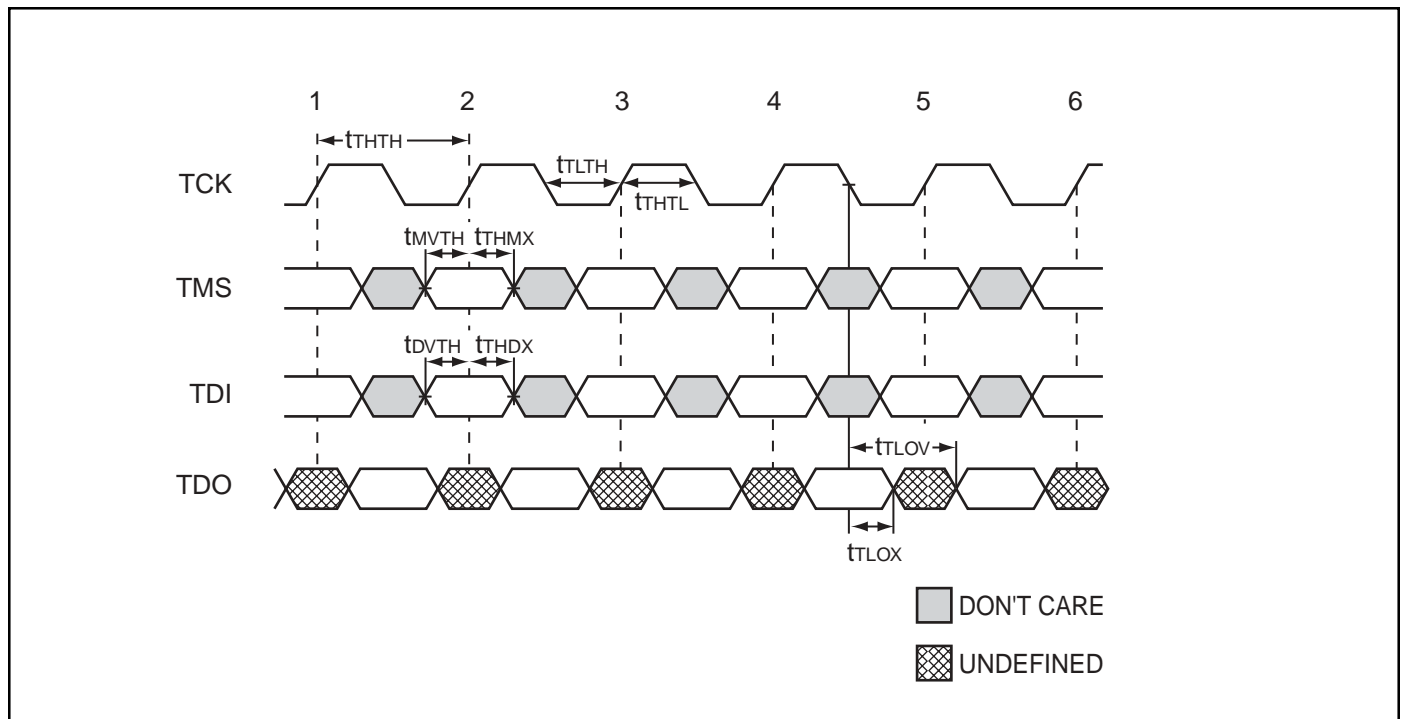
TAP AC TEST CONDITIONS (2.5V/3.3V)

| | |
|--------------------------------------|---------------------|
| Input pulse levels | 0 to 2.5V/0 to 3.0V |
| Input rise and fall times | 1ns |
| Input timing reference levels | 1.25V/1.5V |
| Output reference levels | 1.25V/1.5V |
| Test load termination supply voltage | 1.25V/1.5V |
| Vtrig | 1.25V/1.5V |

TAP Output Load Equivalent



TAP TIMING



209 BOUNDARY SCAN ORDER (256K X 72)

TBD

165 PBGA BOUNDARY SCAN ORDER (x 36)

| Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID |
|-------|-------------|---------|-------|------------------|---------|-------|------------------|---------|-------|-------------|---------|
| 1 | MODE | 1R | 21 | DQb | 11G | 41 | NC | 1A | 61 | DQd | 1J |
| 2 | NC | 6N | 22 | DQb | 11F | 42 | $\overline{CE}2$ | 6A | 62 | DQd | 1K |
| 3 | NC | 11P | 23 | DQb | 11E | 43 | $\overline{BW}a$ | 5B | 63 | DQd | 1L |
| 4 | A | 8P | 24 | DQb | 11D | 44 | $\overline{BW}b$ | 5A | 64 | DQd | 1M |
| 5 | A | 8R | 25 | DQb | 10G | 45 | $\overline{BW}c$ | 4A | 65 | DQd | 2J |
| 6 | A | 9R | 26 | DQb | 10F | 46 | $\overline{BW}d$ | 4B | 66 | DQd | 2K |
| 7 | A | 9P | 27 | DQb | 10E | 47 | CE2 | 3B | 67 | DQd | 2L |
| 8 | A | 10P | 28 | DQb | 10D | 48 | \overline{CE} | 3A | 68 | DQd | 2M |
| 9 | A | 10R | 29 | DQb | 11C | 49 | A | 2A | 69 | DQd | 1N |
| 10 | A | 11R | 30 | NC | 11A | 50 | A | 2B | 70 | A | 3P |
| 11 | ZZ | 11H | 31 | A | 10A | 51 | NC | 1B | 71 | A | 3R |
| 12 | DQa | 11N | 32 | A | 10B | 52 | DQc | 1C | 72 | A | 4R |
| 13 | DQa | 11M | 33 | A | 9A | 53 | DQc | 1D | 73 | A | 4P |
| 14 | DQa | 11L | 34 | A | 9B | 54 | DQc | 1E | 74 | A1 | 6P |
| 15 | DQa | 11K | 35 | ADV | 8A | 55 | DQc | 1F | 75 | A0 | 6R |
| 16 | DQa | 11J | 36 | \overline{OE} | 8B | 56 | DQc | 1G | | | |
| 17 | DQa | 10M | 37 | \overline{CKE} | 7A | 57 | DQc | 2D | | | |
| 18 | DQa | 10L | 38 | \overline{WE} | 7B | 58 | DQc | 2E | | | |
| 19 | DQa | 10K | 39 | CLK | 6B | 59 | DQc | 2F | | | |
| 20 | DQa | 10J | 40 | NC | 11B | 60 | DQc | 2G | | | |

165 PBGA BOUNDARY SCAN ORDER (x 18)

| Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID |
|-------|-------------|---------|-------|------------------|---------|-------|-------------------|---------|-------|-------------|---------|
| 1 | MODE | 1R | 21 | DQa | 11G | 41 | NC | 1A | 61 | DQb | 1J |
| 2 | NC | 6N | 22 | DQa | 11F | 42 | $\overline{CE}2$ | 6A | 62 | DQb | 1K |
| 3 | NC | 11P | 23 | DQa | 11E | 43 | $\overline{B}W_a$ | 5B | 63 | DQb | 1L |
| 4 | A | 8P | 24 | DQa | 11D | 44 | NC | 5A | 64 | DQb | 1M |
| 5 | A | 8R | 25 | DQa | 11C | 45 | $\overline{B}W_b$ | 4A | 65 | DQb | 1N |
| 6 | A | 9R | 26 | NC | 10F | 46 | NC | 4B | 66 | NC | 2K |
| 7 | A | 9P | 27 | NC | 10E | 47 | CE2 | 3B | 67 | NC | 2L |
| 8 | A | 10P | 28 | NC | 10D | 48 | \overline{CE} | 3A | 68 | NC | 2M |
| 9 | A | 10R | 29 | NC | 10G | 49 | A | 2A | 69 | NC | 2J |
| 10 | A | 11R | 30 | A | 11A | 50 | A | 2B | 70 | A | 3P |
| 11 | ZZ | 11H | 31 | A | 10A | 51 | NC | 1B | 71 | A | 3R |
| 12 | NC | 11N | 32 | A | 10B | 52 | NC | 1C | 72 | A | 4R |
| 13 | NC | 11M | 33 | A | 9A | 53 | NC | 1D | 73 | A | 4P |
| 14 | NC | 11L | 34 | A | 9B | 54 | NC | 1E | 74 | A1 | 6P |
| 15 | NC | 11K | 35 | ADV | 8A | 55 | NC | 1F | 75 | A0 | 6R |
| 16 | NC | 11J | 36 | \overline{OE} | 8B | 56 | NC | 1G | | | |
| 17 | DQa | 10M | 37 | \overline{CKE} | 7A | 57 | DQb | 2D | | | |
| 18 | DQa | 10L | 38 | \overline{WE} | 7B | 58 | DQb | 2E | | | |
| 19 | DQa | 10K | 39 | CLK | 6B | 59 | DQb | 2F | | | |
| 20 | DQa | 10J | 40 | NC | 11B | 60 | DQb | 2G | | | |

119 BOUNDARY SCAN ORDER (512K X 36)

TBD

119 BOUNDARY SCAN ORDER (1M X 18)

TBD

ORDERING INFORMATION (3.3V core/2.5V- 3.3V I/O)

Commercial Range: 0°C to +70°C

| Access Time | Order Part Number | Package |
|----------------|---------------------|----------|
| 256Kx72 | | |
| 250 | IS61NLP25672-250B1 | 209 PBGA |
| 200 | IS61NLP25672-200B1 | 209 PBGA |
| 512Kx36 | | |
| 250 | IS61NLP51236-250TQ | 100 TQFP |
| | IS61NLP51236-250B2 | 119 PBGA |
| | IS61NLP51236-250B3 | 165 PBGA |
| 200 | IS61NLP51236-200TQ | 100 TQFP |
| | IS61NLP51236-200B2 | 119 PBGA |
| | IS61NLP51236-200B3 | 165 PBGA |
| 1Mx18 | | |
| 250 | IS61NLP102418-250TQ | 100 TQFP |
| | IS61NLP102418-250B2 | 119 PBGA |
| | IS61NLP102418-250B3 | 165 PBGA |
| 200 | IS61NLP102418-200TQ | 100 TQFP |
| | IS61NLP102418-200B2 | 119 PBGA |
| | IS61NLP102418-200B3 | 165 PBGA |

Industrial Range: -40°C to +85°C

| Access Time | Order Part Number | Package |
|----------------|----------------------|----------|
| 256Kx72 | | |
| 250 | IS61NLP25672-250B1I | 209 PBGA |
| 200 | IS61NLP25672-200B1I | 209 PBGA |
| 512Kx36 | | |
| 250 | IS61NLP51236-250TQI | 100 TQFP |
| | IS61NLP51236-250B2I | 119 PBGA |
| | IS61NLP51236-250B3I | 165 PBGA |
| 200 | IS61NLP51236-200TQI | 100 TQFP |
| | IS61NLP51236-200B2I | 119 PBGA |
| | IS61NLP51236-200B3I | 165 PBGA |
| 1Mx18 | | |
| 250 | IS61NLP102418-250TQI | 100 TQFP |
| | IS61NLP102418-250B2I | 119 PBGA |
| | IS61NLP102418-250B3I | 165 PBGA |
| 200 | IS61NLP102418-200TQI | 100 TQFP |
| | IS61NLP102418-200B2I | 119 PBGA |
| | IS61NLP102418-200B3I | 165 PBGA |

ORDERING INFORMATION (2.5V core/2.5V I/O)

Commercial Range: 0°C to +70°C

| Access Time | Order Part Number | Package |
|----------------|---------------------|----------|
| 256Kx72 | | |
| 250 | IS61NVP25672-250B1 | 209 PBGA |
| 200 | IS61NVP25672-200B1 | 209 PBGA |
| 512Kx36 | | |
| 250 | IS61NVP51236-250TQ | 100 TQFP |
| | IS61NVP51236-250B2 | 119 PBGA |
| | IS61NVP51236-250B3 | 165 PBGA |
| 200 | IS61NVP51236-200TQ | 100 TQFP |
| | IS61NVP51236-200B2 | 119 PBGA |
| | IS61NVP51236-200B3 | 165 PBGA |
| 1Mx18 | | |
| 250 | IS61NVP102418-250TQ | 100 TQFP |
| | IS61NVP102418-250B2 | 119 PBGA |
| | IS61NVP102418-250B3 | 165 PBGA |
| 200 | IS61NVP102418-200TQ | 100 TQFP |
| | IS61NVP102418-200B2 | 119 PBGA |
| | IS61NVP102418-200B3 | 165 PBGA |

Industrial Range: -40°C to +85°C

| Access Time | Order Part Number | Package |
|----------------|----------------------|----------|
| 256Kx72 | | |
| 250 | IS61NVP25672-250BI1 | 209 PBGA |
| 200 | IS61NVP25672-200BI1 | 209 PBGA |
| 512Kx36 | | |
| 250 | IS61NVP51236-250TQI | 100 TQFP |
| | IS61NVP51236-250B2I | 119 PBGA |
| | IS61NVP51236-250B3I | 165 PBGA |
| 200 | IS61NVP51236-200TQI | 100 TQFP |
| | IS61NVP51236-200B2I | 119 PBGA |
| | IS61NVP51236-200B3I | 165 PBGA |
| 1Mx18 | | |
| 250 | IS61NVP102418-250TQI | 100 TQFP |
| | IS61NVP102418-250B2I | 119 PBGA |
| | IS61NVP102418-250B3I | 165 PBGA |
| 200 | IS61NVP102418-200TQI | 100 TQFP |
| | IS61NVP102418-200B2I | 119 PBGA |
| | IS61NVP102418-200B3I | 165 PBGA |