FLASH-ROM MODULE 16MByte (4M x 32Bit), 144-Pin SODIMM, 3.3V Part No. HMF4M32B8VN

GENERAL DESCRIPTION

The HMF4M32B8VN is a high-speed flash read only memory (FROM) module containing 8,388,608 words organized in a x32bit configuration. The module consists of eight 2M x 8bit FROM mounted on a 144-pin, double-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Eight chip enable inputs, (/CS0, /CS1, /CS2, /CS3, /CS4, /CS5, /CS6, CS7) are used to enable the module's 4 bytes independently. Outputs enable (/OE) and write enable (/WE) can set the memory input and output.When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3.3V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Part Identifications

  HMF4M32B8VN : 16Mbyte, 144-pin SODIMM, Gold

- Access time : 70, 90 and 120ns
- High-density 16MByte design
- High-reliability, low-power design
- Single + 3V ± 0.5V power supply
- Easy memory expansion
- All inputs and outputs are TTL-compatible
- FR4-PCB design
- Low profile 144-pin SODIMM
- Minimum 1,000,000 write/erase cycle
- Sectors erase architecture
- Sector group protection
- Temporary sector group unprotection
- The used device is 2Mx8bit 48Pin TSOP

OPTIONS MARKING

- Timing

70ns access	-70
90ns access	-90
120ns access	-120

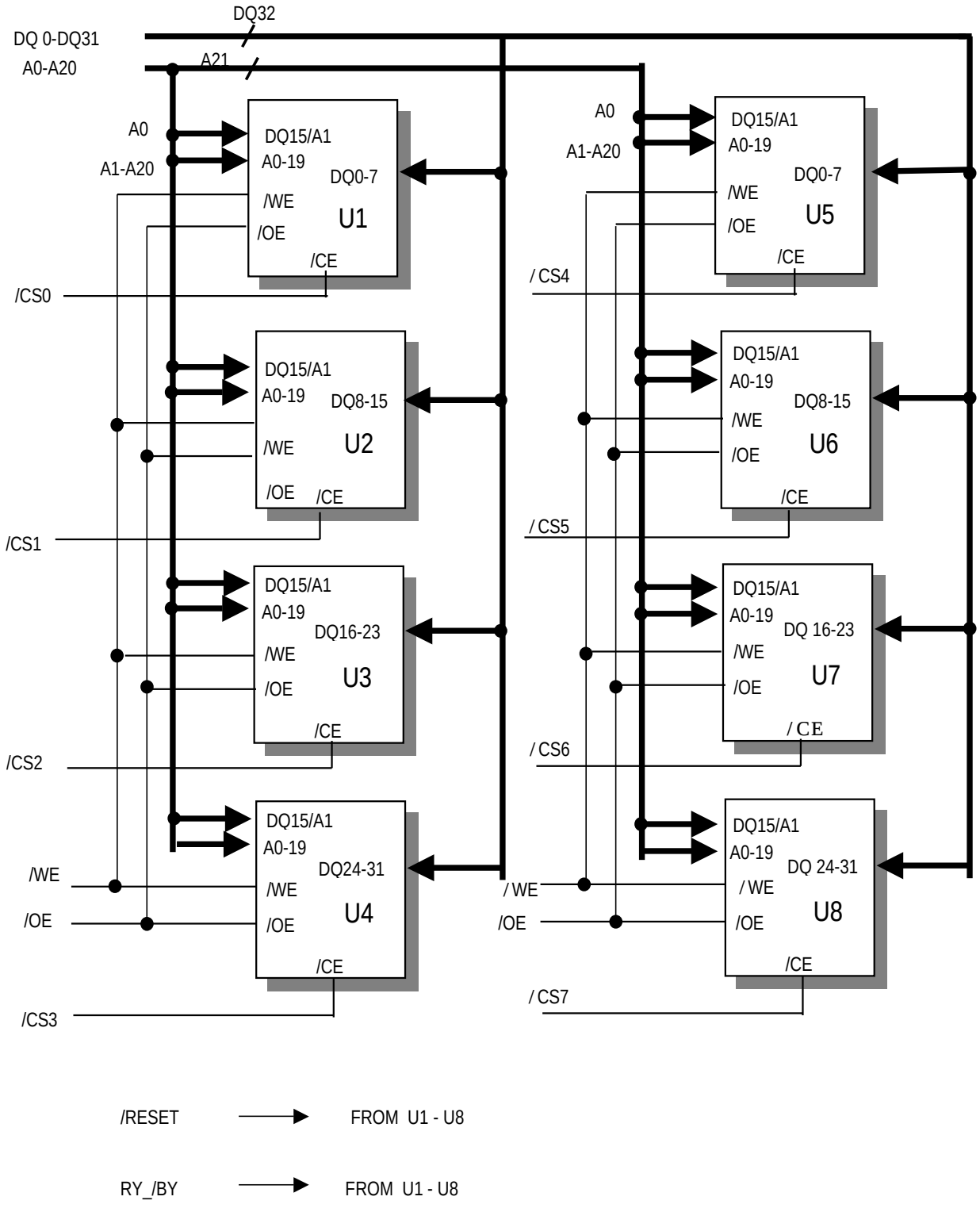
- Packages

144-pin SODIMM	B

PIN ASSIGNMENT

PIN	Front	PIN	Back	PIN	Frontl	PIN	Back	PIN	Front	PIN	Back
1	Vss	2	Vss	49	DQ13	50	NC	97	DQ22	98	NC
3	DQ0	4	NC	51	DQ14	52	NC	99	DQ23	100	NC
5	DQ1	6	NC	53	DQ15	54	NC	101	V_{CC}	102	V_{CC}
7	DQ2	8	NC	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	NC	57	NC	58	NC	105	A8	106	NC
11	V_{CC}	12	V_{CC}	59	NC	60	NC	107	Vss	108	Vss
13	DQ4	14	NC	61	NC	62	NC	109	A9	110	A12
15	DQ5	16	NC	63	V_{CC}	64	V_{CC}	111	A10	112	A11
17	DQ6	18	NC	65	NC	66	NC	113	V_{CC}	114	V_{CC}
19	DQ7	20	NC	67	/WE	68	/OE	115	/CS2	116	/CS6
21	Vss	22	Vss	69	A13	70	A16	117	/CS3	118	/CS7
23	/CS0	24	/CS4	71	A14	72	A17	119	Vss	120	Vss
25	/CS1	26	/CS5	73	A15	74	A18	121	DQ24	122	NC
27	V_{CC}	28	V_{CC}	75	Vss	76	Vss	123	DQ25	124	NC
29	A0	30	A3	77	A19	78	A21	125	DQ26	126	NC
31	A1	32	A4	79	A20	80	NC	127	DQ27	128	NC
33	A2	34	A5	81	V_{CC}	82	V_{CC}	129	V_{CC}	130	V_{CC}
35	Vss	36	Vss	83	DQ16	84	NC	131	DQ28	132	NC
37	DQ8	38	NC	85	DQ17	86	NC	133	DQ29	134	NC
39	DQ9	40	NC	87	DQ18	88	NC	135	DQ30	136	RY_/BY
41	DQ10	42	NC	89	DQ19	90	NC	137	DQ31	138	/RESET
43	DQ11	44	NC	91	Vss	92	Vss	139	Vss	140	Vss
45	V_{CC}	46	V_{CC}	93	DQ20	94	NC	141	NC	142	NC
47	DQ12	48	NC	95	DQ21	96	NC	143	V_{CC}	144	V_{CC}

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	Vcc±0.3	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE or ERASE	H	L	L	Din	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to +0.5V
Voltage with respect to ground Vcc	V_{CC}	-0.5V to +4.0V
Storage Temperature	T_{STG}	-65^{O}C to +150^{O}C
Operating Temperature	T_A	-55^{O}c to +125^{O}C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage t o the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ±5% device Supply Voltages	V_{CC}	3.0V		3.6V
Vcc for ± 10% device Supply Voltages	Vcc	2.7V		3.6V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^{O}C \le T_A \le 70\ ^{O}C$; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	Vcc=Vcc max, V_{IN}= GND to Vcc	I_{L1}		±1.0	µA
Output Leakage Current	Vcc=Vcc max, VOUT= GND to Vcc	I_{L0}		±1.0	µA
Output High Voltage	I_{OH} = -2.5mA, Vcc = Vcc min	V_{OH}	0.85* VCC		V
Output Low Voltage	I_{OL} = 12mA, Vcc =Vcc min	V_{OL}		0.45	V
Vcc Active Current for Read(1)	/CE = V_{IL}, /OE=V_{IH},	I_{CC1}	72	128	mA
Vcc Active Current for Program or Erase(2)	/CE = V_{IL}, /OE=V_{IH}	I_{CC2}	160	240	mA
Vcc Standby Current	/CE= V_{IH}	I_{CC3}	1.6	40	mA
Low Vcc Lock-Out Voltage		V_{LKO}	2.3	2.5	V

Notes: 1. The Icc current listed is typically less than 2mA/MHz, with /OE at V_{IH}.

2. Icc active while embedded algorithm (program or erase) is in progress

3. Maximum Icc current specifications are tested with Vcc=Vcc max

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	Sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	9	300	μs	Excludes system-level overhead
Chip Programming Time	-	18	54.8	Sec	Excludes system-level overhead

CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	64	60	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	68	96	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	60	72	pF

Notes : Test conditions T_A = 25°C, f=1.0 MHz.

AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		Speed Options				UNIT
JEDEC	STANDARD				70R	80	-90	-120	
T_{AVAV}	t_{RC}	Read Cycle Time		Min	70	80	90	120	ns
T_{AVQV}	t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}	Max	70	80	90	120	ns
T_{ELQV}	t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}	Max	70	80	90	120	ns
T_{GLQV}	t_{OE}	Chip Enable to Output Delay		Max	30	30	35	50	ns
T_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max	25	25	30	30	ns
T_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max	125	25	30	30	ns
T_{AXQX}	t_{OH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	0	0	ns

Notes : Test Conditions

Output Load : 1TTL gate and Output Load Capacitance 100 pF, in case of 55ns-30pF

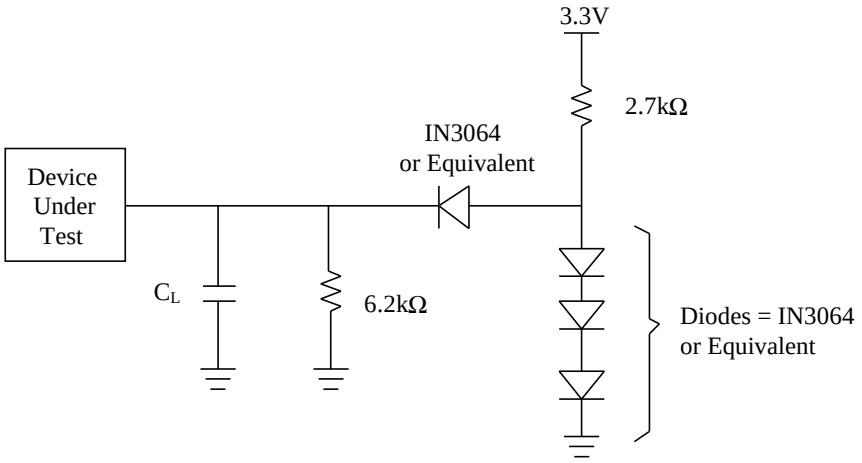
Input rise and fall times : 5 ns, In case of 55ns-5ns

Input pulse levels : 0.45V to 2.4V, In case of 55ns- 0.0V-3.0V

Timing measurement reference level

Input : 0.8V, Incase of 55ns-1.5V

Output : 2.0V, In case of 55ns-1.5V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		Speed Options				UNIT
JEDEC	STANDARD			70R	80	-90	-120	
T_{AVAV}	t_{WC}	Write Cycle Time	Min	70	80	90	120	ns
T_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
T_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
T_{DVWH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
T_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
T_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0				ns
T_{ELWL}	t_{CS}	/CE Setup Time	Min	0				ns
T_{WHEH}	t_{CH}	/CE Hold Time	Min	0				ns
T_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	0.7				sec
	t_{VCS}	Vcc set up time	Min	50				µs

Notes : 1. This does not include the preprogramming time

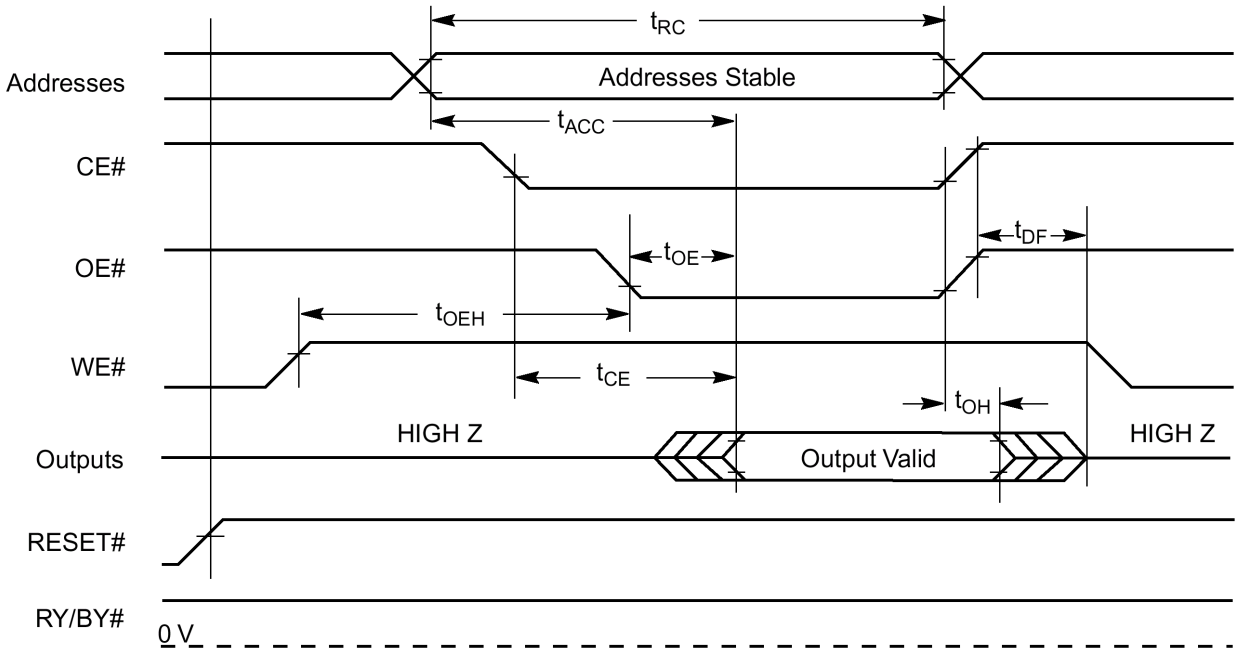
2. This timing is only for Sector Protect operations

u Erase/Program Operations
Alternate /CE Controlled Writes

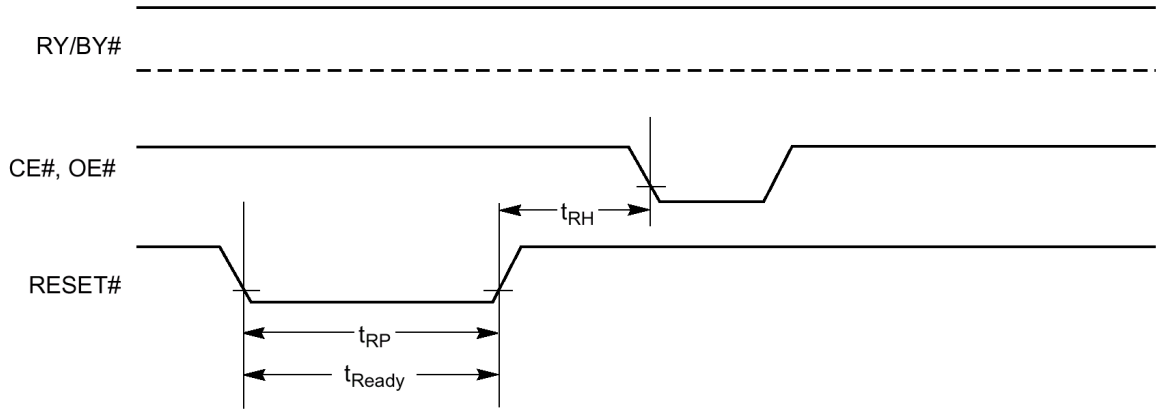
PARAMETER SYMBOLS		DESCRIPTION		SPEED OPTION				UNIT
JEDEC	STANDARD			70R	80	-90	-120	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	80	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0				ns
t_{WLEL}	t_{WS}	/WE Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	/WE Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	/CE Pulse Width	Min	35	35	45	50	ns
t_{EHEL}	t_{CPH}	/CE Pulse Width High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note)	Typ	0.7				sec

Notes : This does not include the preprogramming time.

u READ OPERATIONS TIMING

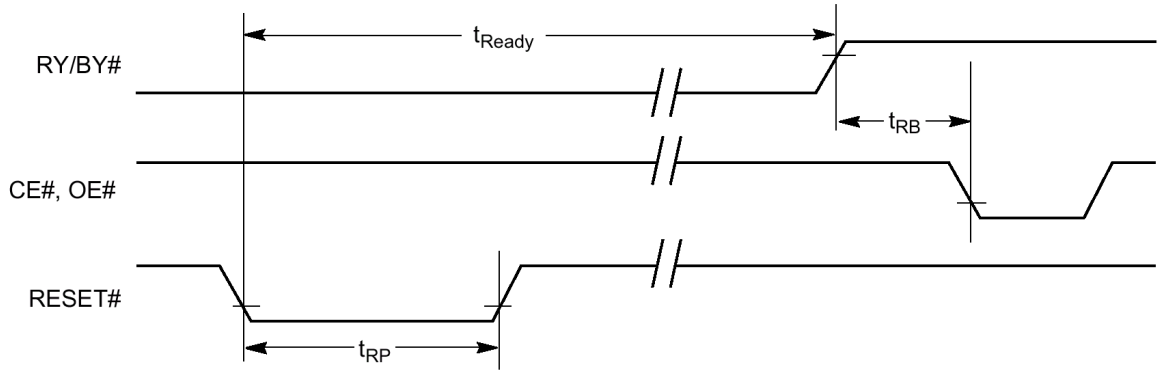


u RESET TIMING

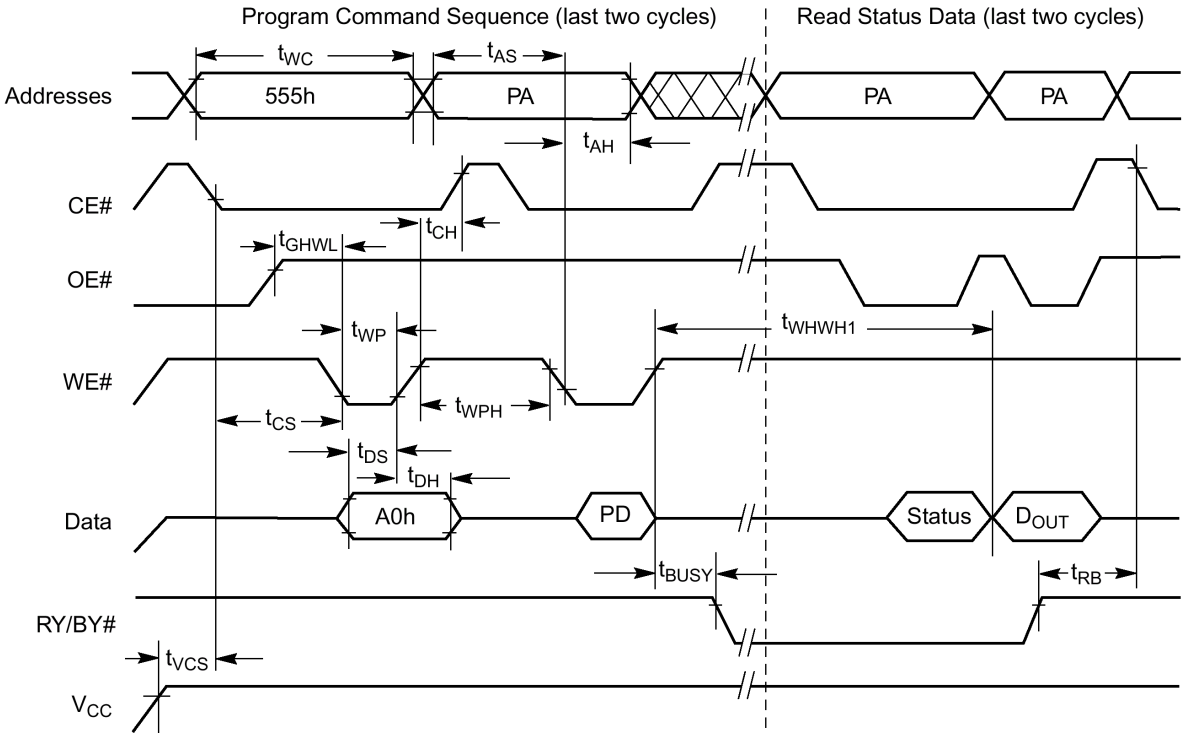


Reset Timings NOT during Embedded Algorithms

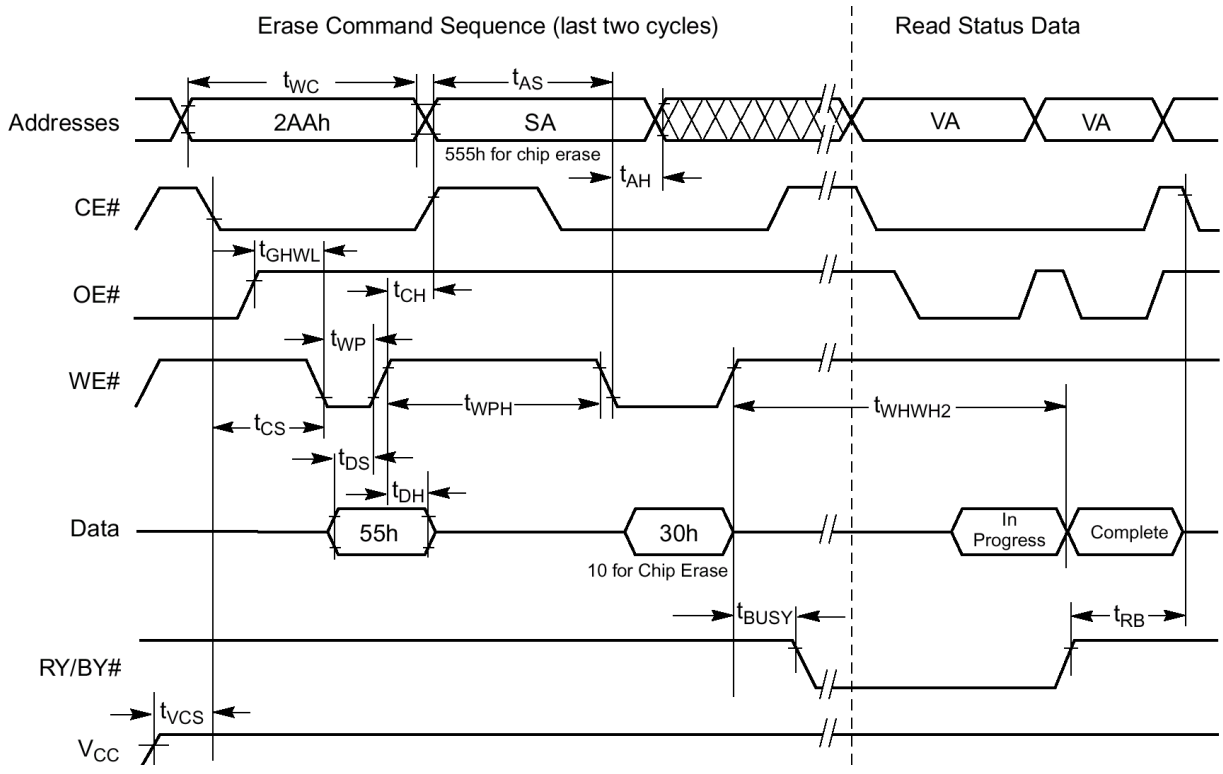
Reset Timings during Embedded Algorithms



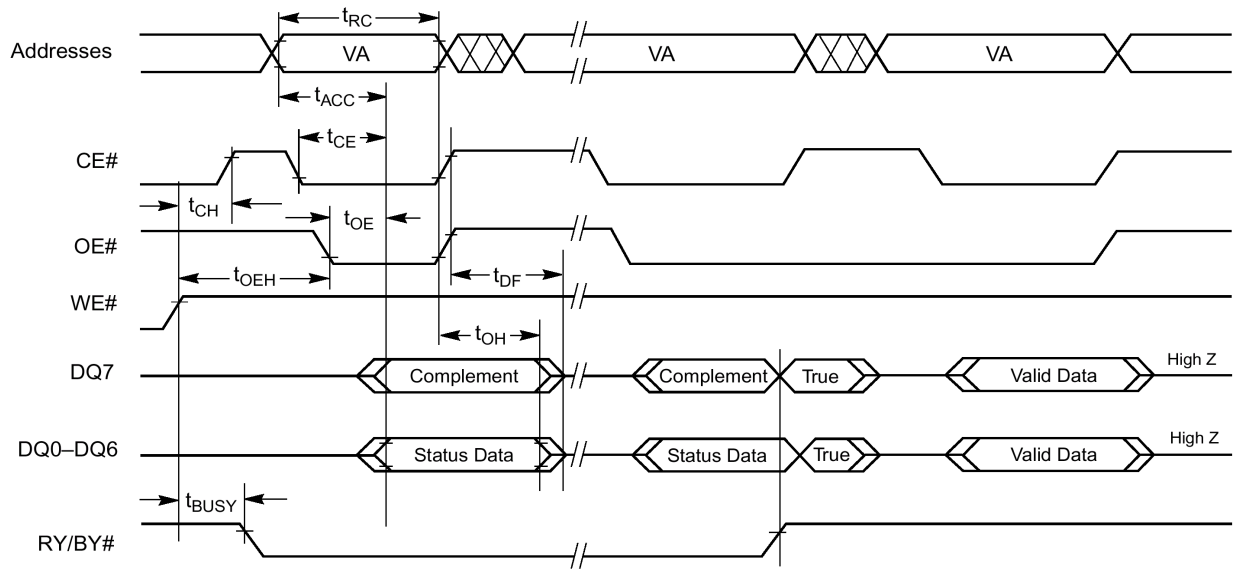
u PROGRAM OPERATIONS TIMING



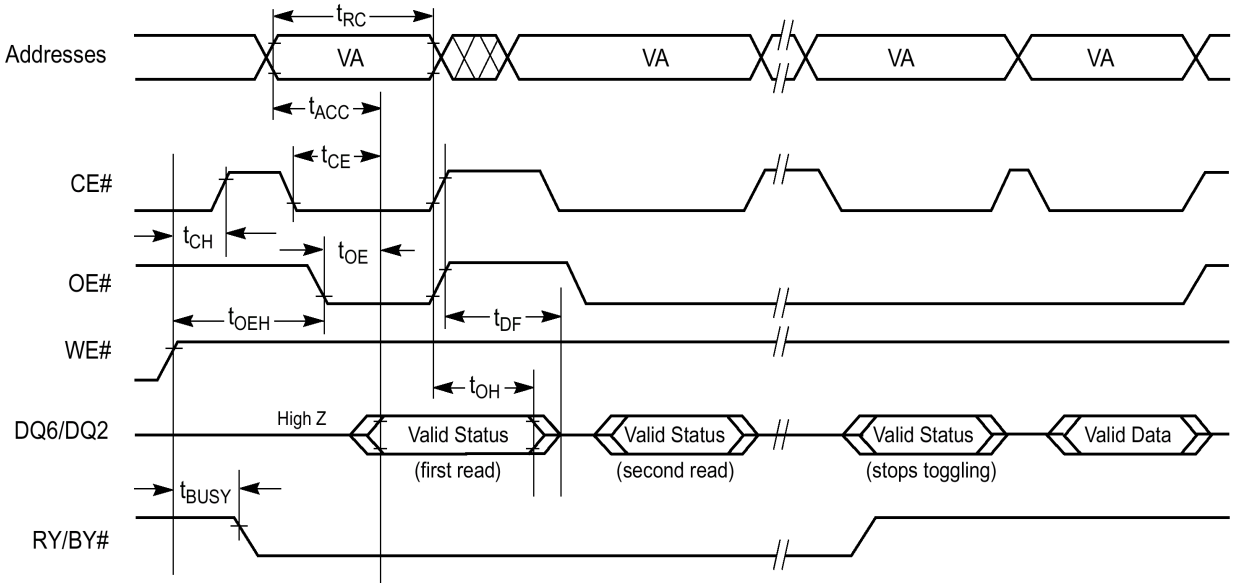
u CHIP/SECTOR ERASE OPERATION TIMINGS



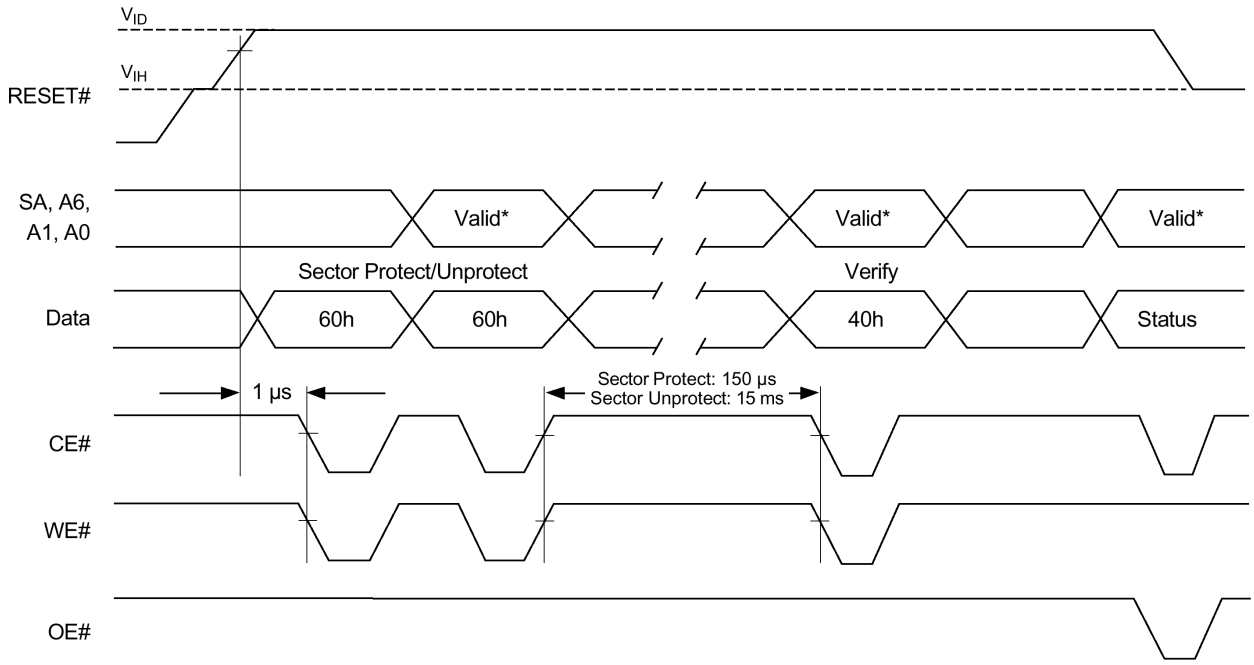
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



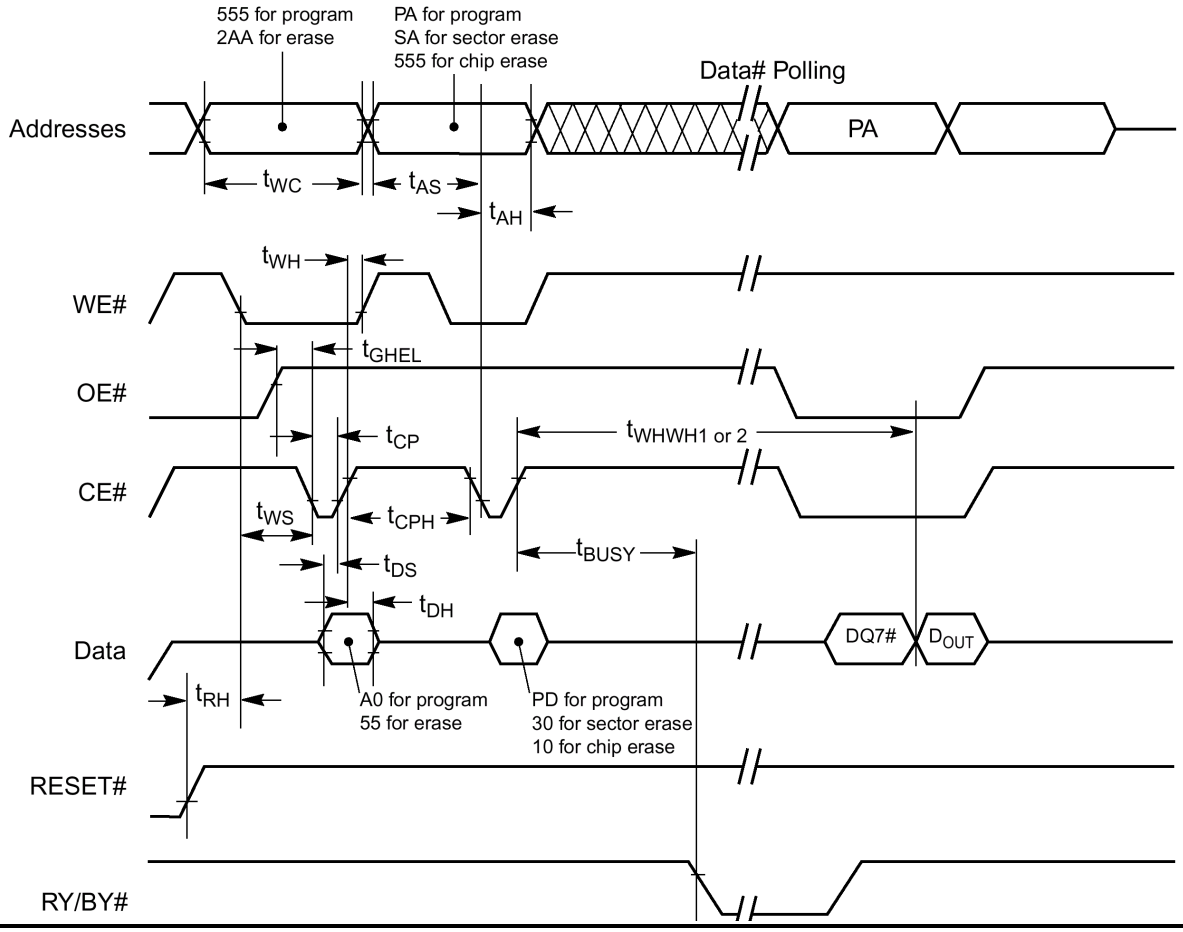
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

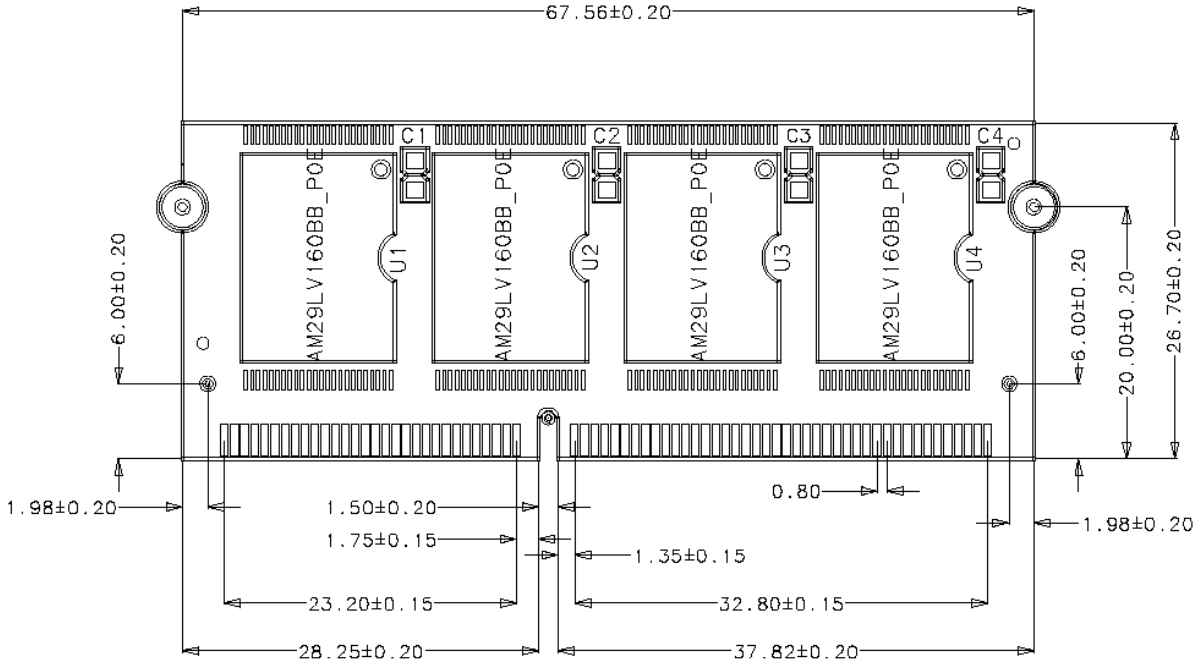


u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



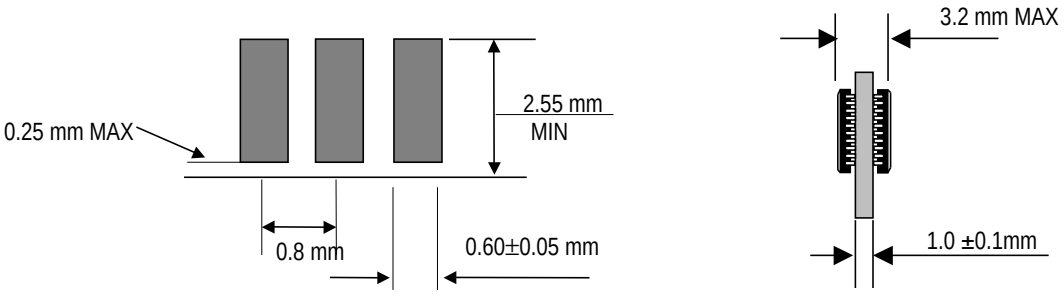
PACKAGE DIMENSIONS

Unit : mm



PCB Thickness: 1.0mm (1.0t - 1.1t)

Immersion Gold PCB Pattern



(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Components Composition	Vcc	SPEED
HMF4M32B8VN-70	16MByte	4MX 32bit	144 Pin-SODIMM	TSOP(2Mx8)*8	3.3V	70ns
HMF4M32B8VN-90	16MByte	4MX 32bit	144 Pin-SODIMM	TSOP(2Mx8)*8	3.3V	90ns
HMF4M32B8VN-120	16MByte	4MX 32bit	144 Pin-SODIMM	TSOP(2Mx8)*8	3.3V	120ns