



SANYO Semiconductors DATA SHEET

LC863448C,LC863440C
LC863432C,LC863428C
LC863424C,LC863420C
LC863416C

CMOS IC
 48K/40K/32K/28K/24K/20K/16K-byte ROM,
 CGROM16K-byte
 on-chip 640/512-byte RAM and 352x9 bit OSD RAM
8-bit 1-chip Microcontroller

Overview

The LC863448C/40C/32C/28C/24C/20C/16C are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424μs
- On-chip ROM capacity
 Program ROM : 48K/40K/32K/28K/24K/20K/16K bytes
 CGROM : 16K bytes
- On-chip RAM capacity : 640/512 bytes
- OSD RAM : 352x9 bits
- Closed-Caption TV controller and the on-screen display controller
- Closed-Caption data slicer
- Four channelsx6-bit AD Converter
- Three channelsx7-bit PWM
- 16-bit timer/counter, 14-bit base timer
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 12-source 8-vectored interrupt system
- Integrated system clock generator and display clock generator
 Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators
 TV control and the Closed Caption function

All of the above functions are fabricated on a single chip.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.

Purchase of SANYO IIC components conveys a license under the Philips IIC Patents Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

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LC863448C/40C/32C/28C/24C/20C/16C

Features

- Read-Only Memory (ROM) : 49152×8 bits / 40960×8 bits / 32768×8 bits /
28672×8 bits / 24576×8 bits / 20480×8 bits /
16384×8 bits for program
16128×8 bits for CGROM

 - Random Access Memory (RAM) : 512×8 bits (working area) : LC863448C/40C
384×8 bits (working area) : LC863432C/28C/24C/20C/16C
128×8 bits (working or ROM correction function)
352×9 bits (for CRT display)

 - OSD Functions
 - Screen display : 36 characters×16 lines (by software)
 - RAM : 352 words (9 bits per word)
Display area : 36 words×8 lines
Control area : 8 words×8 lines
 - Characters
Up to 252 kinds of 16×32 dot character fonts (4 characters including 1 test character are not programmable)
Each font can be divided into two parts and used as two fonts (Ex. 16×16 dot character font×2)
At least 111 characters need to be divide between a 16×17 dot and 8×9 dot character font to display the caption fonts.
 - Various character attributes
Character colors : 16colors (analog mode: 1Vp-p output) / 8colors (digital mode)
Character background colors : 16colors (analog mode: 1Vp-p output) / 8colors (digital mode)
Fringe / shadow colors : 16colors (analog mode: 1Vp-p output) / 8colors (digital mode)
Full screen colors : 16colors (analog mode: 1Vp-p output) / 8colors (digital mode)
Rounding
Underline
Italic character (slanting)
 - Attribute can be changed without spacing
 - Vertical display start line number can be set for each row independently (Rows can be overlapped)
 - Horizontal display start position can be set for each row independently
 - Horizontal pitch (9 to 16 dots)*1 and vertical pitch (1 to 32 dots) can be set for each row independently
 - Different display modes can be set for each row independently
Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplified graphic mode
 - Ten character sizes *1
Horez. × Vert. = (1×1), (1×2), (2×2), (2×4), (0.5×0.5)
(1.5×1), (1.5×2), (3×2), (3×4), (0.75×0.5)
 - Shuttering and scrolling on each row
 - Simplified Graphic Display
- Note *1: range depends on display mode : refer to the manual for details.
- Data Slicer (closed caption format)
 - Closed caption data and XDS data extraction
 - NTSC/PAL, and extracted line can be specified

■ Bus Cycle Time / Instruction-Cycle Time

Bus Cycle Time	Instruction Cycle Time	Clock Divider	System Clock Oscillation	Oscillation Frequency	Voltage
0.424μs	0.848μs	1/2	Internal VCO (Ref: X'tal 32.768kHz)	14.156MHz	4.5V to 5.5V
7.5μs	15.0μs	1/2	Internal RC	800kHz	4.5V to 5.5V
91.55μs	183.1μs	1/1	Crystal	32.768kHz	4.5V to 5.5V
183.1μs	366.2μs	1/2	Crystal	32.768kHz	4.5V to 5.5V

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■ Ports

- Input / Output Ports : 4 ports (23 terminals)
- Data direction programmable in nibble units : 1 port (8 terminals)
- (If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
- Data direction programmable for each bit individually: 3 ports (15 terminals)

■ AD Converter

- 4 channels×6-bit AD converters

■ Serial Interfaces

- IIC-bus compliant serial interface (Multi-master type)
- Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.

■ PWM Output

- 3 channels×7-bit PWM

■ Timer

- Timer 0 : 16-bit timer/counter
 - With 2-bit prescaler + 8-bit programmable prescaler
 - Mode 0 : Two 8-bit timers with a programmable prescaler
 - Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
 - Mode 2 : 16-bit timer with a programmable prescaler
 - Mode 3 : 16-bit counter
 - The resolution of timer is 1 tCYC.
- Base Timer
 - Generate every 500ms overflow for a clock application (using 32.768kHz crystal oscillation for the base timer clock)
 - Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow (using 32.768kHz crystal oscillation for the base timer clock)
 - Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0

■ Remote Control Receiver Circuit (connected to the P73/INT3/T0IN terminal)

- Noise rejection function
- Polarity switching

■ Watchdog Timer

External RC circuit is required
 Interrupt or system reset is activated when the timer overflows

■ ROM Correction Function

Max 128 bytes / 2 addresses

■ Interrupts

- 12 sources 8 vectored interrupts
 1. External Interrupt INT0
 2. External Interrupt INT1
 3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
 4. External Interrupt INT3, base timer
 5. Timer/counter T0H (Upper 8 bits)
 6. Data slicer
 7. Vertical synchronous signal interrupt (\overline{VS}), horizontal line (\overline{HS})
 8. IIC, Software
- Interrupt Priority Control
 - Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 8 listed above. For the external interrupt INT0 and INT1, low or highest priority can be set.

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■ Sub-routine Stack Level

- A maximum of 128 levels (stack is built in the internal RAM)

■ Multiplication/Division Instruction

- 16 bits×8 bits (7 instruction cycle times)
- 16 bits÷8 bits (7 instruction cycle times)

■ 3 Oscillation Circuits

- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

■ Standby Function

- HALT mode

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped.

This mode can be released by the interrupt request or the system reset.

- HOLD mode

The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.

- Pull the reset terminal ($\overline{\text{RES}}$) to low level.
- Feed the selected level to either P70/INT0 or P71/INT1.

■ Package

- MFP36SDJ (Lead-free type)
- DIP36S (Lead-free type)

■ Development Tools

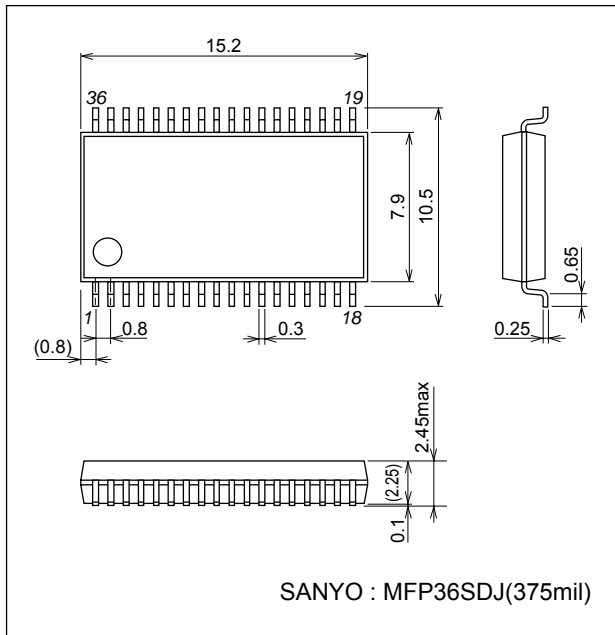
- Flash EEPROM: LC86F3448A
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863200A (evaluation chip board)
+ SUB863400A (sub board)
+ POD36-CABLE (cable)
+ POD36-DIP (for DIP36S)
or POD36-MFP (for MFP36SDJ)

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Package Dimensions

unit : mm (typ)

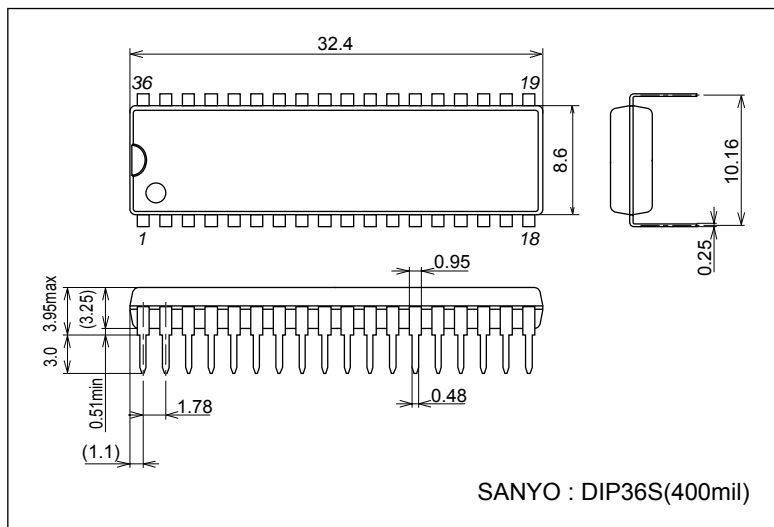
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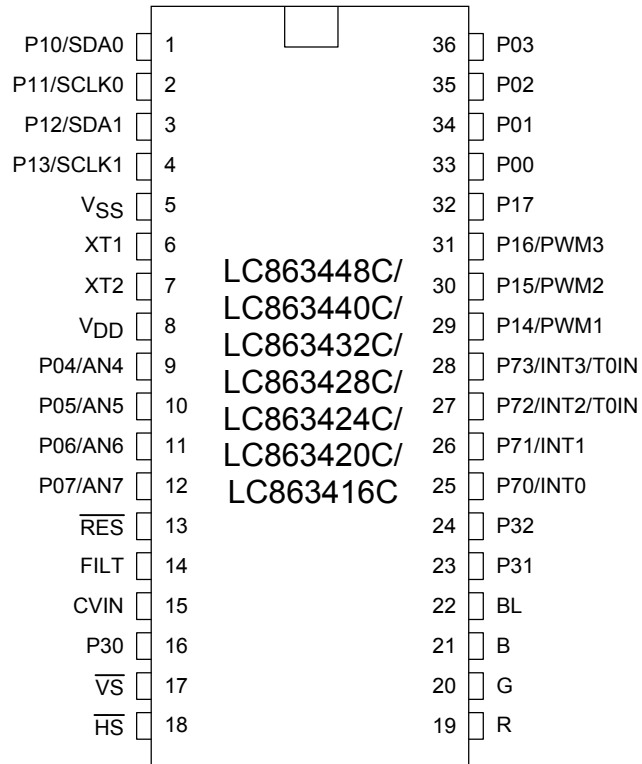


Package Dimensions

unit : mm (typ)

3170A

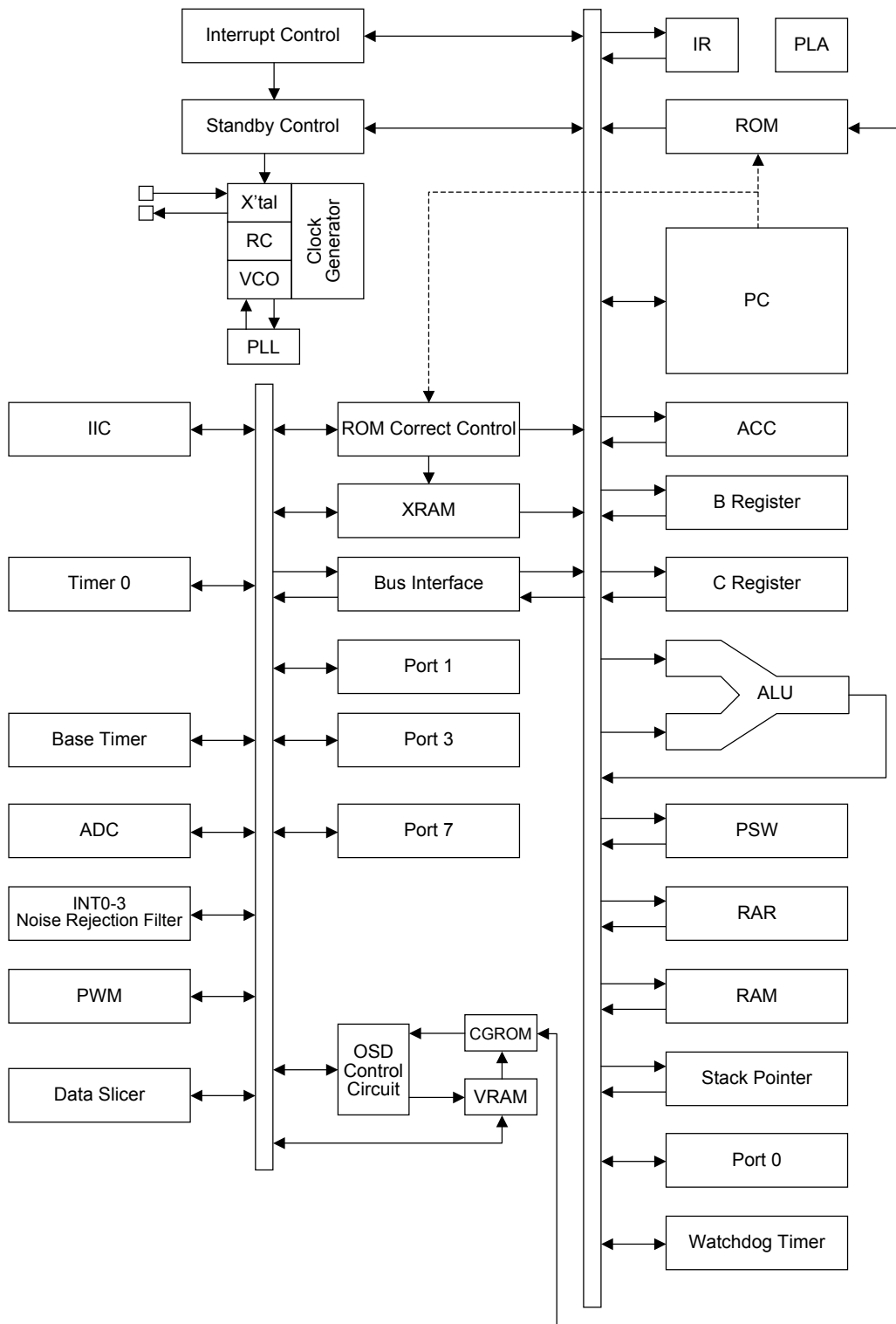


LC863448C/40C/32C/28C/24C/20C/16C**Pin Assignment**

Top view

SANYO: MFP36SDJ “Lead-free Type”
SANYO: DIP36S “Lead-free Type”

System Block Diagram



LC863448C/40C/32C/28C/24C/20C/16C

Pin Description

Pin Description Table

Terminal	I/O	Function Description	Option																																											
V _{SS}	-	Negative power supply																																												
XT1	I	Input terminal for crystal oscillator																																												
XT2	O	Output terminal for crystal oscillator																																												
V _{DD}	-	Positive power supply																																												
RES	I	Reset terminal																																												
FILT	O	Filter terminal for PLL																																												
CVIN	I	Video signal input terminal																																												
V _S	I	Vertical synchronization signal input terminal																																												
H _S	I	Horizontal synchronization signal input terminal																																												
R	O	Red (R) output terminal of RGB image output																																												
G	O	Green (G) output terminal of RGB image output																																												
B	O	Blue (B) output terminal of RGB image output																																												
BL	O	Fast blanking control signal Switch TV image signal and caption/OSD image signal																																												
Port 0 P00 to P07	I/O	<ul style="list-style-type: none"> •8-bit input/output port, Input/output can be specified in nibble unit (If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.) •Other functions AD converter input port (P04 to P07: 4 channels) 	Pull-up resistor provided/not provided Output Format CMOS/Nch-OD																																											
Port 1 P10 to P17	I/O	<ul style="list-style-type: none"> •8-bit input/output port Input/output can be specified for each bit (programmable pull-up resistor provided) •Other functions <table border="1" style="margin-left: 20px;"> <tr><td>P10</td><td>IIC0 data I/O</td></tr> <tr><td>P11</td><td>IIC0 clock output</td></tr> <tr><td>P12</td><td>IIC1 data I/O</td></tr> <tr><td>P13</td><td>IIC1 clock output</td></tr> <tr><td>P14</td><td>PWM1 output</td></tr> <tr><td>P15</td><td>PWM2 output</td></tr> <tr><td>P16</td><td>PWM3 output</td></tr> </table>	P10	IIC0 data I/O	P11	IIC0 clock output	P12	IIC1 data I/O	P13	IIC1 clock output	P14	PWM1 output	P15	PWM2 output	P16	PWM3 output	Output Format CMOS/Nch-OD																													
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P15	PWM2 output																																													
P16	PWM3 output																																													
Port 3 P30 to P32	I/O	<ul style="list-style-type: none"> •3-bit input/output port Input/output can be specified for each bit (CMOS output/input with programmable pull-up resistor) 																																												
Port 7 P70 P71 to P73	I/O	<ul style="list-style-type: none"> •4-bit input/output port Input or output can be specified for each bit <div style="border: 1px solid black; padding: 5px; margin: 5px 0;"> P70: I/O with programmable pull-up resistor P71 to P73: CMOS output/input with programmable pull-up resistor </div> •Other functions <table border="1" style="margin-left: 20px;"> <tr><td>P70</td><td>INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer</td></tr> <tr><td>P71</td><td>INT1 input/HOLD release input</td></tr> <tr><td>P72</td><td>INT2 input/Timer 0 event input</td></tr> <tr><td>P73</td><td>INT3 input (noise rejection filter connected)/ Timer 0 event input</td></tr> </table> <p style="margin-left: 20px;">Interrupt receiver format, vector addresses</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising/ Falling</th> <th>H level</th> <th>L level</th> <th>Vector</th> </tr> </thead> <tbody> <tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr> <tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr> <tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr> <tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr> </tbody> </table>	P70	INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer	P71	INT1 input/HOLD release input	P72	INT2 input/Timer 0 event input	P73	INT3 input (noise rejection filter connected)/ Timer 0 event input		Rising	Falling	Rising/ Falling	H level	L level	Vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	
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INT3	enable	enable	enable	disable	disable	1BH																																								

Note: A capacitor of at least 10 μ F must be inserted between V_{DD} and V_{SS} when using this IC.

LC863448C/40C/32C/28C/24C/20C/16C

- Output form and existence of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.
- Port status in reset

Terminal	I/O	Pull-up resistor status at selecting CMOS output option
Port 0	I	Pull-up resistor OFF, ON after reset release
Port 1	I	Programmable pull-up resistor OFF

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter		Symbol	Pins	Conditions	$V_{DD}[\text{V}]$	Ratings			unit	
						min	typ	max		
Maximum supply voltage		$V_{DD \text{ max}}$	V_{DD}			-0.3		+6.5	V	
Input voltage		$V_I(1)$	\overline{RES} , \overline{HS} , \overline{VS} , $CVIN$			-0.3		$V_{DD}+0.3$		
Output voltage		$V_O(1)$	R, G, B, BL, FILT			-0.3		$V_{DD}+0.3$		
Input/output voltage		V_{IO}	Ports 0, 1, 3, 7			-0.3		$V_{DD}+0.3$		
High level output current	Peak output current	$IO_{PH}(1)$	Ports 0, 1, 3, 7	•CMOS output •For each pin.		-4			mA	
		$IO_{PH}(2)$	R, G, B, BL	•CMOS output •For each pin.		-5				
	Total output current	$\Sigma IO_{AH}(1)$	Ports 0, 1	Total of all pins.			-20			
		$\Sigma IO_{AH}(2)$	Ports 3, 7	Total of all pins.			-10			
$\Sigma IO_{AH}(3)$		R, G, B, BL	Total of all pins.			-12				
Low level output current	Peak output current	$IO_{PL}(1)$	Ports 0, 1, 3	For each pin.				20		
		$IO_{PL}(2)$	Port 7	For each pin.				15		
		$IO_{PL}(3)$	R, G, B, BL	For each pin.				5		
	Total output current	$\Sigma IO_{AL}(1)$	Ports 0, 1	Total of all pins.						40
		$\Sigma IO_{AL}(2)$	Ports 3, 7	Total of all pins.						20
		$\Sigma IO_{AL}(3)$	R, G, B, BL	Total of all pins.					12	
Maximum power dissipation	$P_d \text{ max}$	MFP36SDJ	Ta=-10 to +70°C					360	mW	
		DIP36S						610		
Operating temperature range	T_{opr}					-10		+70	°C	
Storage temperature range	T_{stg}					-55		+125		

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Recommended Operating Range at $T_a = -10^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				$V_{DD}[\text{V}]$	min	typ		max
Operating supply voltage range	$V_{DD}(1)$	V_{DD}	$0.844\mu\text{s} \leq t_{CYC} \leq 0.852\mu\text{s}$		4.5		5.5	V
	$V_{DD}(2)$		$4\mu\text{s} \leq t_{CYC} \leq 400\mu\text{s}$		4.5		5.5	
Hold voltage	VHD	V_{DD}	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Port 0	Output disable	4.5 to 5.5	$0.6V_{DD}$		V_{DD}	
	$V_{IH}(2)$	•Ports 1, 3 (Schmitt) •Port 7 (Schmitt) port input/interrupt • \overline{HS} , \overline{VS} , \overline{RES} (Schmitt)	Output disable	4.5 to 5.5	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(3)$	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	$V_{DD}-0.5$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Port 0	Output disable	4.5 to 5.5	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	•Ports 1, 3 (Schmitt) •Port 7 (Schmitt) port input/interrupt • \overline{HS} , \overline{VS} , \overline{RES} (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(3)$	Port 70 Watchdog timer input	Output disable	4.5 to 5.5	V_{SS}		$0.6V_{DD}$	
CVIN	VCVIN	CVIN		5.0	$0.7V_{p-p}$	$1V_{p-p}$	$1.4V_{p-p}$	V_{p-p}^*
Operation cycle time	$t_{CYC}(1)$		•All functions operating	4.5 to 5.5	0.844	0.848	0.852	μs
	$t_{CYC}(2)$		•OSD and Data slicer are not operating	4.5 to 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 to 5.5	0.4	0.8	3.0	MHz

* V_{p-p} : Peak-to-peak voltage

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Electrical Characteristics at Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min	typ		max
High level input current	I _{IH} (1)	Ports 0, 1, 3, 7	•Output disable •Pull-up MOS Tr. OFF •V _{IN} =V _{DD} (including the off-leak current of the output Tr.)	4.5 to 5.5			1	μA
	I _{IH} (2)	• \overline{RES} • \overline{FS} , \overline{VS}	•V _{IN} =V _{DD}	4.5 to 5.5			1	
Low level input current	I _{IL} (1)	Ports 0, 1, 3, 7	•Output disable •Pull-up MOS Tr. OFF •V _{IN} =V _{SS} (including the off-leak current of the output Tr.)	4.5 to 5.5	-1			
	I _{IL} (2)	• \overline{RES} • \overline{FS} , \overline{VS}	V _{IN} =V _{SS}	4.5 to 5.5	-1			
High level output voltage	V _{OH} (1)	•CMOS output of ports 0, 1, 3, 71 to 73	I _{OH} =-1.0mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)	R, G, B, BL	I _{OH} =-0.1mA R, G, B: digital mode	4.5 to 5.5	V _{DD} -0.5			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 3, 71 to 73	I _{OL} =10mA	4.5 to 5.5			1.5	V
	V _{OL} (2)	Ports 0, 3, 71 to 73	I _{OL} =1.6mA	4.5 to 5.5			0.4	
	V _{OL} (3)	•R, G, B, BL •Port 1	I _{OL} =3.0mA R, G, B: digital mode	4.5 to 5.5			0.4	
	V _{OL} (4)	Port 70	I _{OL} =1mA	4.5 to 5.5			0.4	
Pull-up MOS Tr. resistance	R _{pu}	Ports 0, 1, 3, 7	V _{OH} =0.9V _{DD}	4.5 to 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1)	RBS	•P10 to P12 •P11 to P13		4.5 to 5.5		130	300	Ω
Hysteresis voltage	VHYS	•Ports 1, 3, 7 • \overline{RES} • \overline{FS} , \overline{VS}	Output disable	4.5 to 5.5		0.1V _{DD}		V
Input clump voltage	VCLMP	CVIN		5.0	2.3	2.5	2.7	
Pin capacitance	CP	All pins	•f=1MHz •Every other terminals are connected to V _{SS} . •Ta=25°C	4.5 to 5.5		10		pF

LC863448C/40C/32C/28C/24C/20C/16C

IIC Input/Output Conditions at Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Standard		High speed		unit
		min	max	min	max	
SCL Frequency	fSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7	-	1.3	-	μs
HOLD time of start, restart condition	tHD;STA	4.0	-	0.6	-	μs
L time of SCL	tLOW	4.7	-	1.3	-	μs
H time of SCL	tHIGH	4.0	-	0.6	-	μs
Set-up time of restart condition	tSU;STA	4.7	-	0.6	-	μs
HOLD time of SDA	tHD;DAT	0	-	0	0.9	μs
Set-up time of SDA	tSU;DAT	250	-	100	-	ns
Rising time of SDA, SCL	tR	-	1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	tF	-	300	20+0.1Cb	300	ns
Set-up time of stop condition	tSU;STO	4.0	-	0.6	-	μs

Refer to figure 8

Note 1: Cb: Total capacitance of all BUS (unit : pF)

Pulse Input Conditions at Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (1tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (16tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	32			
	tPIH(4) tPIL(4)	INT3/T0IN (64tCYC is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	128			
	tPIL(5)	RES	Reset acceptable	4.5 to 5.5	200			μs
tPIH(6) tPIL(6)	HS, VS	•Display position controllable •The active edge of HS and VS must be apart at least 1tCYC. •Refer to figure 4.	4.5 to 5.5	3				
Rising/falling time	tTHL tTLH	HS	Refer to figure 4.	4.5 to 5.5			500	ns

AD Converter Characteristics at Ta = -10°C to +70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit	
					min	typ	max		
Resolution	N			4.5 to 5.5		6		bit	
Absolute precision	ET		(Note 2)				±1		LSB
Conversion time	tCAD	Vref selection to conversion finish	1 bit conversion time=2×Tcyc				1.69		μs
Analog input voltage range	VAIN	AN4 to AN7				VSS		VDD	V
Analog port input current	IAINH IAINL		VAIN=VDD VAIN=VSS					1	μA
					-1				

Note 2: Absolute precision does not include quantizing error (1/2LSB).

LC863448C/40C/32C/28C/24C/20C/16C**Analog Mode RGB Characteristics** at Ta = -10°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Ratings				
				V _{DD} [V]	min.	typ.	max.	unit
Analog output voltage		R.G.B Analog output mode	Low level output	5.0	0.45	0.5	0.55	V
			Intensity output		0.90	1.0	1.10	
			Hi level output		1.35	1.5	1.65	
Time setting		R.G.B	70% 10pf load				50	ns

Sample Current Dissipation Characteristics at Ta = -10°C to +70°C, V_{SS} = 0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally.

The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				V _{DD} [V]	min	typ		max
Current dissipation during basic operation (Note 3)	IDDOP(1)	V _{DD}	•FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD operating •OSD is Digital mode •Internal RC oscillation stops	4.5 to 5.5		11	25	mA
	IDDOP(2)	V _{DD}	•FmX'tal=32.768kHz X'tal scillation •System clock : VCO •VCO for OSD operating •OSD is Analog mode •Internal RC oscillation stops	4.5 to 5.5		20	35	
	IDDOP(3)	V _{DD}	•FmX'tal=32.768kHz X'tal scillation •System clock : X'tal (Instruction cycle time: 366.2μs) •VCO for system VCO for OSD, internal RC oscillation stop •Data slicer, AD converters stop	4.5 to 5.5		65	300	μA
Current dissipation in HALT mode (Note 3)	IDDHALT(1)	V _{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •System clock : VCO •VCO for OSD stops •Internal RC oscillation stops	4.5 to 5.5		3	9	mA
	IDDHALT(2)	V _{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : Internal RC	4.5 to 5.5		300	1000	
	IDDHALT(3)	V _{DD}	•HALT mode •FmX'tal=32.768kHz X'tal oscillation •VCO for system stops •VCO for OSD stops •System clock : X'tal (Instruction cycle time: 366.2μs)	4.5 to 5.5		57	200	μA
Current dissipation in HOLD mode (Note 3)	IDDHOLD	V _{DD}	•HOLD mode •All oscillation stops.	4.5 to 5.5		0.05	20	μA

Note 3: The currents through the output transistors and the pull-up MOS transistors are ignored.

LC863448C/40C/32C/28C/24C/20C/16C

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.

Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10°C to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ	max	
32.768kHz	SEIKO EPSON	C-002RX	18pF	18pF	OPEN	390kΩ	4.5 to 5.5V	1.0s	1.5s	

Notes: The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The V_{DD} becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' V_{SS} should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

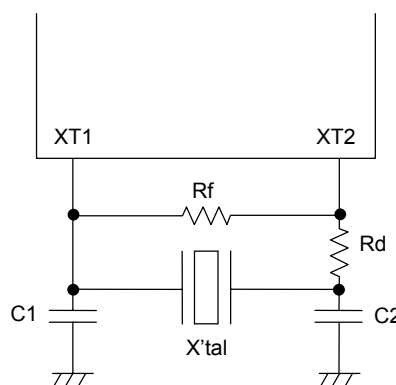
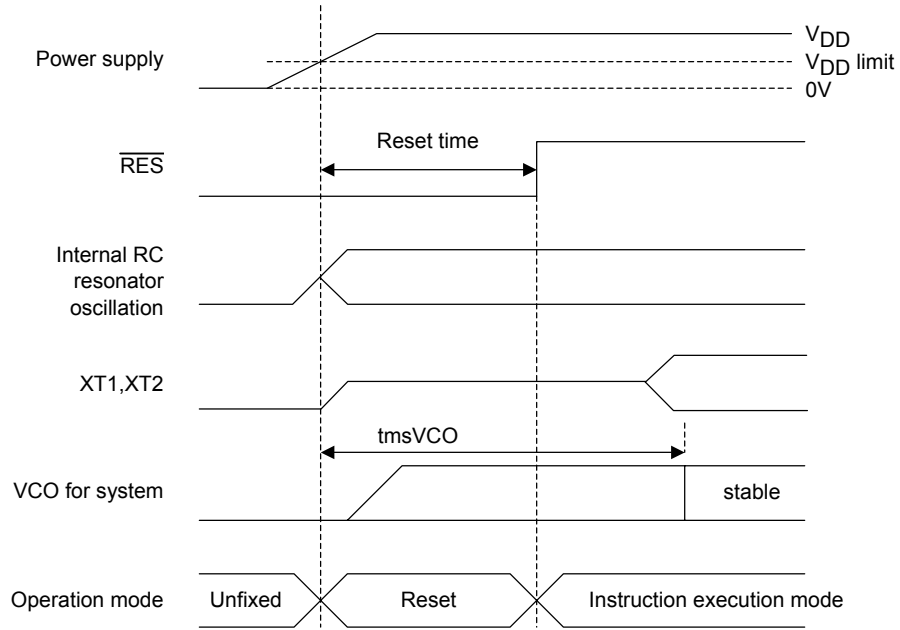
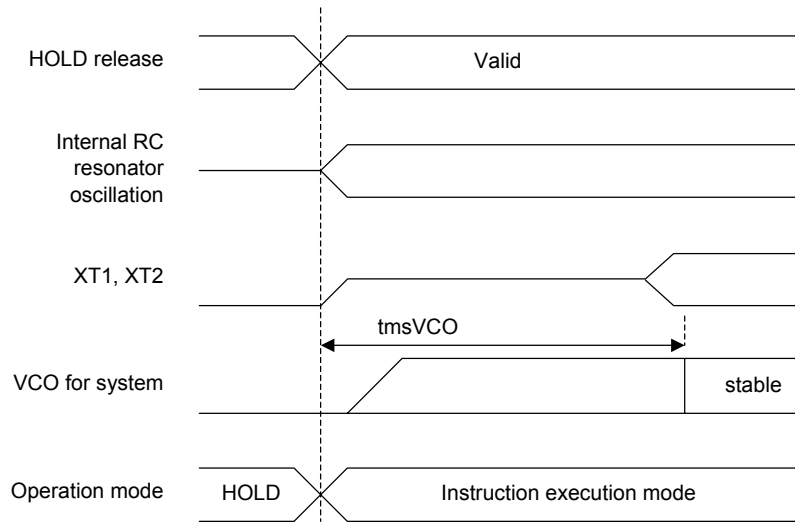


Figure 1 Recommended Oscillation Circuit



Reset Time and Oscillation Stabilizing Time



HOLD Release Signal and Oscillation Stabilizing Time

Figure 2 Oscillation Stabilizing Time

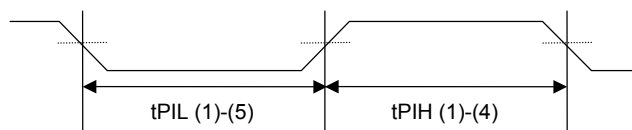


Figure 3 Pulse Input Timing Condition - 1

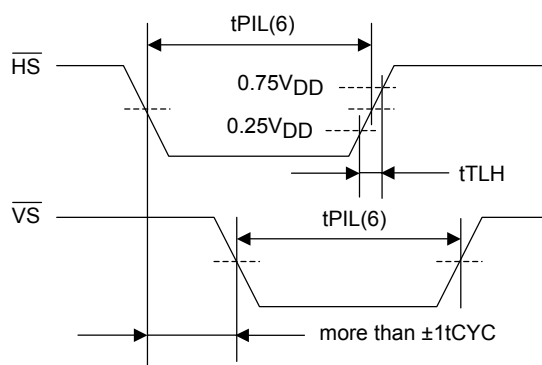


Figure 4 Pulse Input Timing Condition - 2

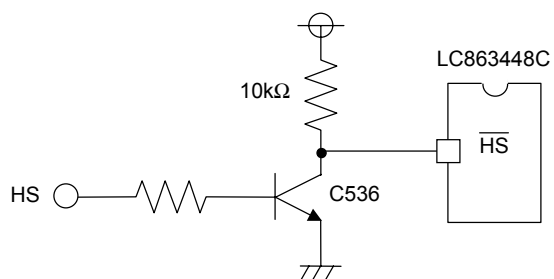
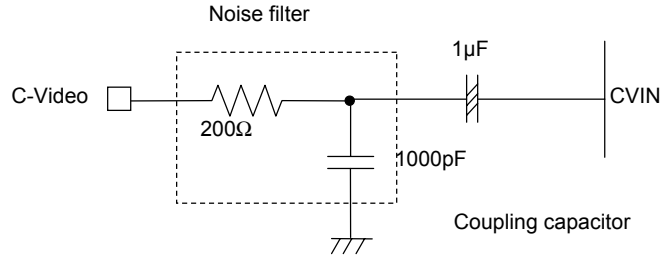


Figure 5 Recommended Interface Circuit

LC863448C/40C/32C/28C/24C/20C/16C



Output impedance of C-Video before Noise filter should be less then 100Ω.

Figure 6 CVIN Recommended Circuit

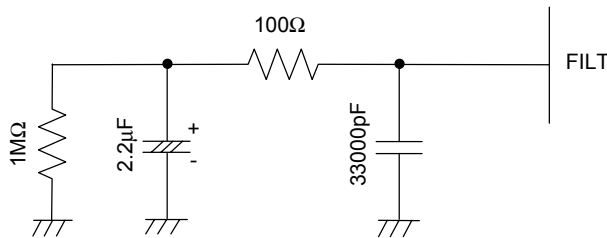
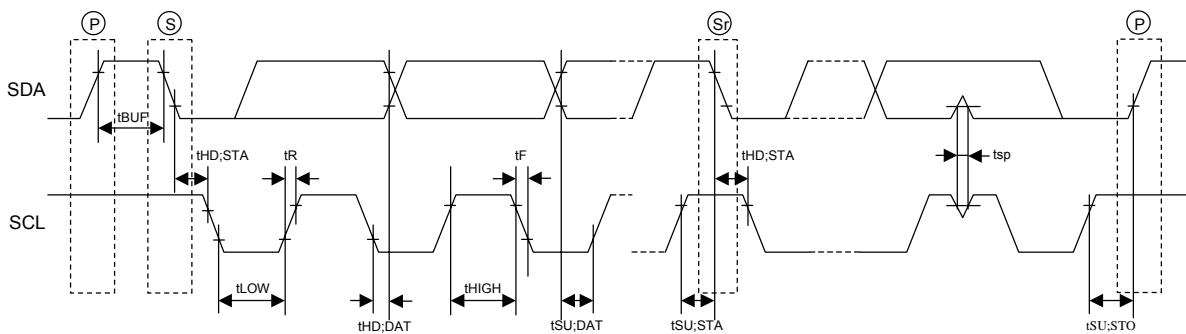


Figure 7 FILT Recommended Circuit

Note: Place FILT parts on board as close to the microcontroller as possible.



S : start condition
P : stop condition
Sr : restart condition

tsp : spike suppression

Standard mode : not exist
High speed mode : less than 50ns

Figure 8 IIC Timing

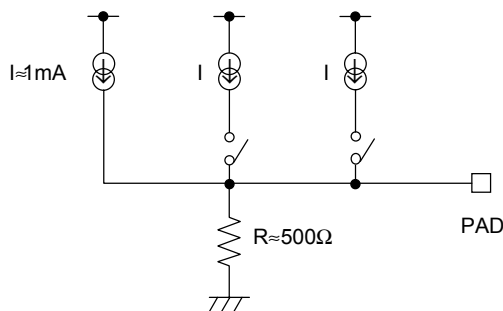


Figure 9 R.G.B. Analog Output Equivalent Circuit

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