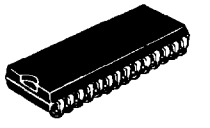
HM571000 Series

1,048,576-Word x 1-Bit High Speed Dynamic Random Access Memory

■ DESCRIPTION

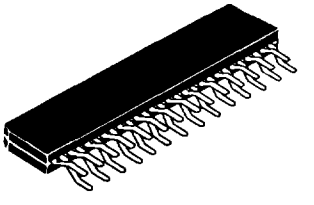
The Hitachi HM571000 is a super high speed dynamic RAM organized 1,048,576-word x 1-bit. HM571000 have realized higher density, higher performance and various functions by employing 1.3 μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM571000 offers 8 bits static column mode as a high speed access mode.

HM571000JP Series



(CP-28DN)

HM571000ZP Series



(ZP-28)

■ FEATURES

- Single
  - 5V (±10%) for HM571000JP/ZP-40/45
  - 5V (±5%) for HM571000JP/ZP-35R
- High Speed
  - Access Time .....35 ns/40 ns/45 ns (max)
- 512 Refresh Cycles .....(4 ms)
- 2 Variations of Refresh
  - $\overline{CE}$ Refresh
  - Automatic Refresh
- 8 Bits Static Column Mode

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM571000JP-35R HM571000JP-40 HM571000JP-45	35 ns 40 ns 45 ns	300 mil 28-pin Plastic SOJ (CP-28DN)
HM571000ZP-35*1 HM571000ZP-40*1 HM571000ZP-45*1	35 ns 40 ns 45 ns	400 mil 28-pin Plastic ZIP (ZP-28)

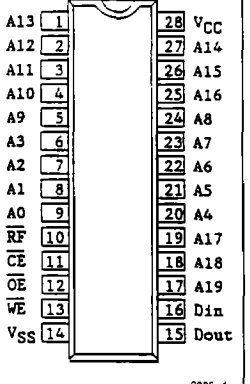
Note: *1. ZIP type products are preliminary.

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input for $\overline{CE}$ Refresh
A_9–A_{16}	Address Input
A_{17}–A_{19}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
D_{in}	Data-in
D_{out}	Data-out
$\overline{RF}$	Refresh Control
V_{CC}	Power (+5V)
V_{SS}	Ground

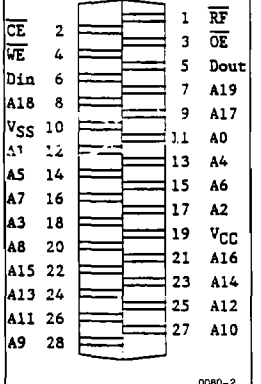
■ PIN OUT

HM571000JP Series



(Top View)

HM571000ZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	-35R	V_{CC}	4.75	5.0	5.25	V	1
	-40/-45		4.50		5.50		
Input High Voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input Low Voltage		V_{IL}	− 1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the − 2V level with a maximum pulse width of 20 ns at the − 1.5V level. (See Figure 1.)

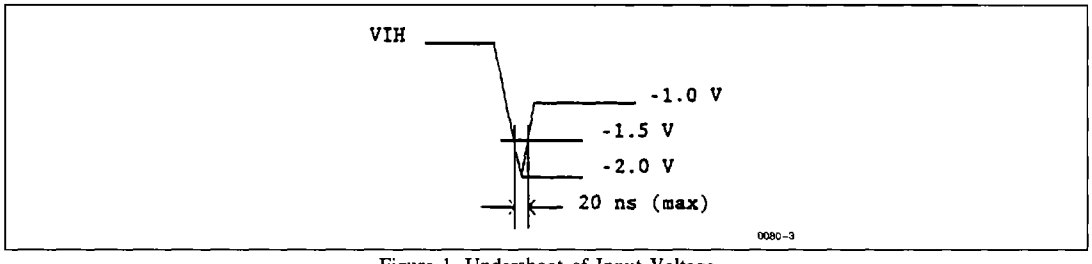


Figure 1. Undershoot of Input Voltage

3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} + 0.5V.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{SS} = 0V)

(V_{CC} = 5V ± 10% for HM571000JP-40/45)
(V_{CC} = 5V ± 5% for HM571000JP-35R)

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Normal Operating Current	I_{CCA}	See Figure 2						mA		1
Refresh Current	I_{CCR}	See Figure 2						mA		1
Standby Current	I_{CCS}	—	5	—	5	—	5	mA		
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V < V_{in} < 7V	2
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V < V_{out} < 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 4 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 8 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. The V_{IN} level of $\overline{OE}$ that is I_{LI} test condition of $\overline{OE}$ must be lower than V_{CC} + 0.5V.

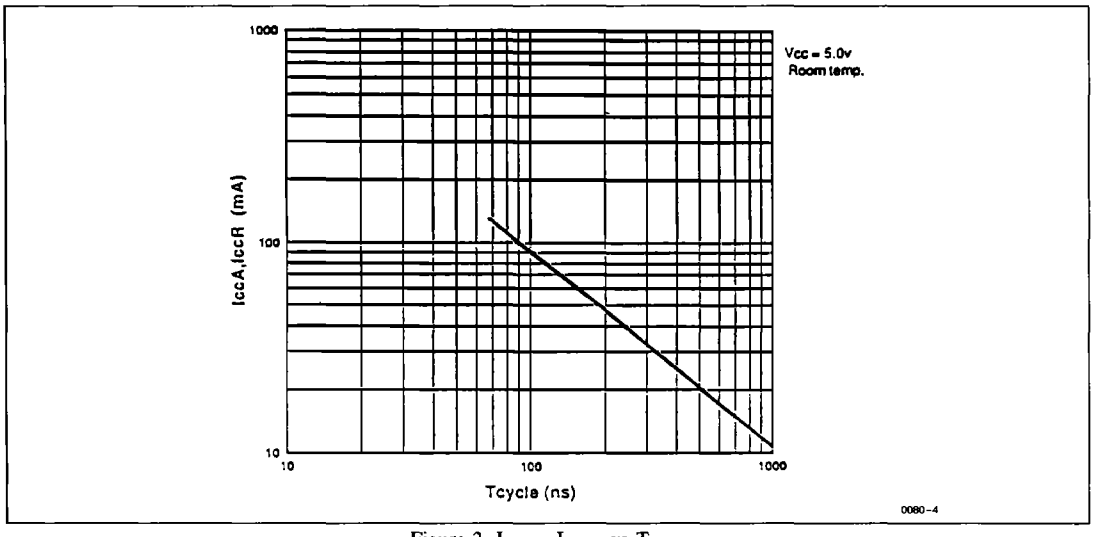


Figure 2. I_{CCA}, I_{CCR} vs T_{cycle}

• **Capacitance** (T_A = 25°C)
(V_{CC} = 5V ±10% for HM571000JP-40/45)
(V_{CC} = 5V ± 5% for HM571000JP-35R)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data-in	C_{in1}	—	5	pF	1
	Clocks ($\overline{CE}$, $\overline{OE}$)	C_{in2}	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	C_{in3}	—	7	pF	1
Output Capacitance	(Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

• **AC CHARACTERISTICS** [1] (T_A = 0 to +70°C, V_{SS} = 0V)
(V_{CC} = 5V ±10% for HM571000JP/40/45)
(V_{CC} = 5V ±5% for HM571000JP/35R)

Test Conditions

Input Pulse Levels: V_{IH} = 3.0V, V_{IL} = 0V
Transition Time: t_T = 3 ns
Input Timing Reference Levels: High = 2.4V, Low = 0.8V (See Figure 3.)
Output Timing Reference Levels: High = 2.4V, Low = 0.4V
Output Load: See Figure 4.

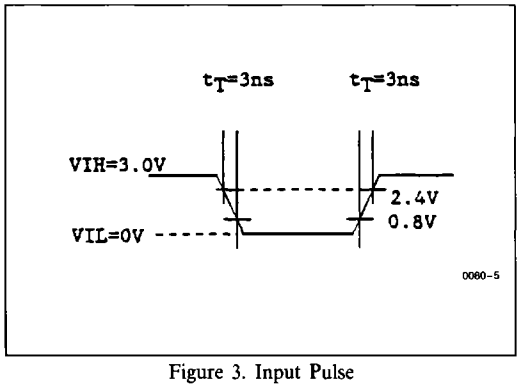


Figure 3. Input Pulse

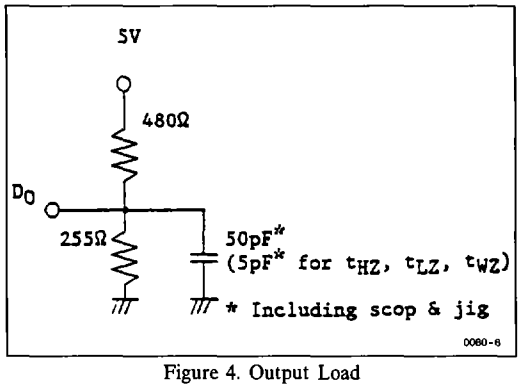


Figure 4. Output Load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read/Write Cycle Time	t_{CC}	75	—	85	—	90	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ Precharge Time	t_{CP}	34	—	39	—	39	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	10	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

Read Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time on Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time from Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Output in High-Z	t_{WZ}	—	15	—	20	—	20	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ Delay Time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

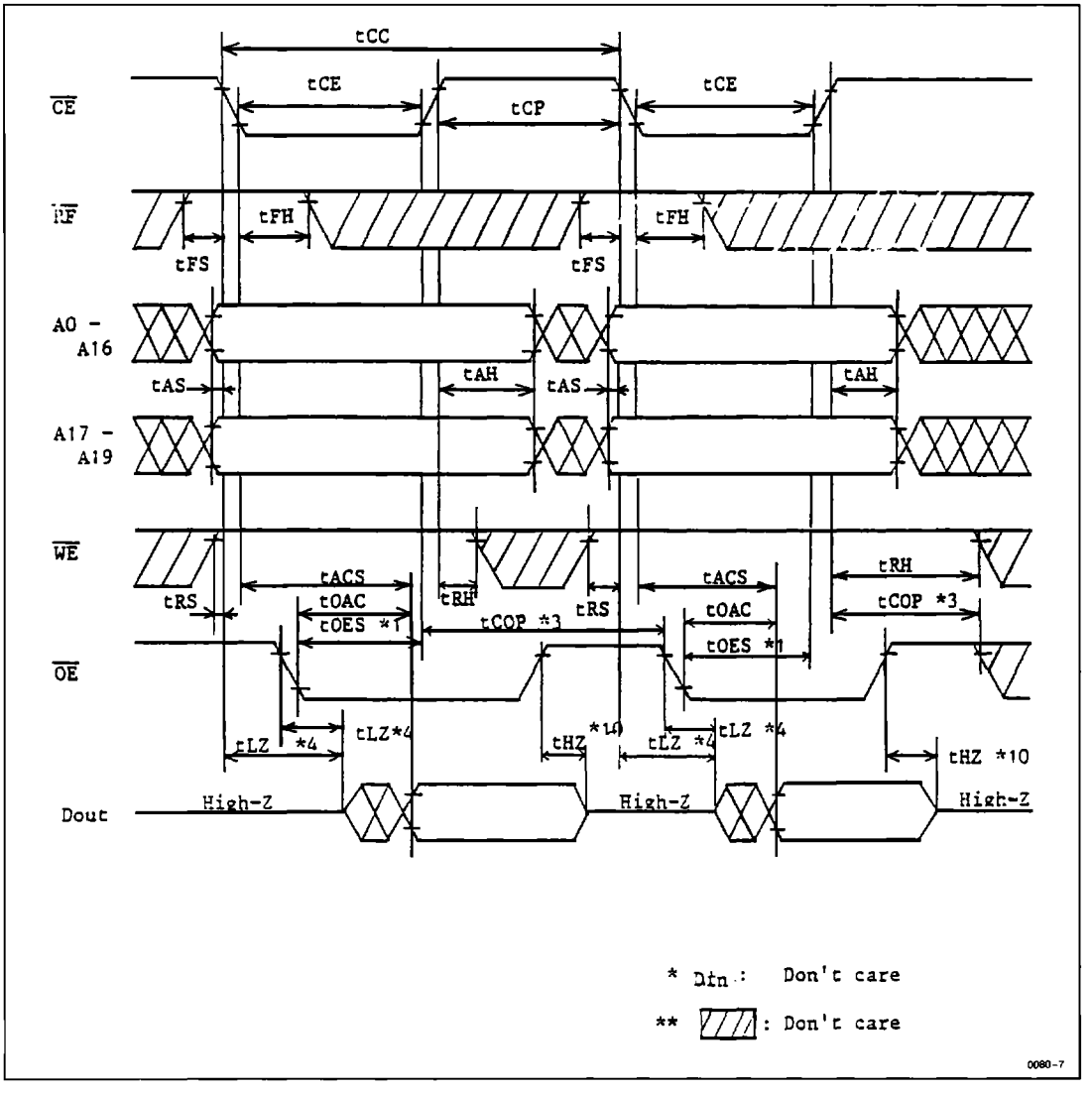
Static Column Mode Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

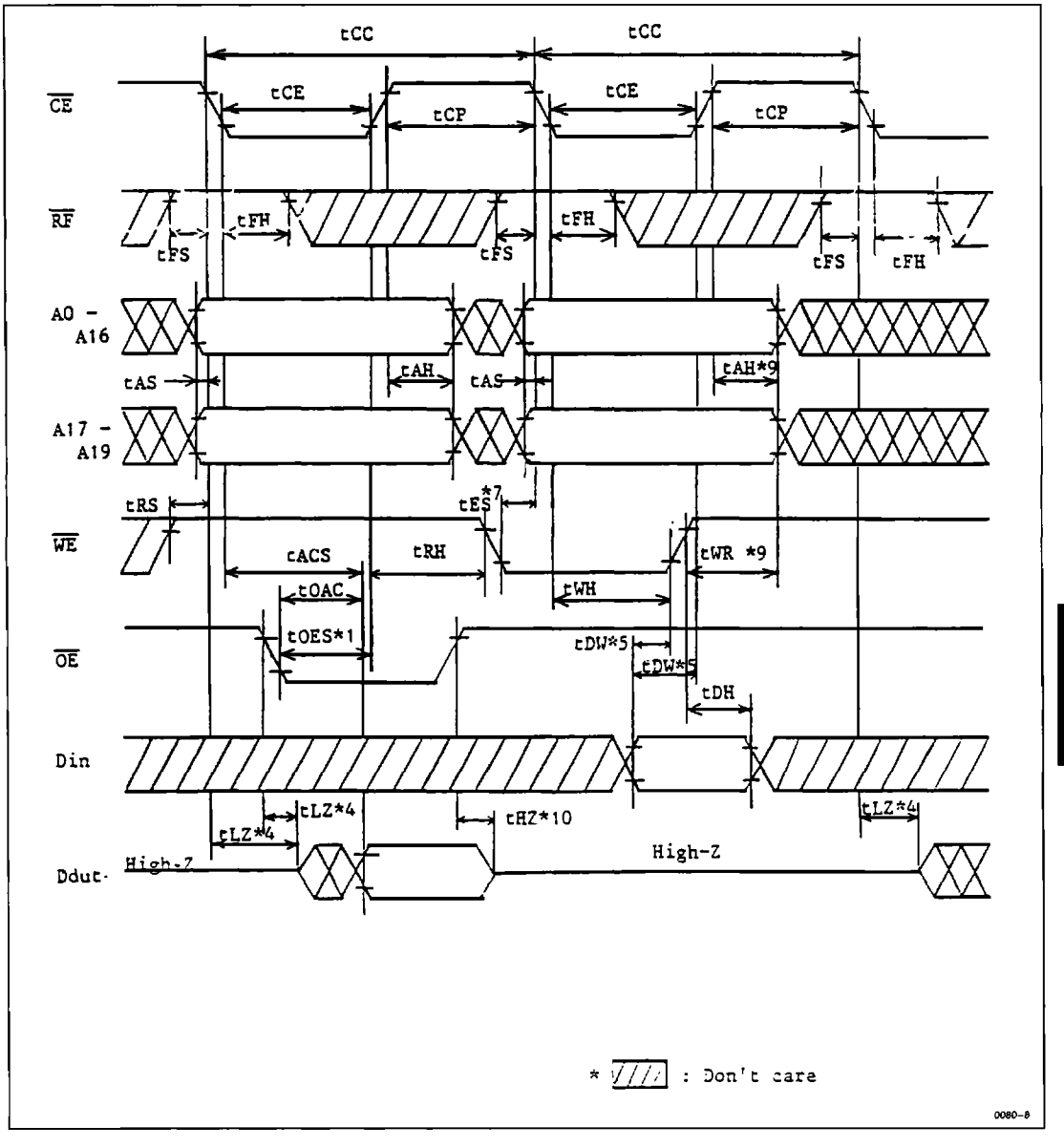
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisified for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), D_{out} cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisified for a write cycle.
10. t_{HZ} defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μS is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. In static column mode cycle, there must not be any invalid address inputs for static column mode (A_{17}–A_{19}) which are less than t_{AA}.

■ TIMING WAVEFORMS

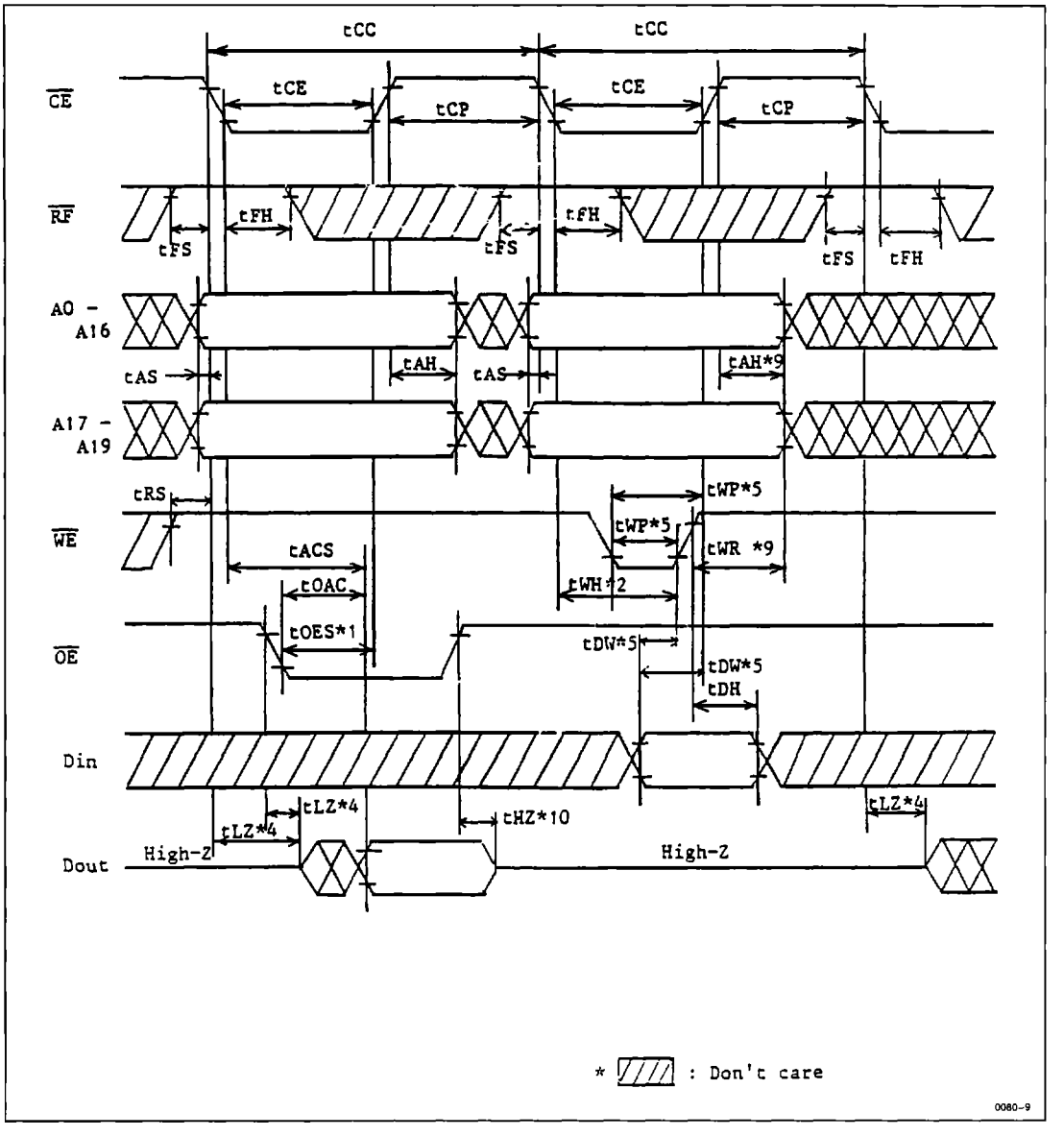
• Read/Read Cycle



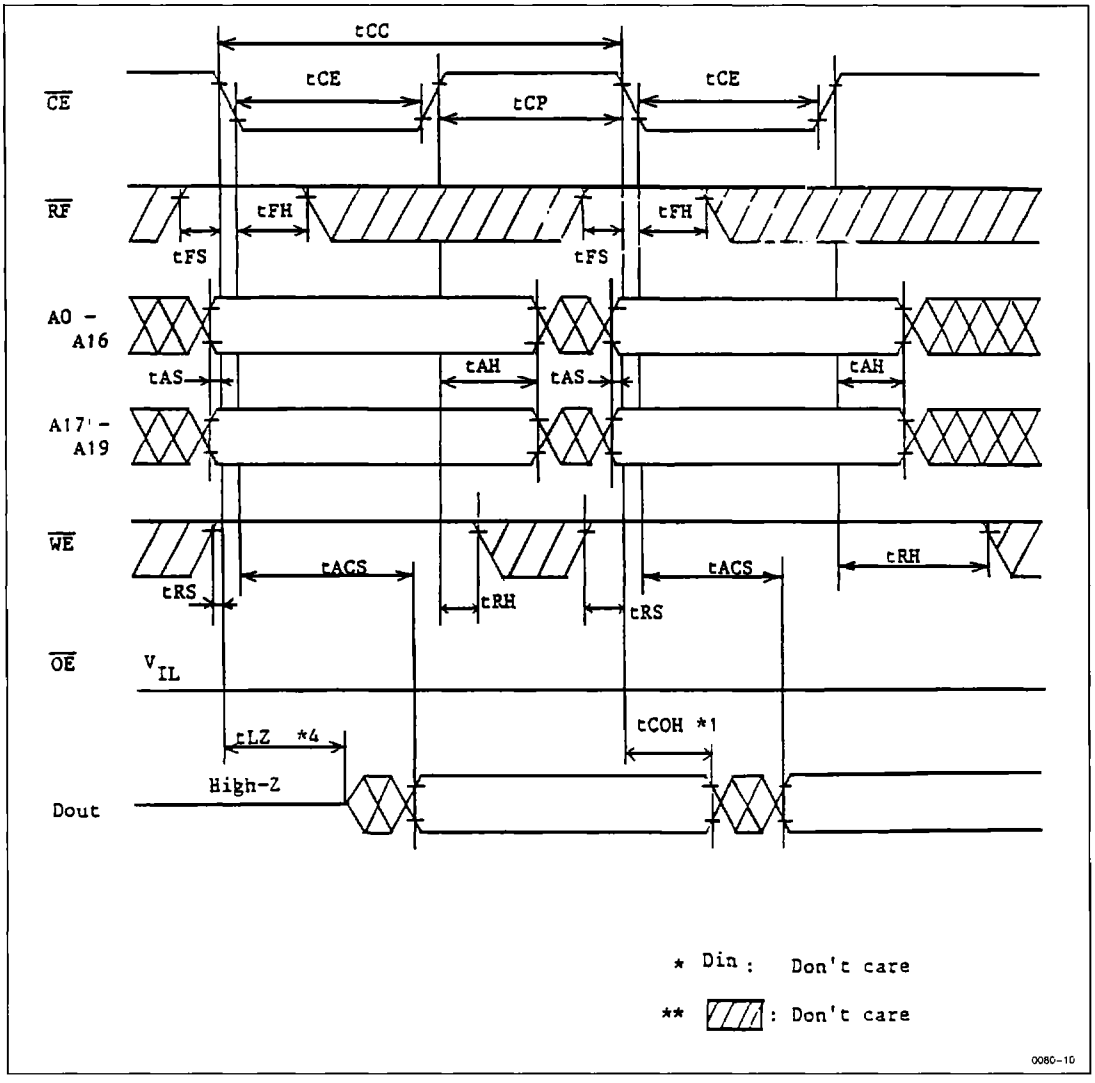
• **Read/Early Write Cycle**



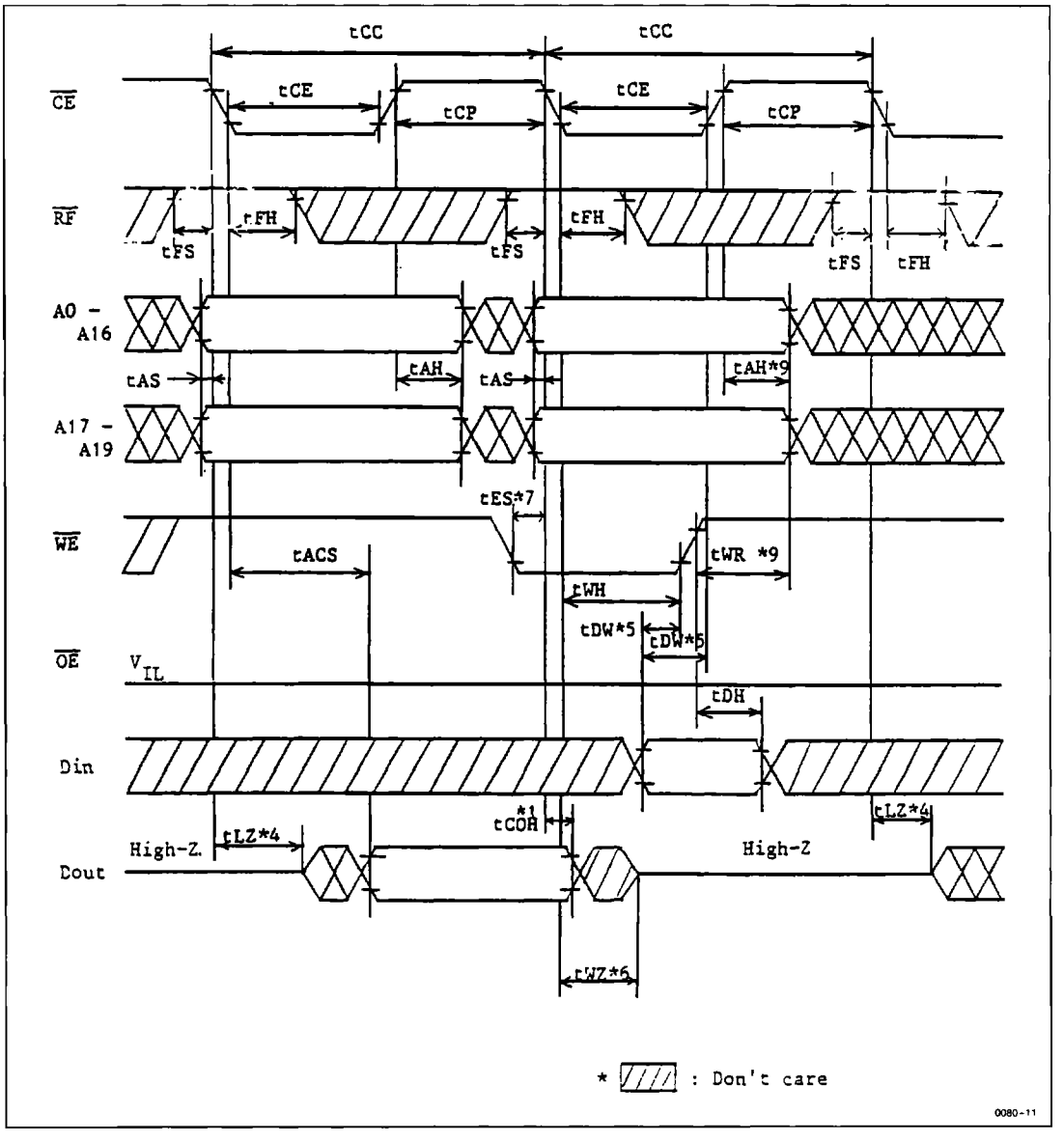
• **Read/Delayed Write Cycle**



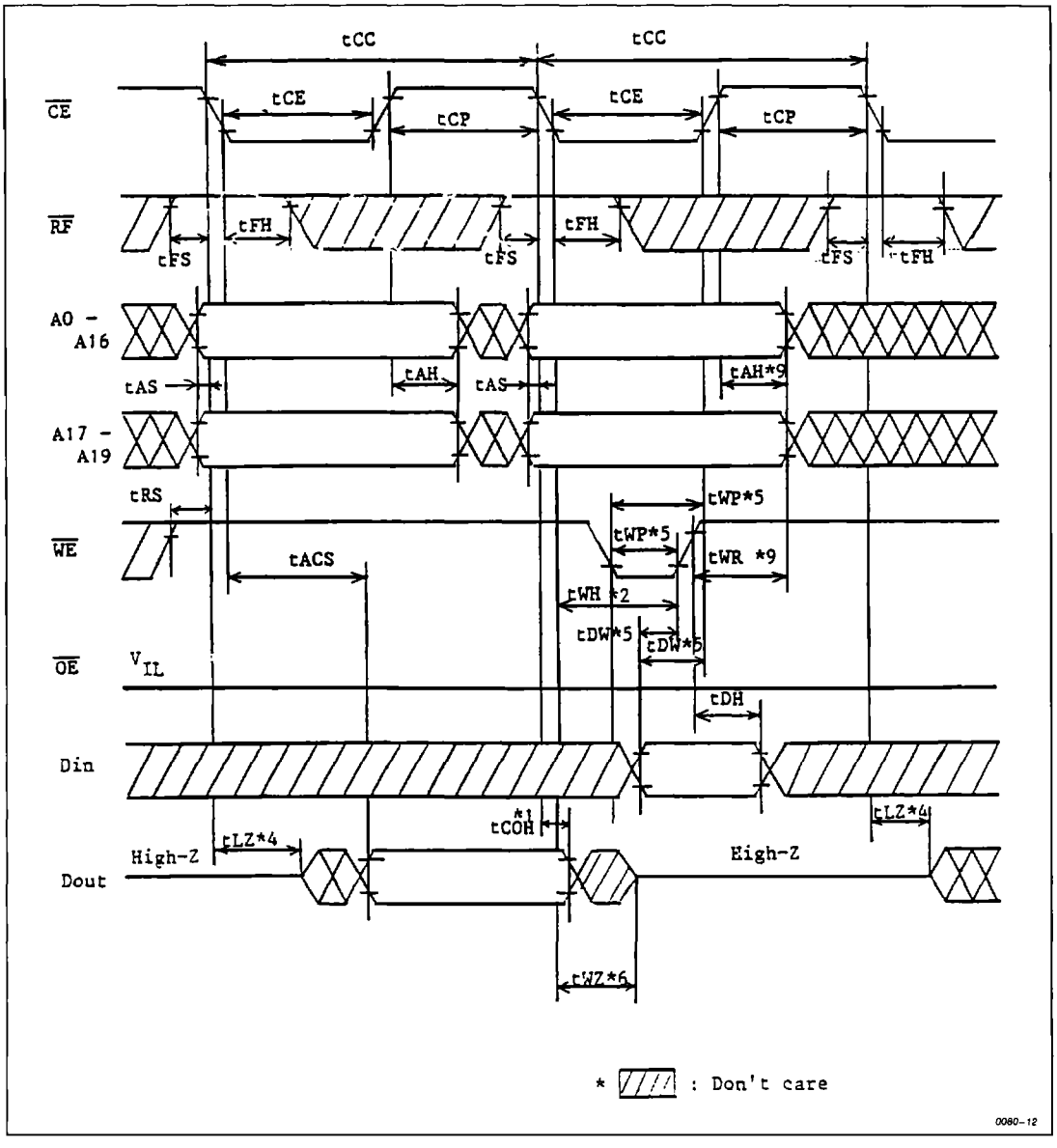
• **Read/Read Cycle ($\overline{OE}$ = V_{IL})**



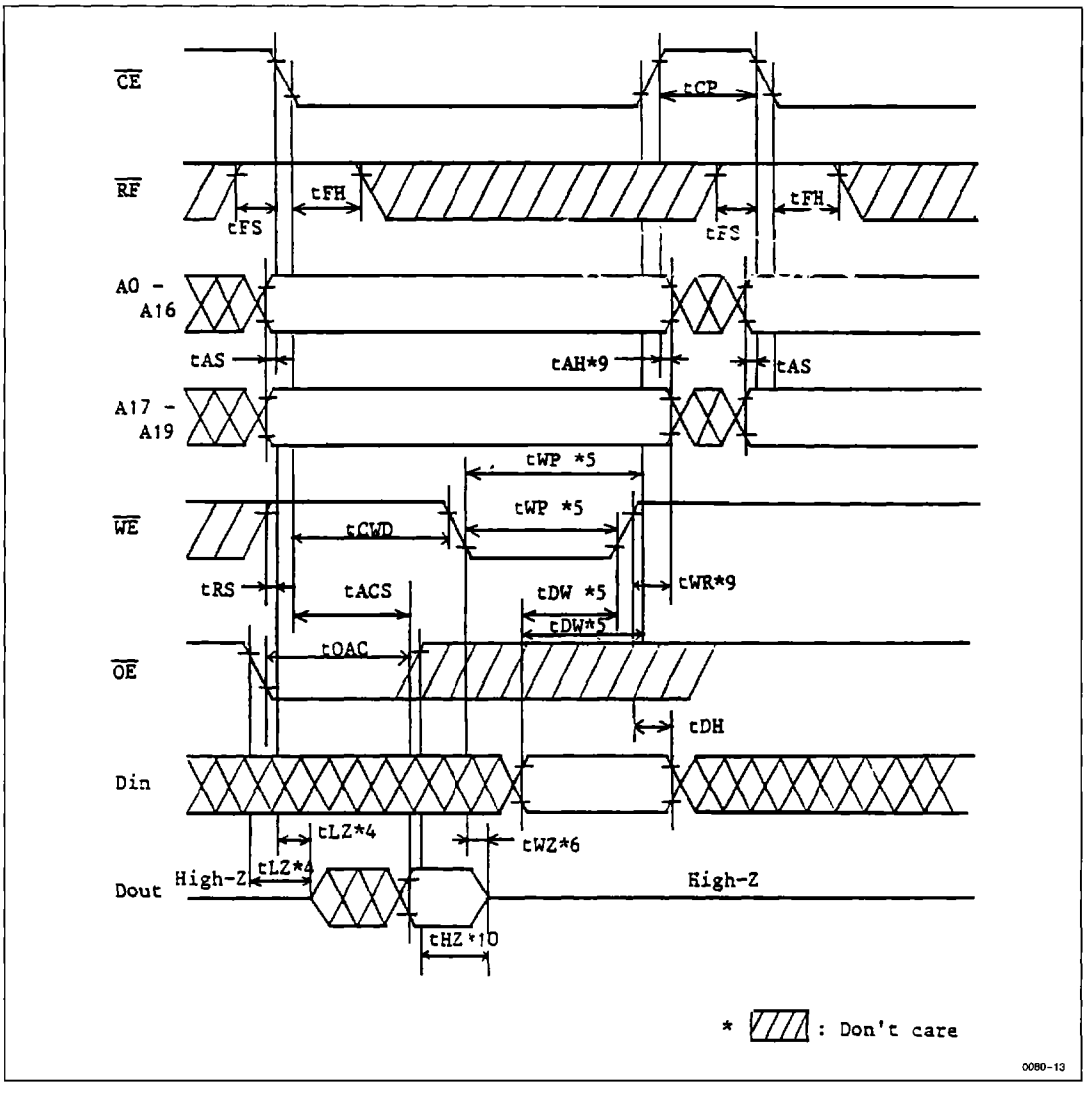
• **Read/Early Write Cycle ($\overline{OE}$ = V_{IL})**



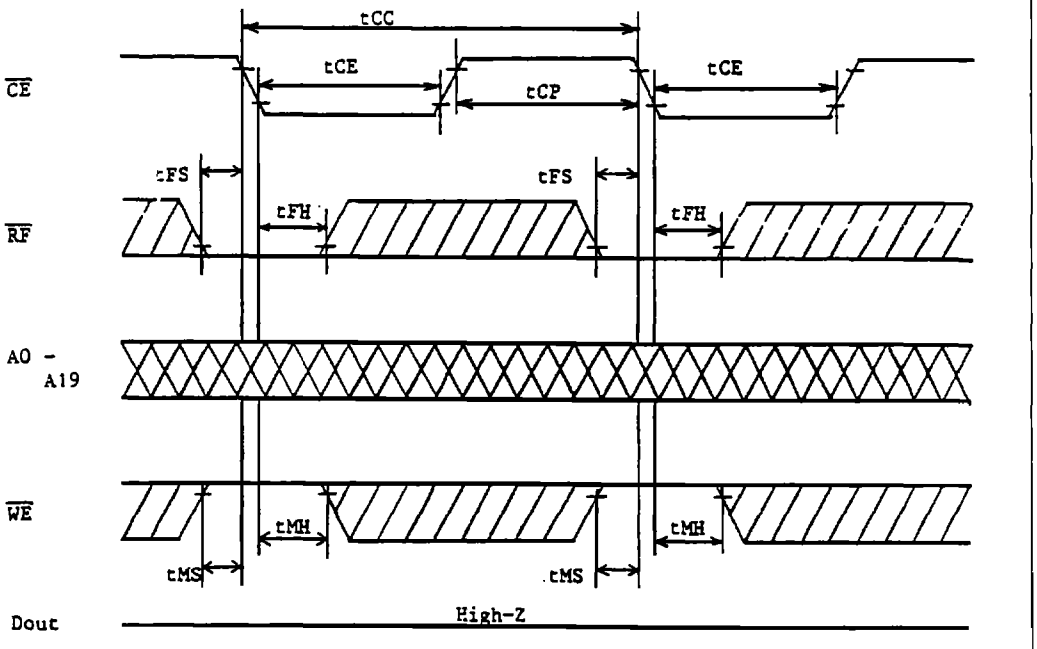
• **Read/Delayed Write Cycle ($\overline{OE}$ = V_{IL})**



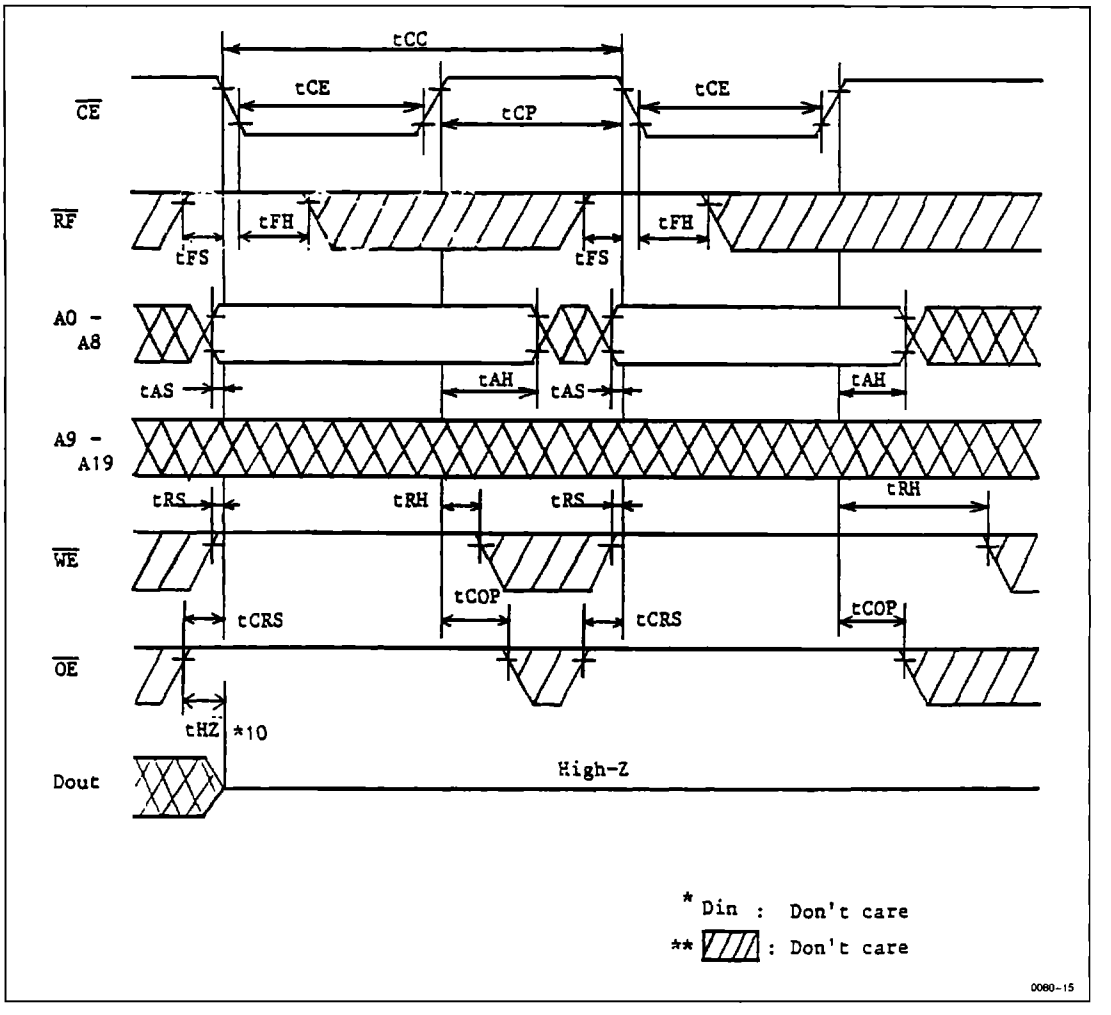
• **Read-Modify-Write Cycle**



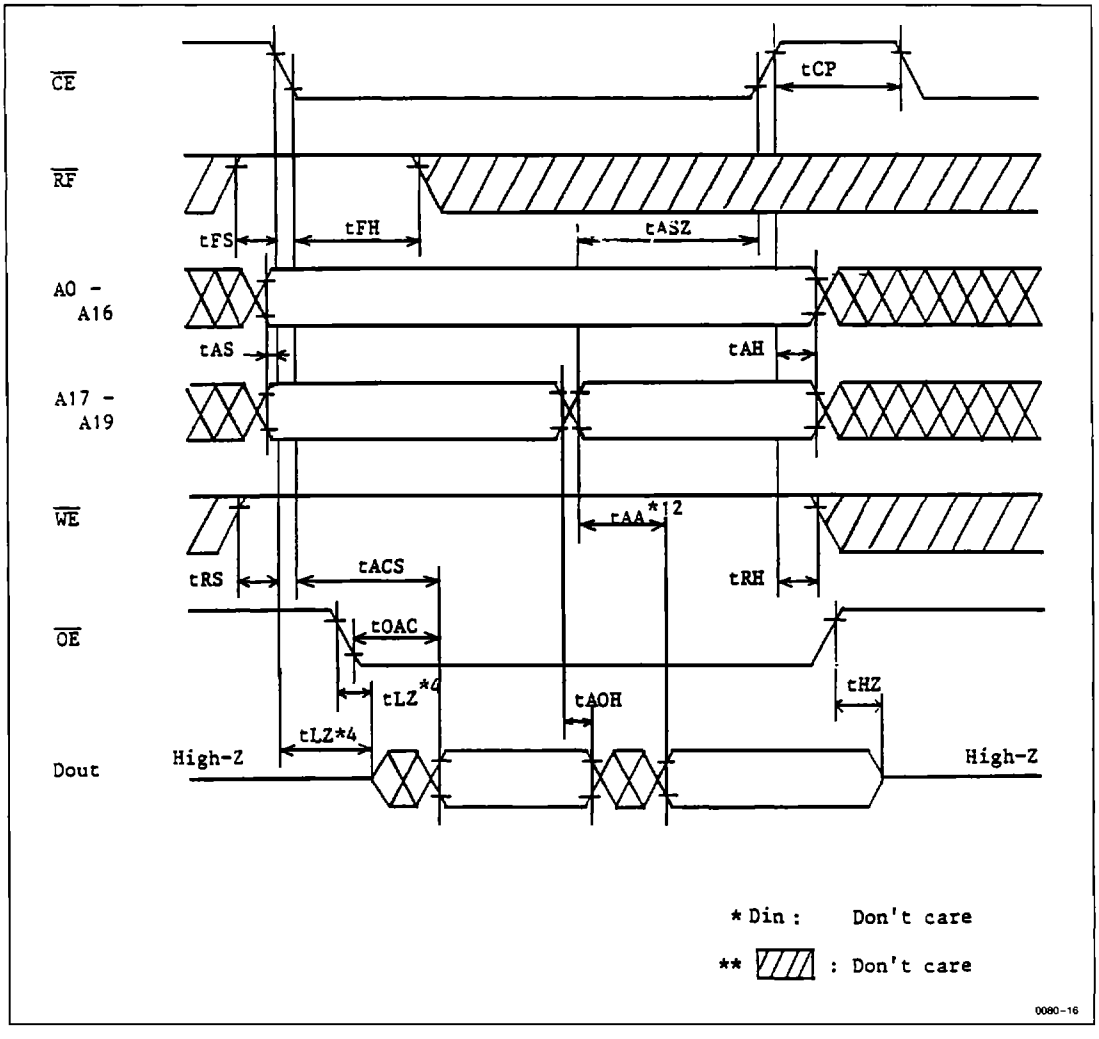
• **Automatic Refresh Cycle**



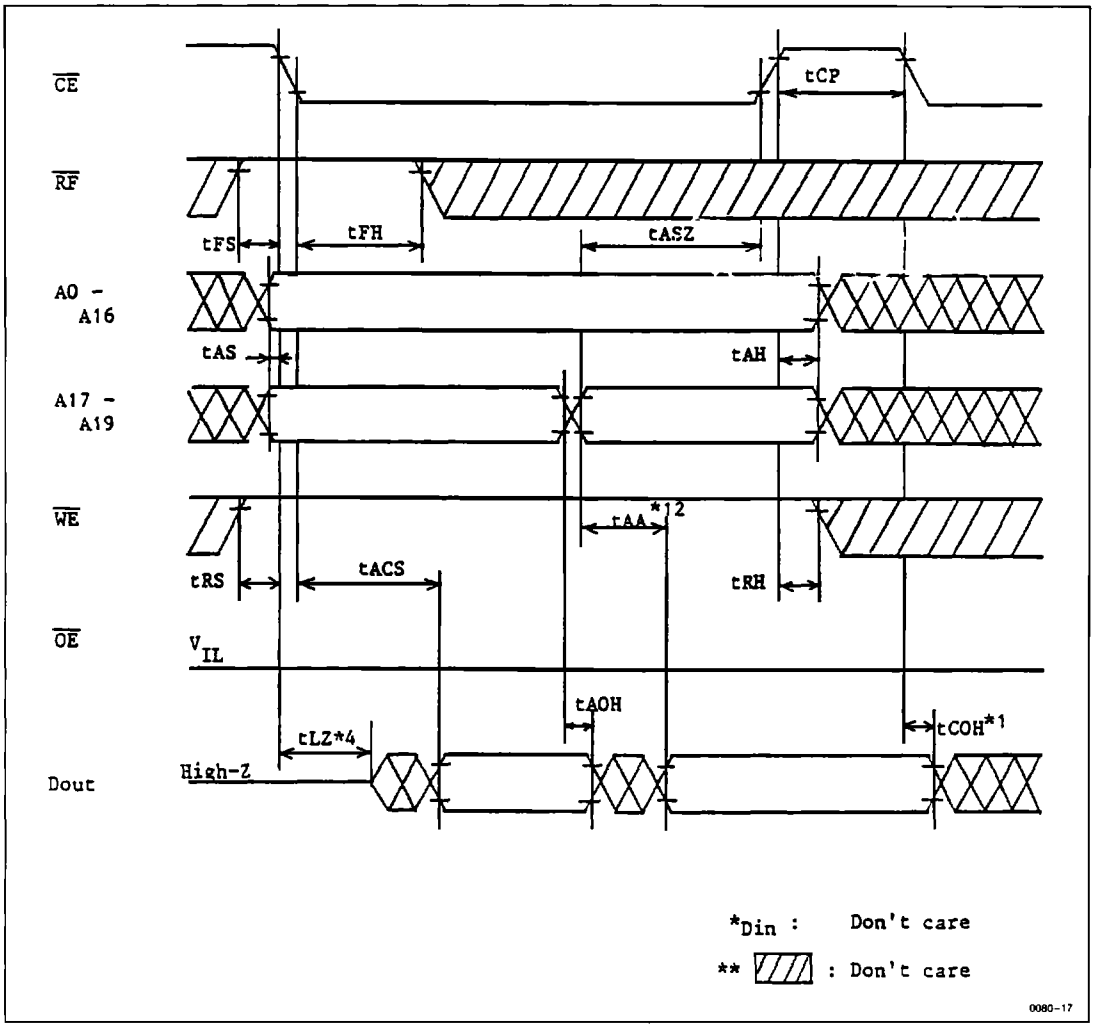
• $\overline{CE}$ Refresh



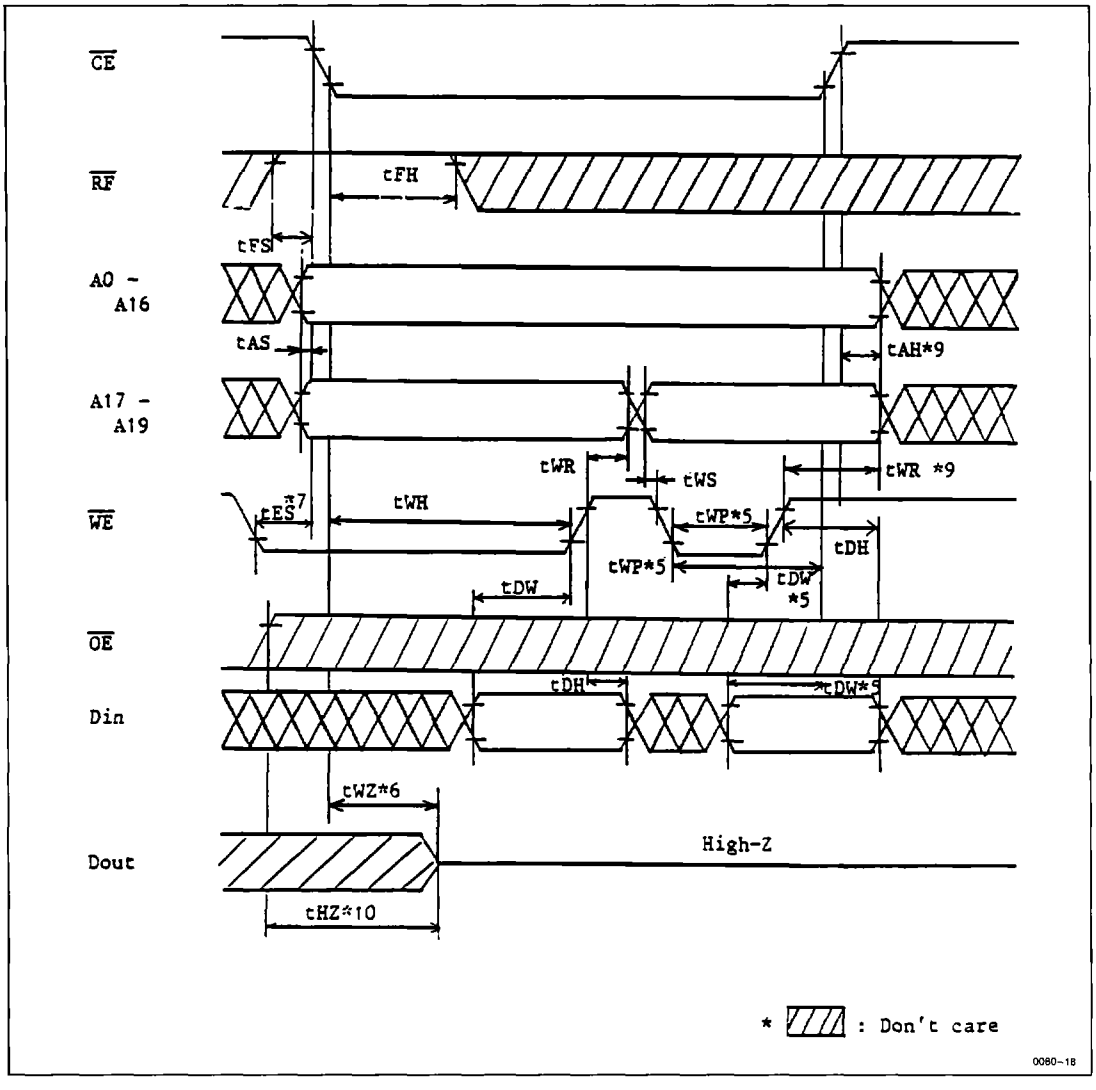
• **Static Column Mode Read Cycle**



• Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})



• Static Column Mode Write Cycle *8 (1st Cycle = Early Write Cycle)



• Static Column Mode Write Cycle *8 (1st Cycle = Delayed Write Cycle)