8. ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the TMP68000 and TMP68HC000.

8.1 MAXIMUM RATINGS

Rating	Symble	Value		Unit
		TMP68000	TMP68HC000	
Supply Voltage	Vcc	−0.3~ +7.0	−0.3~ +6.5	V
Input Voltage	Vin	−0.3~ +7.0	−0.3~ +6.5	V
Operating Temperature Range	Ta	0~ +70	0~ +70	°C
Storage Temperature	Tstg	−55~ +150	−55~ +150	°C

This device contains circitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or Vcc).

8.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0℃ ~ + 70℃ ; see Figures 8.1)

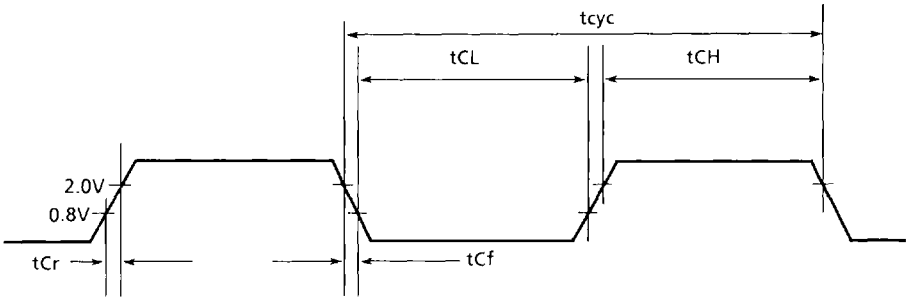
Characteristic		Symbol	TMP68000		TMP68HC000		Unit
			Min	Max	Min	Max	
Input High Voltage		V_{IH}	2.0	V_{CC}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND-0.3	0.8	GND-0.3	0.8	V
Input Leakage Current (5.25V)	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$,CLK,	I_{IN}	–	2.5	–	2.5	μA
	$\overline{IPL0}$~$\overline{IPL2}$, VPA		–	2.5	–	2.5	
	$\overline{HALT}$, $\overline{RESET}$		–	20	–	20	
Three-State (Off State) Input Current	(2.4V/0.4V)	I_{TSI}					μA
	$\overline{AS}$, A1~A23, D0-D15,		–	20	–	20	
	$\overline{FC0}$~$\overline{FC2}$, $\overline{LDS}$, R/$\overline{W}$,		–	20	–	20	
	$\overline{UDS}$, $\overline{VMA}$		–	20	–	20	
Output High Voltage (I_{OH} = -400μA)	E*	V_{OH}	V_{CC}-0.75		–		V
	E, $\overline{AS}$, A1~A23, $\overline{BG}$,		2.4	–	V_{CC}-0.75	–	
	D0~D15,		2.4	–	V_{CC}-0.75	–	
	$\overline{FC0}$-$\overline{FC2}$, $\overline{LDS}$, R/$\overline{W}$,		2.4	–	V_{CC}-0.75	–	
	$\overline{UDS}$, $\overline{VMA}$		2.4	–	V_{CC}-0.75	–	
Output Low Voltage		V_{OL}					V
(I_{OL} = 1.6mA)	$\overline{HALT}$		–	0.5	–	0.5	
(I_{OL} = 3.2mA)	A1~A23, $\overline{BG}$, FC0~FC2		–	0.5	–	0.5	
(I_{OL} = 5.0mA)	$\overline{RESET}$		–	0.5	–	0.5	
(I_{OL} = 5.3mA)	E, $\overline{AS}$, D0~D15,		–	0.5	–	0.5	
	$\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		–	0.5	–	0.5	
Current Dissipation***	f = 8MHz	I_D	–	–	–	25	mA
	f = 10MHz		–	–	–	30	
	f = 12.5MHz		–	–	–	35	
	f = 16.67MHz		–	–	–	50	
Power Dissipation	f = 8MHz	P_D	–	1.5	–	0.13	W
	f = 10MHz		–	1.5	–	0.16	
	f = 12.5MHz		–	1.5	–	0.19	
	f = 16.67MHz		–	–	–	0.26	
Capacitance (Vin = 0V, Ta = 25℃ ; Frequency = 1MHz)**		C_{IN}	–	20.0	–	20.0	pF
Load Capacitance	$\overline{HALT}$	C_L	–	70	–	70	pF
	All Others		–	130	–	130	

* : With external pullup resistor of 1.1kΩ.

** : Capacitance is periodically sampled rather than 100% tested.

*** : During normal operation instaneous V_{CC} current requirements may be as high as 1.5 A.

8.3 AC ELECTRICAL SPECIFICATIONS – CLOCK TIMING



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

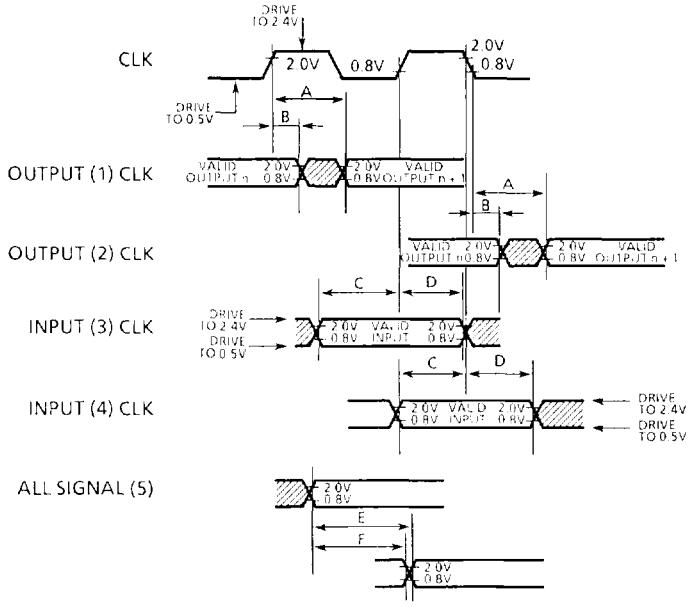
Figure 8.1 Clock Input Timing Diagram

8.4 AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clolk and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 8.2. In order to test the parameters guaranteed by TOSHIBA, inputs must be driven to the voltage levels specified in this figure. Outputs are specified with minimum and / or maximum limits, as appropriate, and are measured as shown in Figure 8.2. Inputs are specified with minimum setup and hold times, and are measured as shown. Finaly, the measurement for signal-to-signal specifications are also shown.

Note : The testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical character-istics.



Notes :

1 This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2 This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3 This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4 This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5 This timing is applicable to all parameters specified relative to the assertion / negation of another signal.

Legend :

A Maximum output delay specification.
B Minimum output hold time.
C Minimum input setup time specification.
D Minimum input hold time specification.
E Signal valid to signal valid specification (maximum or minimum).
F Signal valid to signal invalid specification (maximum to minimum).

Figure 8.2 Drive Levels and Test Points for AC Specifications

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (1/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	tCYC	125	250	100	250	80	250	60	125	ns
2	Clock Width Low	tCL	55	125	45	125	35	125	27	62.5	ns
3	Clock Width High	tCH	55	125	45	125	35	125	27	62.5	ns
4	Clock Fall Time	tCf	–	10	–	10	–	5	–	5	ns
5	Clock Rise Time	tCr	–	10	–	10	–	5	–	5	ns
6	Clock Low to Address Valid	tCLAV	–	62	–	50	–	50	–	30	ns
6A	Clock High to FC Valid	tCHFCV	–	62	–	50	–	45	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	tCHADZ	–	80	–	70	–	60	–	50	ns
8	Clock High to Address, FC Invalid (Minimum)	tCHAFI	0	–	0	–	0	–	0	–	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low	tCHSL	3	60	3	50	3	40	3	30	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Low (Read) / $\overline{AS}$ Low (Write)	tAVSL	30	–	20	–	15	–	15	–	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Low (Read) / $\overline{AS}$ Low (Write)	tFCVSL	90	–	70	–	60	–	45	–	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	tCLSH	–	62	–	50	–	40	3	30	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address / FC Invalid	tSHAFI	40	–	30	–	20	–	15	–	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (Read) / $\overline{AS}$ Low (Write)	tSL	270	–	195	–	160	–	120	–	ns
14A	$\overline{DS}$ Width Low (Write)	tDSL	140	–	95	–	80	–	60	–	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	tSH	150	–	105	–	65	–	60	–	ns

* : 68HC000 only

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (2/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
16	Clock High to Control Bus High Impedance	tCHCZ	–	80	–	70	–	60	–	50	ns
17[2]	$\overline{AS}$, $\overline{DS}$, High to R / $\overline{W}$ High (Read)	tSHRH	40	–	30	–	20	–	15	–	ns
18[1]	Clock High to R / $\overline{W}$ High	tCHRH	0	55	0	45	0	40	0	30	ns
20[1]	Clock High to R / $\overline{W}$ Low (Write)	tCHRL	0	55	0	45	0	40	0	30	ns
20A[2,6]	$\overline{AS}$ Low to R / $\overline{W}$ Valid (Write)	tASRV	–	10	–	10	–	10	–	10	ns
21[2]	Address Valid to R / $\overline{W}$ Low (Write)	tAVRL	20	–	0	–	0	–	0	–	ns
21A[2]	FC Valid to R / $\overline{W}$ Low (Write)	tFCVRL	60	–	50	–	30	–	30	–	ns
22[2]	R / $\overline{W}$ Low to $\overline{DS}$ Low (Write)	tRLSL	80	–	50	–	30	–	30	–	ns
23	CLock Low to Data Out Valid (Write)	tCLDO	–	62	–	50	–	50	–	30	ns
25[2]	$\overline{AS}$, $\overline{DS}$ High to Data Out Invalid (Write)	tSHDOI	40	–	30	–	20	–	15	–	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (Write)	tDOSL	40	–	30	–	20	–	15	–	ns
27[5]	Data in to Clock Low (Setup Time on Read)	tDICL	10	–	10	–	10	–	5	–	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to $\overline{DTACK}$ High (Asynchronous Hold)	tSHDAH	0	240	0	190	0	150	0	110	ns
29	($\overline{AS}$, $\overline{DS}$ High to Data-In Invalid (Hold Time on Read)	tSHDII	0	–	0	–	0	–	0	–	ns

* : 68HC000 only

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (3/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	tSHBEH	0	–	0	–	0	–	0	–	ns
31[2,5]	$\overline{DTACK}$ Low to Data In (Setup Time)	tDALDI	–	90	–	65	–	50	–	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition	tRHr, f	0	200	0	200	0	200	–	150	ns
33	Clock High to $\overline{BG}$ Low	tCHGL	–	62	–	50	–	40	0	30	ns
34	CLock High to $\overline{BG}$ Low	tCHGH	–	62	–	50	–	40	0	30	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36[7]	$\overline{BR}$ High to $\overline{BG}$ Low	tBRHGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ Low	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37A[8]	$\overline{BGACK}$ Low to $\overline{BG}$ Low	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	10	1.5 Clocks	ns
38	$\overline{BG}$ Width High	tGLZ	–	80	–	70	–	60	–	50	ns
39	$\overline{BG}$ Width High	tGH	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
40	Clock Low to $\overline{VMA}$ Low	tCLVML	–	70	–	70	–	70	–	50	ns
41	Clock Low to E Transition	tCLET	–	55	–	45	–	35	–	35	ns
42	E Output Rise and Fall Time	tEr, f	–	15	–	15	–	15	–	15	ns
43	$\overline{VMA}$ Low to E High	tVMLEH	200	–	150	–	90	–	80	–	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	tSHVPH	0	120	0	90	0	70	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	tELCAI	30	–	10	–	10	–	10	–	ns

* : 68HC000 only

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (4/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

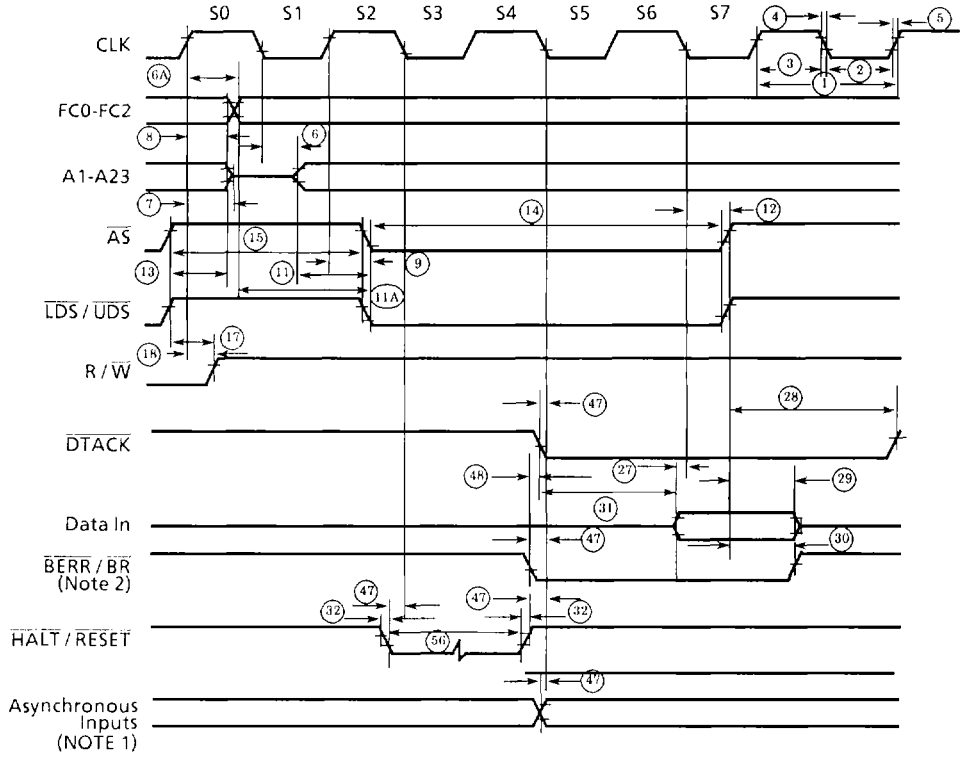
Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
46	$\overline{BGACK}$ Width Low	tGAL	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
47[5]	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	5	–	ns
48[2,3]	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	tBELDAL	20	–	20	–	20	–	10	–	ns
49[9]	$\overline{AS}$, $\overline{DS}$ High to E Low	tSHEL	−70	70	−55	55	−45	45	−35	35	ns
50	E Width High	tEH	450	–	350	–	280	–	220	–	ns
51	E Width High	tEL	700	–	550	–	440	–	340	–	ns
53	Clock High to Data Out Invalid	tCHDOI	0	–	0	–	0	–	0	–	ns
54	E Low to Data Out Invalid	tELDOI	30	–	20	–	15	–	10	–	ns
55	R / $\overline{W}$ to Data Bus Driven	tRLDBD	30	–	20	–	10	–	0	–	ns
56[4]	$\overline{HALT}$ / $\overline{RESET}$ Pulse Width	tHRPW	10	–	10	–	10	–	10	–	Clk. Per.
57	$\overline{BGACK}$ High to Control Bus Driven	tGASD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
58[7]	$\overline{BG}$ High to Control Bus Driven	tRHSD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.

* : 68HC000 only

Note :

1. For a loading capacitance of less than or equal to 50 picofarads, substract 5 nanoseconds from the value given in the maximum columns.
2. Actual value depends on period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may by 0 nanoseconds.
4. For powder up, the MPU must be held in $\overline{RESET}$ state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the date-in clock-low setup time (#27) for the following cycle.
6. When $\overline{AS}$ and R / $\overline{W}$ are equally loaded (±20%), subtract 10 nanoseconds from the values given in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{xDS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

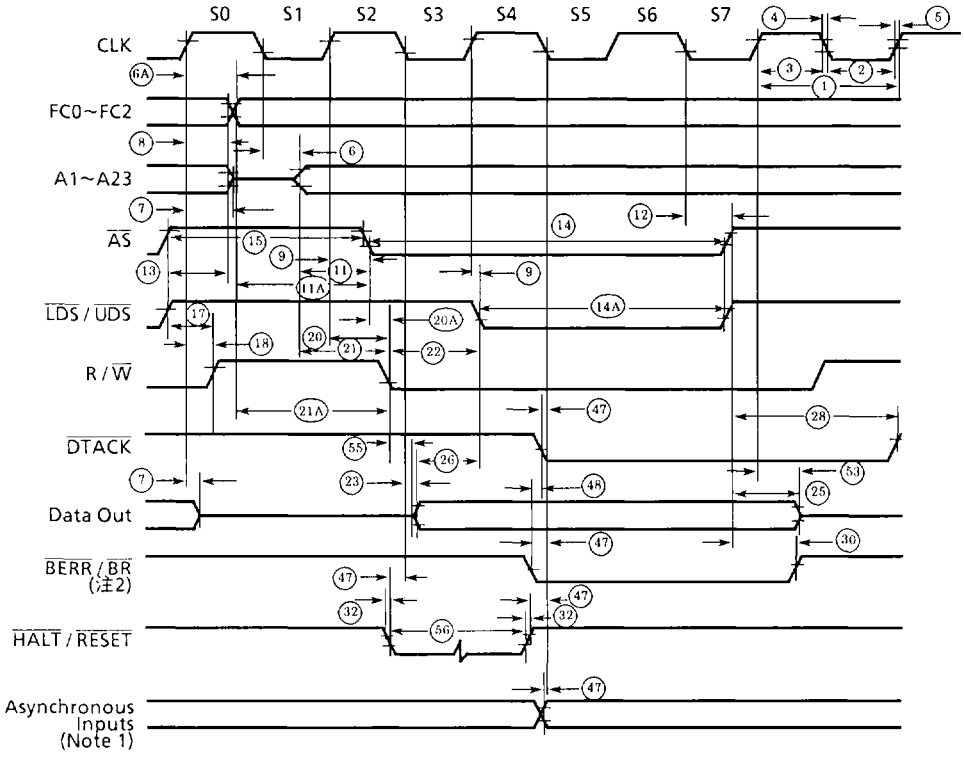


Note :

1. Setup time for the asynchronous inputs $\overline{IPL0}$~$\overline{IPL2}$, and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only in order to insure being recognized at the end of this bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8.3 Read Cycle Timing Diagram

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note :

1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
   The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt 2.0 volts.
2. Because of loading variation, R / $\overline{W}$ may be valid after $\overline{AS}$ even through both are initiated by the rising edge of S2 (Specification 20A).

Figure 8.4 Write Cycle Timing Diagram

8.6 AC ELECTRICAL SPECIFICATIONS – TMP68HC000 TO 6800 PERIPHERAL

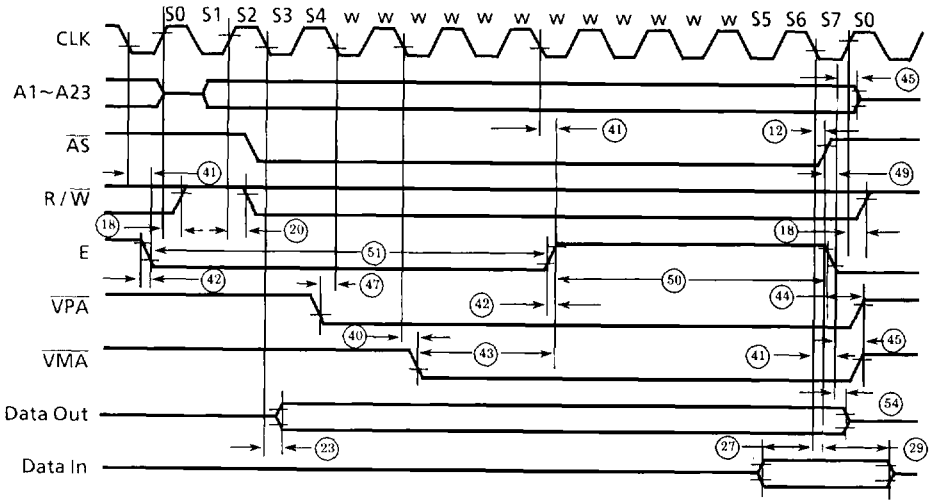
(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.5 and 8.6)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
12[1]	CLock Low to $\overline{AS}$, $\overline{DS}$ High	tCLSH	–	62	–	50	–	40	3	30	ns
18[1]	Clock High to R / $\overline{W}$ High	tCHRH	0	55	0	45	0	40	0	30	ns
20[1]	Clock High to R / $\overline{W}$ Low (Write)	tCHRL	0	55	0	45	0	40	0	30	ns
23	Clock Low to Data Out Valid (Write)	tCLDO	–	62	–	50	–	50	–	30	ns
27	Data In to Clock Low (Setup Time on Read)	tDICL	10	–	10	–	10	–	5	–	ns
29	$\overline{AS}$, $\overline{DS}$ High to Data in Invalid (Hold Time on Read)	tSHDII	0	–	0	–	0	–	0	–	ns
40	Clock Low to $\overline{VMA}$ Low	tCLVML	–	70	–	70	–	70	–	50	ns
41	Clock Low to E Transition	tCLET	–	55	–	45	–	35	–	35	ns
42	E Output Rise and Fall Time	tEr, f	–	15	–	15	–	15	–	15	ns
43	$\overline{VMA}$ Low to E High	tVMLEH	200	–	150	–	90	–	80	–	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	tSHVPH	0	120	0	90	0	70	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	tELCAI	30	–	10	–	10	–	10	–	ns
47	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	5	–	ns
49[2]	$\overline{AS}$, $\overline{DS}$ High to E Low	tSHEL	– 70	70	– 55	55	– 45	45	– 35	35	ns
50	E Width High	tEH	450	–	350	–	280	–	220	–	ns
51	E Width Low	tEL	700	–	550	–	440	–	340	–	ns
54	E Low to Data Out Invalid	tELDOI	30	–	20	–	15	–	10	–	ns

Note 1 : For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

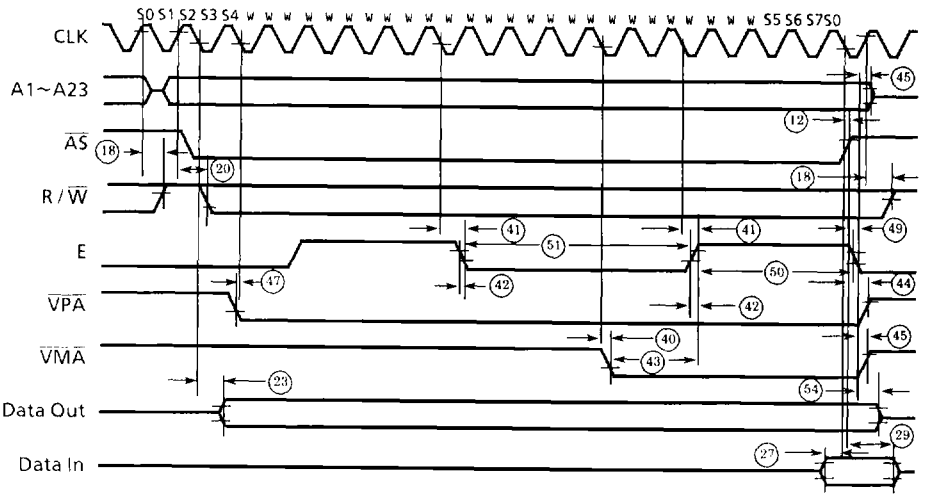
2 : The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and falling edge of the E clock.

* : 68HC000 only



Note : This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the best case possibly attainable.

Figure 8.5 TMP68000 to 6800 Peripheral Timimg Diagram – Best Case



Note : This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the worst case possibly attainable.

Figure 8.6 TMP68000 to 6800 Peripheral Timing Diagram – Worst Case

8.7 AC ELECTRICAL SPECIFICATIONS – BUS ARBITRATION

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.7)

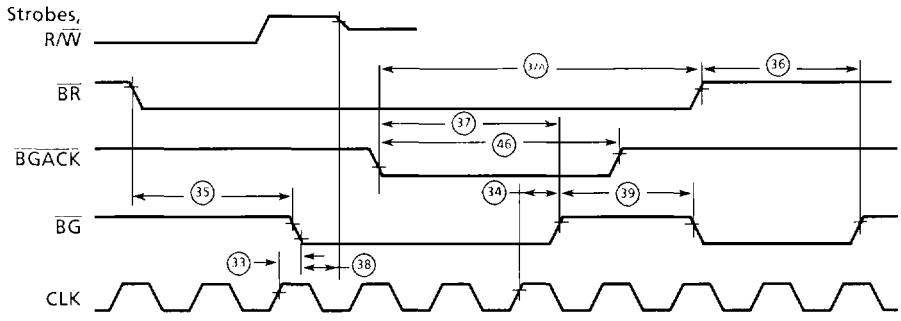
Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance	tCHADZ	–	80	–	70	–	60	–	50	ns
16	Clock High to Control Bus High Impedance	tCHCZ	–	80	–	70	–	60	–	50	ns
33	Clock High to $\overline{BG}$ Low	tCHGL	–	62	–	50	–	40	0	30	ns
34	Clock High to $\overline{BG}$ High	tCHGH	–	62	–	50	–	40	0	30	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36[1]	$\overline{BR}$ High to $\overline{BG}$ High	tBKHGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37A[2]	$\overline{BGACK}$ Low to $\overline{BR}$ High	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	10	1.5 Clocks	ns
38	$\overline{BG}$ Low to Control, Address, Data Bus High Impedance ($\overline{AS}$ High)	tGLZ	–	80	–	70	–	60	–	50	ns
39	$\overline{BG}$ Width High	tGH	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
46	$\overline{BGACK}$ Width Low	tGAL	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
47	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	5	–	ns
57	$\overline{BGACK}$ High to Control Bus Driven	tGABD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
58[1]	$\overline{BG}$ High to Control Bus Driven	tGHBD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.

Note: 1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

2. The minimum value must to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.

*: 68HC000 only

The waveforms shown in Figures 8.9, 8.10, and 8.11 should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note : Setup time to the clock (#47) for the asynchronous imputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$~$\overline{IPL2}$ and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.

Figure 8.7 Bus Arbitration Diagram