

### IGBT chip with monolithically integrated diode in packages offering space saving advantage

#### Features:

TRENCHSTOP<sup>TM</sup> Reverse Conducting (RC) technology for 600V applications offering:

- Optimised V<sub>CEsat</sub> and V<sub>F</sub> for low conduction losses
- Smooth switching performance leading to low EMI levels
- Very tight parameter distribution
- Operating range of 1 to 20kHz
- Maximum junction temperature 175°C
- Short circuit capability of 5µs
- Best in class current versus package size performance
- Qualified according to JEDEC for target applications
- Complete product spectrum and PSpice Models: http://www.infineon.com/igbt/



Motor drives Discrete components and molded modules

Chip Type	V <sub>CE</sub>	I <sub>Cn</sub>	Die Size	Package
IGC10R60D	600V	15A	2.70 x 3.73 mm <sup>2</sup>	sawn on foil

#### **Mechanical Parameter** Raster size 2.70 x 3.73 Emitter pad size see chip drawing $mm^2$ Gate pad size see chip drawing Area: total / active IGBT / active Diode 10.071 / 5.544 / 1.317 **Thickness** 70 μm Wafer size 150 mm Max.possible chips per wafer 1450 Photoimide Passivation frontside Pad metal 3200 nm AlSiCu Ni Ag -system Backside metal suitable for epoxy and soft solder die bonding Die bond Electrically conductive glue or solder Wire bond AI, <500µm Reject ink dot size Ø 0.65mm; max 1.2mm Store in original container, in dry nitrogen, in dark Recommended storage environment environment, < 6 month at an ambient temperature of 23°C





### **Maximum Ratings**

Parameter	Symbol	Value	Unit	
Collector-Emitter voltage, T <sub>j</sub> =25 °C	V <sub>CE</sub>	600	V	
DC collector current, limited by T <sub>j max</sub>	I <sub>C</sub>	1)	Α	
Pulsed collector current, t <sub>p</sub> limited by T <sub>j max</sub>	I <sub>c,puls</sub>	45	Α	
Gate emitter voltage	V <sub>GE</sub>	±20	V	
Junction temperature	$T_{\rm vj,max}$	-40 +175	°C	
Operating junction temperature	$T_{vj,op,max}$	-40 +175	°C	
Short circuit data <sup>2)</sup> V <sub>GE</sub> = 15V, V <sub>CC</sub> = 400V, T <sub>vj</sub> = 150°C	t <sub>p,max</sub>	5	μs	
Safe operating area IGBT <sup>2 )3)</sup>	$I_{C,max} = 30A, V_{CE,max} = 600V, T_{vj,op} \le T_{vj,op,m}$			
Safe operating area Diode <sup>2</sup> )	$I_{F,max} = 30A, V_{R,max} = 600V,$ $P_{max} = 12 \text{ kW}, T_{V,i,op} \le T_{V,i,op,max}$			

## Static Characteristics (tested on wafer), $T_j$ =25 °C

Parameter	Symbol	Conditions	Value			Unit
Tarameter	Cymbol	Conditions	min. typ.		max.	
Collector-Emitter breakdown voltage	V <sub>(BR)CES</sub>	$V_{GE}$ =0V , $I_{C}$ = 0.2mA	600			
Collector-Emitter saturation voltage	V <sub>CE(sat)</sub>	V <sub>GE</sub> =15V, I <sub>C</sub> =15A		1.65	2.1	V
Diode Forward Voltage	V <sub>F</sub>	V <sub>GE</sub> =0V, I <sub>F</sub> =15A		1.7	2.1	V
Gate-Emitter threshold voltage	V <sub>GE(th)</sub>	$I_C$ =0.25mA , $V_{GE}$ = $V_{CE}$	4.3	5	5.7	
Zero gate voltage collector current	I <sub>CES</sub>	V <sub>CE</sub> =600V , V <sub>GE</sub> =0V			40	μA
Gate-Emitter leakage current	I <sub>GES</sub>	V <sub>CE</sub> =0V , V <sub>GE</sub> =20V			100	nA
Integrated gate resistor	R <sub>Gint</sub>			0		Ω

## **Dynamic Characteristics** (not subject to production test - verified by design / characterization), T<sub>i</sub>=25 °C

Parameter	Symbol	Conditions	Value			Unit
raiailletei	Syllibol	Conditions	min.	typ.	max.	Ullit
Input capacitance	Ciss	V <sub>CE</sub> =25V,		961		
Output capacitance	Coss	V <sub>GE</sub> =0V,		53		pF
Reverse transfer capacitance	Crss	f=1MHz		33		

<sup>&</sup>lt;sup>1)</sup> depending on thermal properties of assembly <sup>2)</sup> not subject to production test - verified by design/characterization

<sup>&</sup>lt;sup>3)</sup> allowed number of short circuits: <1000; time between short circuits: >1s





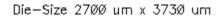
#### **Further Electrical Characteristic**

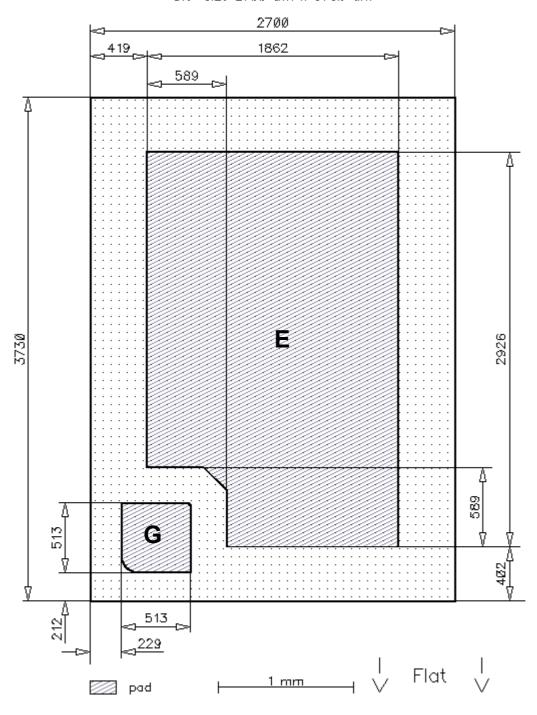
Switching characteristics and thermal properties are depending strongly on package design and mounting technology and can therefore not be specified for a bare die.

Further technical information about the performance of this chip in package t.b.d. is given exemplarily at www.infineon.com/igbt. The chip qualification is independent of the qualification which is performed for the Discretes.



## **Chip Drawing**



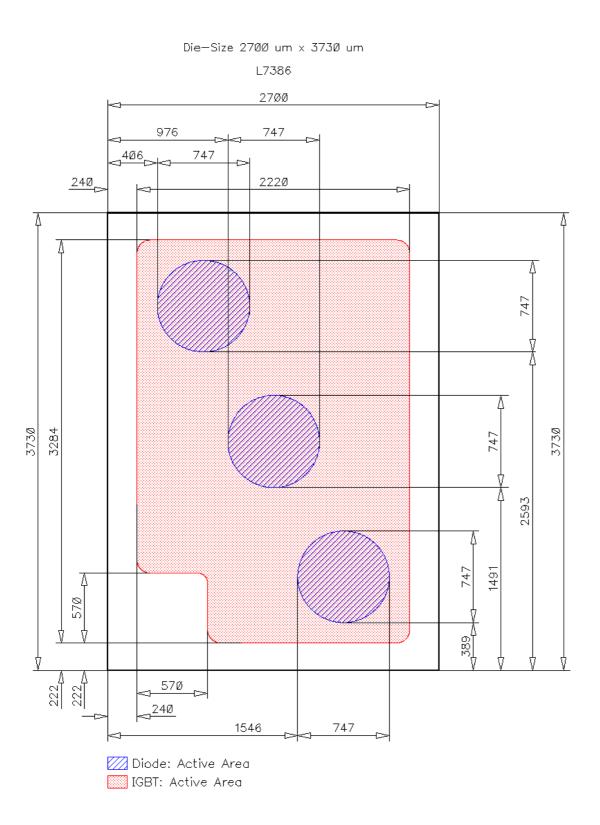


**E** = Emitter

**G** = Gate



## **Chip Drawing active areas**





#### Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

#### **Revision History**

Version	Subjects (major changes since last revision)	Date
2.0	Release of final datasheet	12.01.2010

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