Complete, Quad, 12-/14-/16-Bit, Serial Input, Unipolar/Bipolar Voltage Output DACs

Preliminary Technical Data

AD5724R/AD5734R/AD5754R

FEATURES

Complete, quad, 12-/14-/16-bit D/A converter
Operates from single/dual supplies
Software programmable output range
+5 V, +10 V, +10.8 V, ±5 V, ±10 V, ±10.8 V
INL error: ±16 LSB maximum, DNL error: ±1 LSB maximum
Total unadjusted error (TUE): 0.1% FSR maximum
Settling time: 10 µs maximum
Integrated reference: 5 ppm/°C typ.
Integrated reference buffers
Output control during power-up/brownout
Simultaneous updating via $\overline{\text{LDAC}}$
Asynchronous $\overline{\text{CLR}}$ to zero-/mid-scale
DSP/microcontroller-compatible serial interface
24-lead TSSOP
Operating temperature range: −40°C to +85°C
***i*CMOS™ process technology[1]**

APPLICATIONS

Industrial automation
Closed-loop servo control, process control
Automotive test and measurement
Programmable logic controllers

GENERAL DESCRIPTION

The AD5724R/AD5734R/AD5754R are quad, 12-/14-/16-bit serial input, voltage output, digital-to-analog converters. They operate from single supply voltages of +4.5 V up to +16.5 V or dual supply voltages from ±4.5 V up to ±16.5 V. Nominal full-scale output range is software-selectable from the options of +5 V, +10 V, +10.8 V, ±5 V, ±10 V, or ±10.8 V. Integrated output amplifiers, reference buffers, and proprietary power-up/power-down control circuitry are also provided.

The parts offer guaranteed monotonicity, integral nonlinearity (INL) of ±16 LSB maximum, low noise, 10 µs maximum settling time, and an on-chip +2.5 V reference.

The AD5724R/AD5734R/AD5754R use a serial interface that operates at clock rates up to 30 MHz and are compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is user-selectable twos complement or offset binary for a bipolar output (depending on the state of pin BIN/$\overline{\text{2sComp}}$), and straight binary for a unipolar output. The asynchronous clear function clears all DAC registers to a user-selectable zero-scale or mid-scale output. The parts are available in a 24-lead TSSOP and offer guaranteed specifications over the −40°C to +85°C industrial temperature range.

Table 1. Pin Compatible Devices

Part Number	Description
AD5724/AD5734/AD5754	AD5724R/AD5734R/AD5754R without internal reference.
AD5722/AD5732/AD5752	Complete, dual, 12-/14-/16-bit, serial input, unipolar/bipolar, voltage output DAC.
AD5722R/AD5732R/AD5752R	AD5722/AD5732/AD5752 with internal reference.

[1] For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30 V and operating at ±15 V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.

Rev. PrC

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REVISION HISTORY

PrC – Preliminary Revision, November 16, 2007

FUNCTIONAL BLOCK DIAGRAM

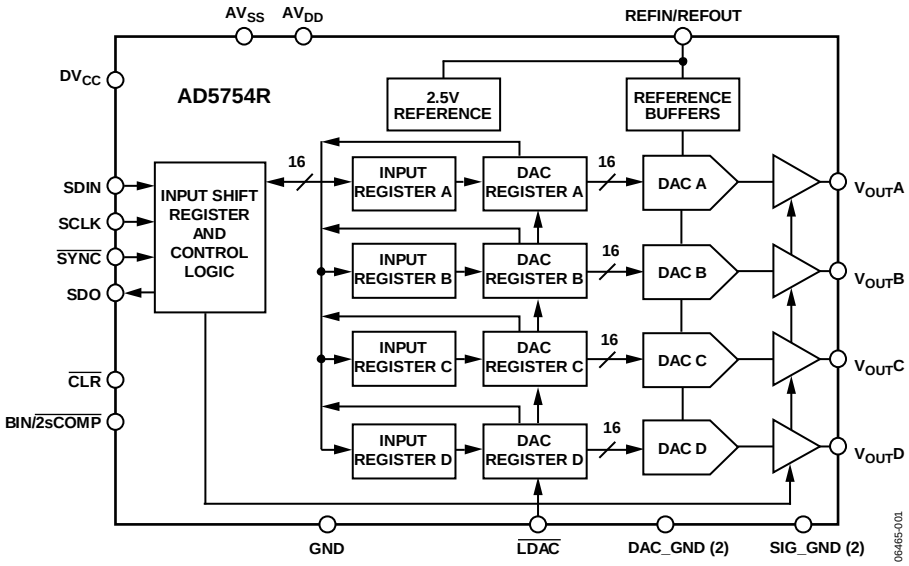


Figure 1.

SPECIFICATIONS

DUAL SUPPLY SPECIFICATIONS

AV_{DD} = 4.5 V[1] to 16.5 V, AV_{SS} = −4.5 V[1] to −16.5 V, GND = 0 V, REFIN= +2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX}, ±10 V range unless otherwise noted.

Table 2.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY			Outputs unloaded
Bipolar Output			
Resolution			
AD5754R	16	Bits	
AD5734R	14	Bits	
AD5724R	12	Bits	
Total Unadjusted Error (TUE)	0.1	% FSR max	Over temperature, supplies, and time
Relative Accuracy (INL)			
B Grade	±16	LSB max	@ 16-bit resolution
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic (@ 16-bit resolution)
Bipolar Zero Error	±5	mV max	@ 25°C, error at other temperatures obtained using Bipolar Zero TC
Bipolar Zero TC[2]	±8	ppm FSR/°C max	
Zero-Scale Error	±1	mV max	@ 25°C, error at other temperatures obtained using Zero Scale TC
Zero-Scale TC[2]	±8	ppm FSR/°C max	
Gain Error	±0.05	% FSR max	@ 25°C, error at other temperatures obtained using Gain TC
Gain TC[2]	±8	ppm FSR/°C max	
DC Crosstalk[2]	0.6	LSB max	@ 16-bit resolution
Unipolar Output			
Resolution			
AD5754R	16	Bits	
AD5734R	14	Bits	
AD5724R	12	Bits	
Total Unadjusted Error (TUE)	0.1	% FSR max	Over temperature, supplies, and time
Relative Accuracy (INL)			
B Grade	±16	LSB max	@ 16-bit resolution
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic (@ 16 bit-resolution)
Zero-Scale Error	+10	mV max	@ 25°C, error at other temperatures obtained using Zero-Scale TC
Zero-Scale TC[2]	±4	ppm FSR/°C max	
Offset Error	±10	mV max	
Gain Error	±0.05	% FSR max	@ 25°C, error at other temperatures obtained using Gain TC
Gain TC[2]	±4	ppm FSR/°C max	
DC Crosstalk[2]	0.6	LSB max	@ 16-bit resolution
REFERENCE INPUT/OUTPUT			
Reference Input[2]			
Reference Input Voltage	2.5	V nom	±1% for specified performance
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±10	µA max	Typically ±30 nA
Reference Range	2 to 3	V min to V max	
Reference Output			
Output Voltage	2.498 to 2.502	V min to V max	@ 25°C
Reference TC	±5	ppm/°C typ	
	±10	ppm/°C max	
Output Noise (0.1 Hz to 10 Hz)[2]	18	µV p-p typ	
Noise Spectral Density[2]	75	nV/√Hz typ	@ 10 kHz
Output Voltage Drift vs. Time[2]	±40	ppm/500 hr typ	
	±50	ppm/1000 hr typ	

Parameter	Value	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS[2]			
Output Voltage Range	±10.8	V min to V max	AV_{DD}/AV_{SS} = ±11.7 V min , REFIN = +2.5 V
	±12	V min to V max	AV_{DD}/AV_{SS} = ±12.9 V min, REFIN = +3 V
Headroom	0.9	V max	
	0.5	V typ	
Output Voltage TC	±8	ppm FSR/°C max	
Output Voltage Drift vs. Time	±12	ppm FSR/500 hr typ	
	±15	ppm FSR/1000 hr typ	
Short-Circuit Current	20	mA typ	
Load	2	kΩ min	For specified performance
Capacitive Load Stability	4000	pF max	
DC Output Impedance	0.5	Ω typ	
DIGITAL INPUTS[2]			DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage	0.8	V max	
Input Current	±1	µA max	Per pin
Pin Capacitance	5	pF typ	Per pin
DIGITAL OUTPUTS (SDO)[2]			
V_{OL}, Output Low Voltage	0.4	V max	DV_{CC} = 5 V ± 10%, sinking 200 µA
V_{OH}, Output High Voltage	DV_{CC} – 1	V min	DV_{CC} = 5 V ± 10%, sourcing 200 µA
V_{OL}, Output Low Voltage	0.4	V max	DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA
V_{OH}, Output High Voltage	DV_{CC} – 0.5	V min	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	µA max	
High Impedance Output Capacitance	5	pF typ	
POWER REQUIREMENTS			
AV_{DD}	4.5 to 16.5	V min to V max	
AV_{SS}	-4.5 to -16.5	V min to V max	
DV_{CC}	2.7 to 5.5	V min to V max	
Power Supply Sensitivity[2]			
$\Delta V_{OUT}/\Delta AV_{DD}$	−75	dB typ	200mV sine wave superimposed on AV_{SS}/AV_{DD} @ 50/60 Hz
AI_{DD}	2	mA/channel max	Outputs unloaded
AI_{SS}	1.5	mA/channel max	Outputs unloaded
DI_{CC}	1	µA max	$V_{IH} = DV_{CC}$, V_{IL} = GND, 0.5 µA typ
Power Dissipation	TBD	mW typ	±12 V operation, outputs unloaded
Power-Down Currents			All DAC channels and internal reference powered-down
AI_{DD}	80	µA typ	
AI_{SS}	TBD	µA typ	
DI_{CC}	TBD	µA typ	

[1] For specified performance minimum headroom requirement is 0.9V
[2] Guaranteed by characterization. Not production tested.

SINGLE SUPPLY SPECIFICATIONS

AV_{DD} = 4.5 V[1] to 16.5 V, AV_{SS} = 0 V, GND = 0 V, REFIN= 2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX}, 10 V range unless otherwise noted.

Table 3.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY			Outputs unloaded
Resolution			
AD5754R	16	Bits	
AD5734R	14	Bits	
AD5724R	12	Bits	
Total Unadjusted Error (TUE)	0.1	% FSR max	Across temperature and supplies
Relative Accuracy (INL)			
B Grade	±16	LSB max	@ 16-bit resolution
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic (@ 16-bit resolution)
Zero-Scale Error	+10	mV max	@ 25°C, error at other temperatures obtained using Zero-Scale TC
Zero-Scale TC[2]	±4	ppm FSR/°C max	
Offset Error	±10	mV max	
Gain Error	±0.02	% FSR max	@ 25°C, error at other temperatures obtained using Gain TC
Gain TC[2]	±8	ppm FSR/°C max	
DC Crosstalk[2]	0.6	LSB max	@ 16-bit resolution
REFERENCE INPUT/OUTPUT			
Reference Input[2]			
Reference Input Voltage	2.5	V nom	±1% for specified performance
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±10	µA max	Typically ±30 nA
Reference Range	2 to 3	V min to max	
Reference Output			
Output Voltage	2.498 to 2.502	V min to V max	@ 25°C
Reference TC	±5	ppm/°C max	
Output Noise (0.1 Hz to 10 Hz)[2]	18	µV p-p typ	
Noise Spectral Density[2]	75	nV/√Hz typ	@ 10 kHz
Output Drift vs. Time[2]	±40	ppm/500 hr typ	
	±50	ppm/1000 hr typ	
OUTPUT CHARACTERISTICS[2]			
Output Voltage Range	10.8	V max	AV_{DD} = 11.7 V min, REFIN = 2.5 V
	12	V max	AV_{DD} = 12.9 V min, REFIN = 3.75 V
Headroom	0.9	V max	
	0.5	V typ	
Output Voltage TC	±8	ppm FSR/°C max	
Output Voltage Drift vs. Time	±12	ppm/500 hr typ	
	±15	ppm/1000 hr typ	
Short Circuit Current	20	mA typ	
Load	2	KΩ min	For specified performance
Capacitive Load Stability	4000	pF max	
DC Output Impedance	0.5	Ω typ	
DIGITAL INPUTS[2]			DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage	0.8	V max	
Input Current	±1	µA max	Per pin
Pin Capacitance	5	pF max	Per pin
DIGITAL OUTPUTS (SDO)[2]			
V_{OL}, Output Low Voltage	0.4	V max	DV_{CC} = 5 V ± 10%, sinking 200 µA

Parameter	Value	Unit	Test Conditions/Comments
V_{OH}, Output High Voltage	DV_{CC} – 1	V min	DV_{CC} = 5 V ± 10%, sourcing 200 µA
V_{OL}, Output Low Voltage	0.4	V max	DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA
V_{OH}, Output High Voltage	DV_{CC} – 0.5	V min	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	µA max	
High Impedance Output Capacitance	5	pF typ	
POWER REQUIREMENTS			
AV_{DD}	4.5 to 16.5	V min to V max	
DV_{CC}	2.7 to 5.5	V min to V max	
Power Supply Sensitivity[2]			
$\Delta V_{OUT}/\Delta AV_{DD}$	−75	dB typ	200mV sine wave superimposed on AV_{DD} @ 50/60 Hz
AI_{DD}	2.75	mA/channel max	Outputs unloaded
DI_{CC}	1	µA max	V_{IH} = DV_{CC}, V_{IL} = GND, 0.5 µA typ
Power Dissipation	TBD	mW typ	12 V operation, outputs unloaded
Power-down currents			All DAC channels and internal reference powered-down
AI_{DD}	80	µA typ	
DI_{CC}	TBD	µA typ	

[1] For specified performance minimum headroom requirement is 0.9V
[2] Guaranteed by characterization. Not production tested.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 4.5[1] V to 16.5 V, AV_{SS} = −4.5[1] V to −16.5 V / 0V, GND = 0 V, REFIN= 2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX}, ±10 V range unless otherwise noted.

Table 4.

Parameter[2]	B Grade	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	8	µs typ	Full-scale step (20 V) to ±0.03 % FSR
	10	µs max	
	5	µs typ	512 LSB step settling (@ 16 bits)
Slew Rate	4.5	V/µs typ	
Digital-to-Analog Glitch Energy	35	nV-sec typ	
Glitch Impulse Peak Amplitude	25	mV typ	
Digital Crosstalk	10	nV-sec typ	
DAC-to-DAC Crosstalk	10	nV-sec typ	
Digital Feedthrough	0.1	nV-sec typ	
Output Noise (0.1 Hz to 10 Hz Bandwidth)	0.05	LSB p-p typ	@ 16 bit resolution
Output Noise (100 kHz Bandwidth)	80	µV rms typ	
1/f Corner Frequency	1	kHz typ	
Output Noise Spectral Density	120	nV/√Hz typ	Measured at 10 kHz

[1] For specified performance headroom requirement is 0.9V
[2] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 4.5 V to 16.5 V, AV_{SS} = −4.5 V to −16.5 V / 0V, GND = 0 V, REFIN = 2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	100	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	0	ns min	Data hold time
t_9	20	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{10}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	20	ns min	$\overline{LDAC}$ pulse width low
t_{12}	1.5	µs max	$\overline{LDAC}$ falling edge to DAC output response time
t_{13}	10	µs max	DAC output settling time
t_{14}	1.5	µs max	$\overline{SYNC}$ rising edge to output response time ($\overline{LDAC}$ = 0)
t_{15}	20	ns min	$\overline{CLR}$ pulse width low
t_{16}	2.5	µs max	$\overline{CLR}$ pulse activation time
t_{17}[4]	13	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{18}[4]	40	ns max	SCLK rising edge to SDO valid ($C_{L\ SDO}$[5] = 15 pF)
t_{19}	200	ns min	Minimum $\overline{SYNC}$ high time (readback/daisy-chain mode)

[1] Guaranteed by characterization. Not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] Daisy-chain and Readback mode.
[5] $C_{L\ SDO}$ = Capacitive load on SDO output.

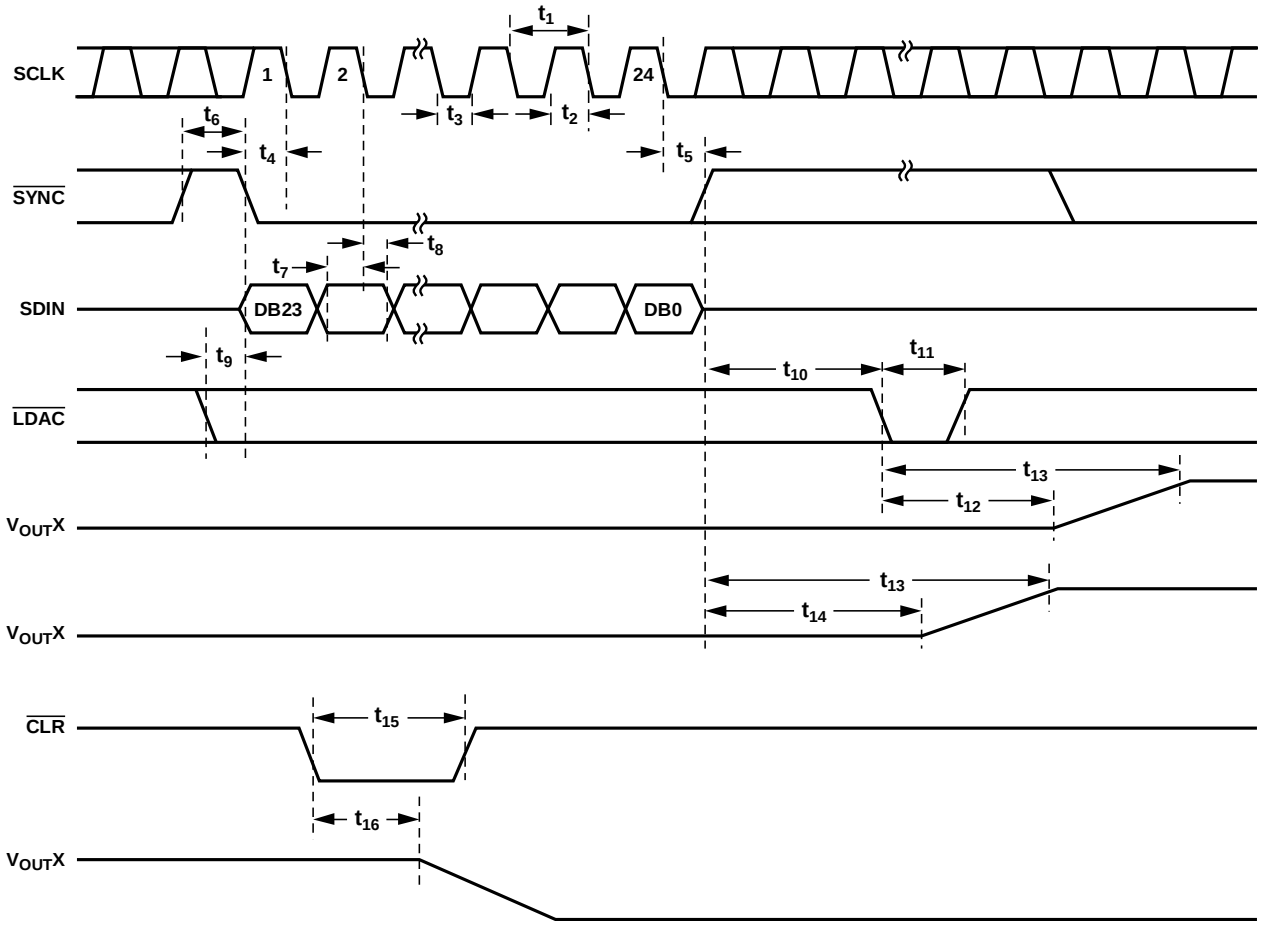


Figure 2. Serial Interface Timing Diagram

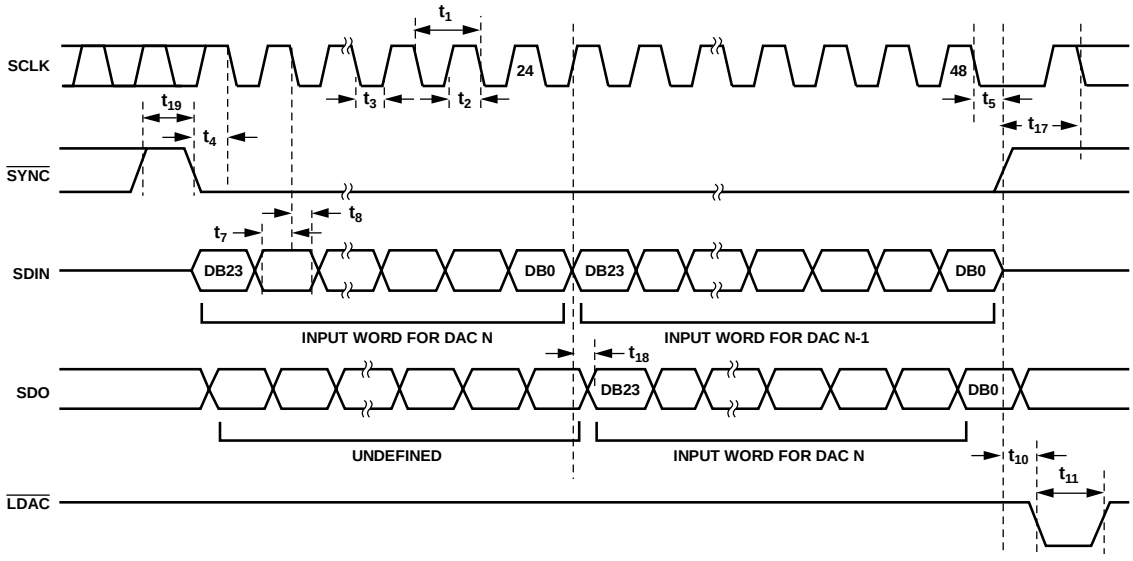


Figure 3. Daisy Chain Timing Diagram

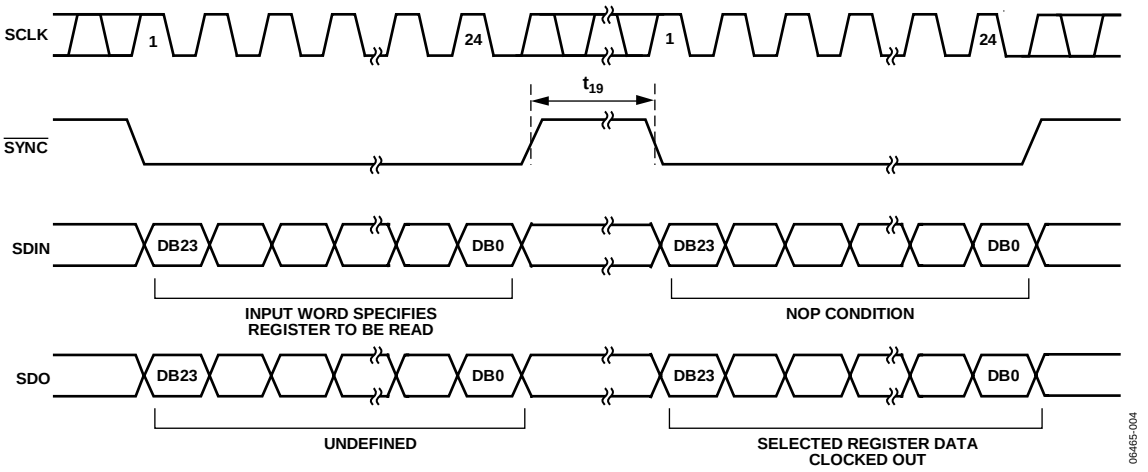


Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 6.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +17 V
AV_{SS} to GND	+0.3 V to −17 V
DV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7V (whichever is less)
REFIN/REFOUT to GND	−0.3 V to +17 V
$V_{OUT}A$, $V_{OUT}B$, $V_{OUT}C$, $V_{OUT}D$ to GND	AV_{SS} to AV_{DD}
DAC_GND to GND	-0.3V to +0.3V
SIG_GND to GND	-0.3V to +0.3V
Operating Temperature Range, T_A	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, T_J max	105°C
24-Lead TSSOP Package	
θ_{JA} Thermal Impedance	90°C/W
Power Dissipation	(T_J max – T_A)/ θ_{JA}
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

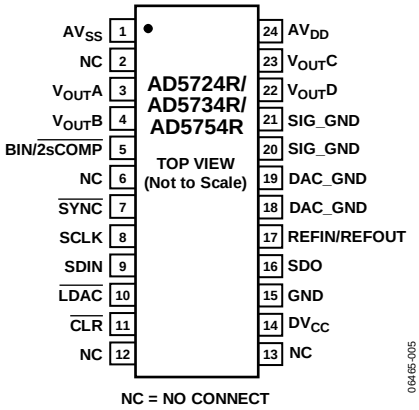


Figure 5.Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from –4.5 V to –16.5 V. This pin can be connected to 0 V if output ranges are unipolar.
2, 6, 12, 13	NC	Do not connect to these pins.
3	$V_{OUT}A$	Analog Output Voltage of DAC A. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
4	$V_{OUT}B$	Analog Output Voltage of DAC B. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
5	BIN/$\overline{2sCOMP}$	Determines the DAC coding for a bipolar output range. This pin should be hardwired to either DV_{CC} or GND. When hardwired to DV_{CC}, input coding is offset binary. When hardwired to GND, input coding is twos complement. (For unipolar output ranges, coding is always straight binary).
7	$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	$\overline{LDAC}$	Load DAC, Logic Input. This is used to update the DAC registers and consequently, the analog output. When tied permanently low, the addressed DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the output update is held off until the falling edge of $\overline{LDAC}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin should not be left unconnected.
11	$\overline{CLR}$[1]	Active Low Input. Asserting this pin sets the DAC registers to zero-scale code or mid-scale code (user-selectable).
14	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
15	GND	Ground Reference Pin.
16	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
17	REFIN/REFOUT	External Reference Voltage Input and Internal Reference Voltage Output. Reference input range is 2 V to 3 V. REFIN = 2.5 V for specified performance. REFOUT = 2.5 V ± 2 mV @ 25°C.
18, 19	DAC_GND	Ground reference pins for the four digital-to-analog converters.
20, 21	SIG_GND	Ground reference pins for the four output amplifiers.
22	$V_{OUT}D$	Analog Output Voltage of DAC D. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
23	$V_{OUT}C$	Analog Output Voltage of DAC C. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
24	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 4.5 V to 16.5 V.
Exposed Paddle	AV_{SS}	Negative Analog Supply connection. Voltage ranges from –4.5 V to –16.5 V. This paddle can be connected to 0 V if output ranges are unipolar.

[1] Internal pull-up device on this logic input. Therefore, it can be left floating and defaults to a logic high.

TYPICAL PERFORMANCE CHARACTERISTICS

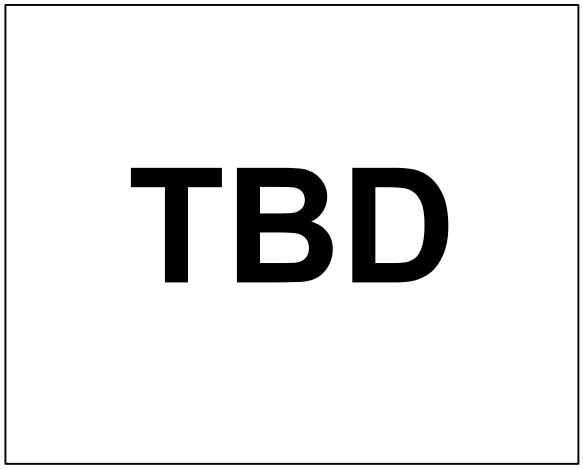


Figure 6. AD5754R Integral Nonlinearity Error vs. Code (Four Traces)

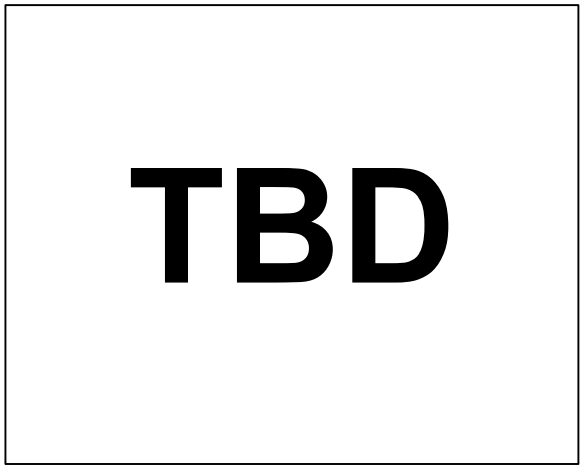


Figure 7. AD5734R Integral Nonlinearity Error vs. Code (Four Traces)

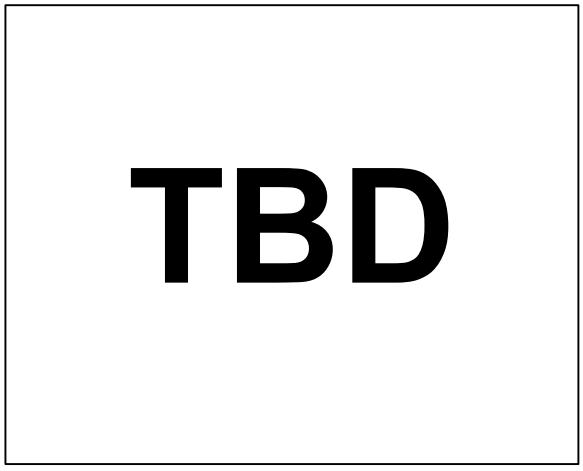


Figure 8. AD5724R Integral Nonlinearity Error vs. Code (Four Traces)

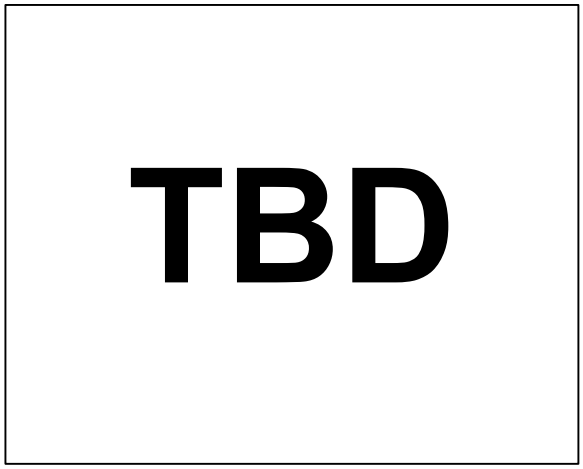


Figure 9. AD5754R Differential Nonlinearity Error vs. Code (Four Traces)

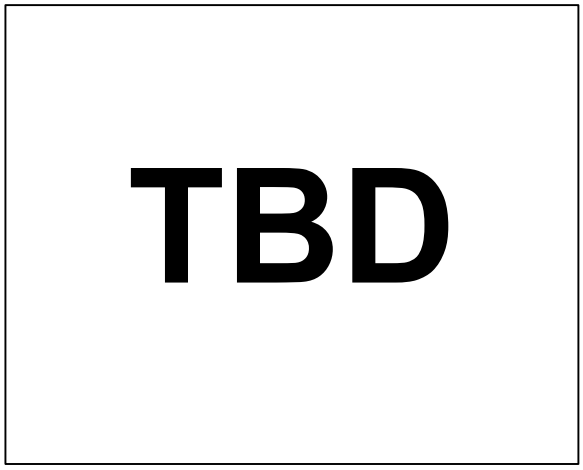


Figure 10. AD5734R Differential Nonlinearity Error vs. Code (Four Traces)

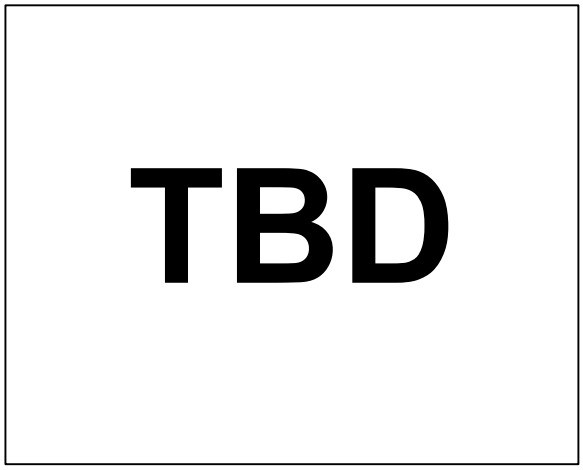


Figure 11. AD5724R Differential Nonlinearity Error vs. Code (Four Traces)

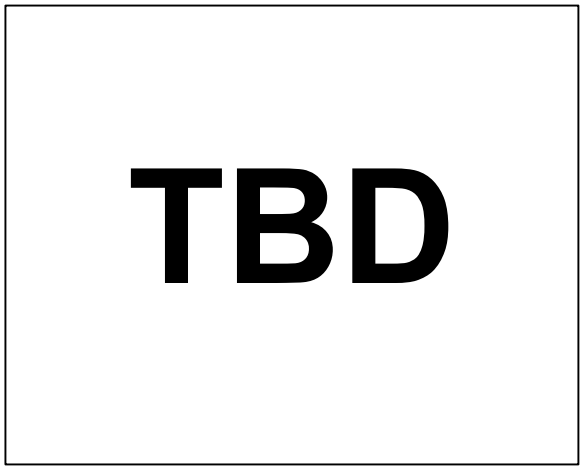


Figure 12. AD5754R Integral Nonlinearity Error vs. Temperature (Four Traces)

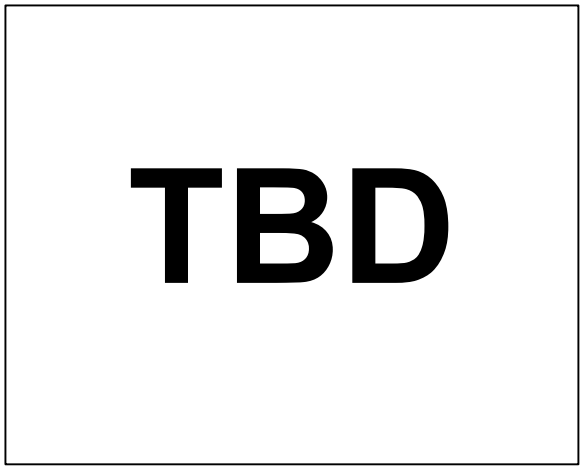


Figure 13. AD5754R Differential Nonlinearity Error vs. Temperature (Four Traces)

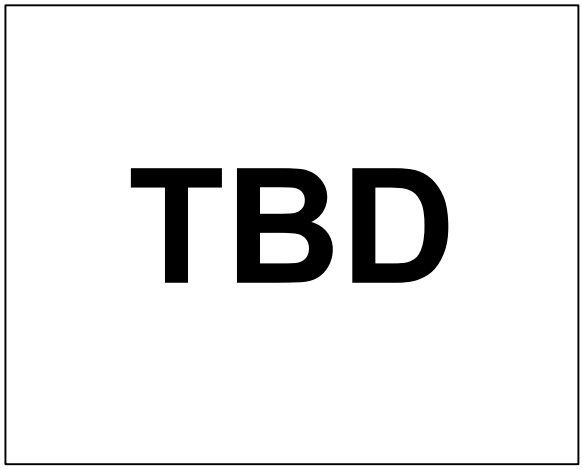


Figure 14. AD5754R Integral Nonlinearity Error vs. Supply Voltage (Four Traces)

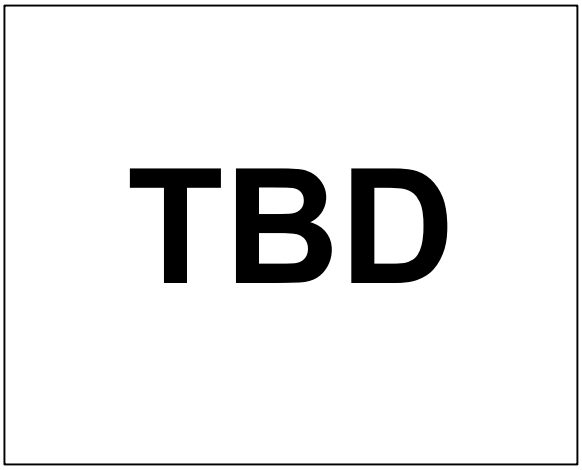


Figure 15.AD5754R Differential Nonlinearity Error vs. Supply Voltage (Four Traces)

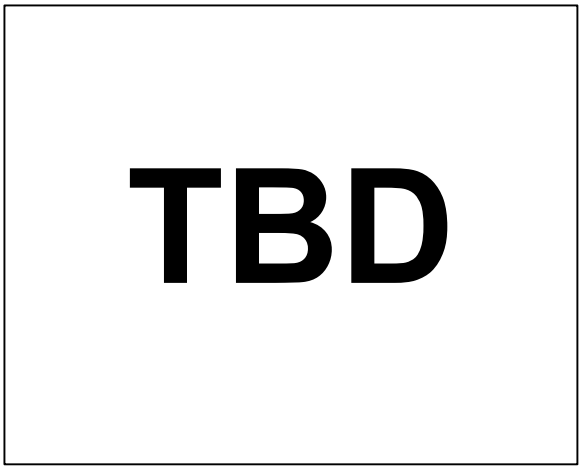


Figure 16. AD5754R Integral Nonlinearity Error vs. Reference Voltage (Four Traces)

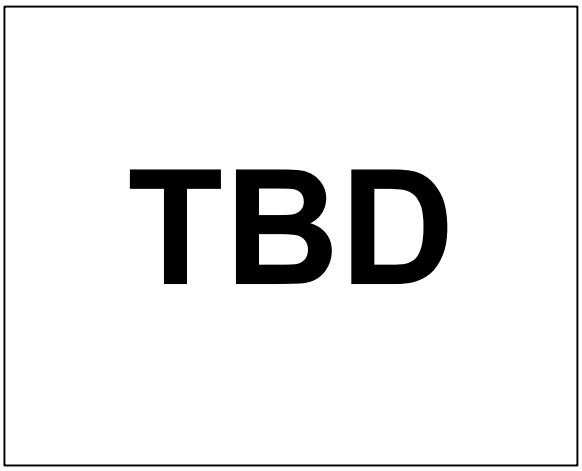


Figure 17. AD5754R Differential Nonlinearity vs. Reference Voltage (Four Traces)

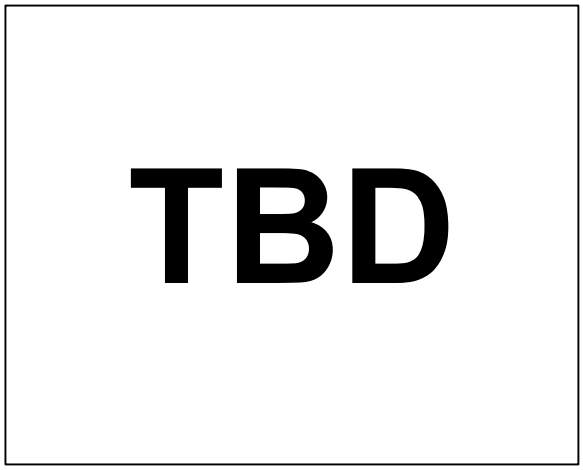


Figure 18. AD5754R Total Unadjusted Error vs. Reference Voltage (Four Traces)

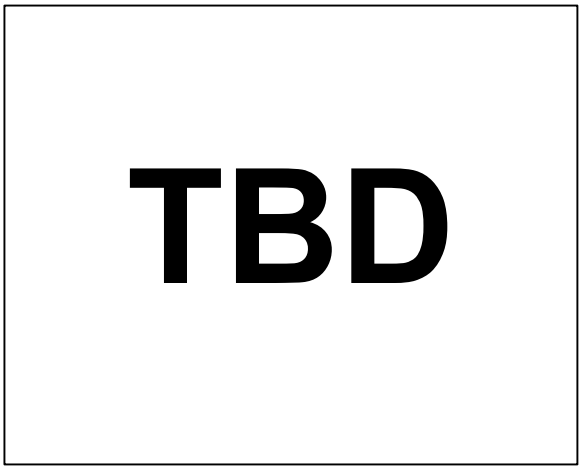


Figure 21. AI_{DD} vs. AV_{DD}

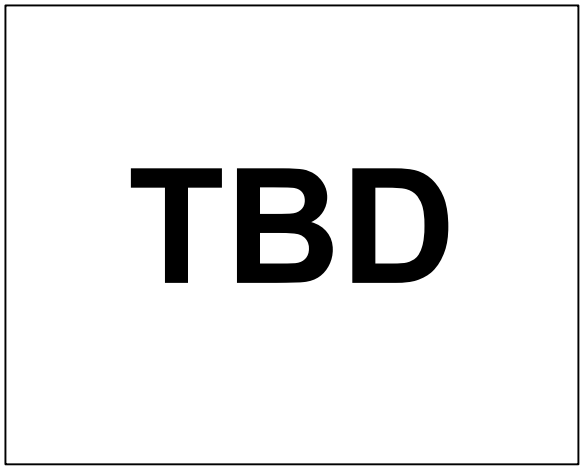


Figure 19. AD5754R Total Unadjusted Error vs. Supply Voltage (Four Traces)

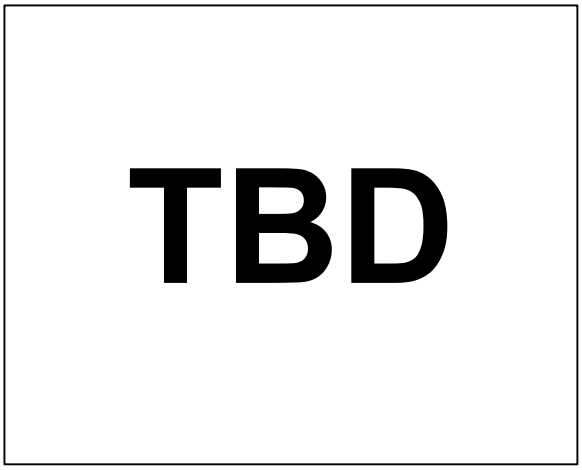


Figure 22. Zero-Scale Error vs. Temperature (Four Traces)

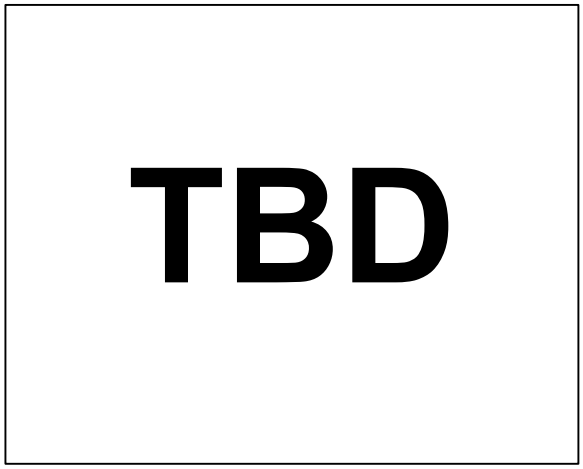


Figure 20. AI_{DD}/AI_{SS} vs. AV_{DD}/AV_{SS}

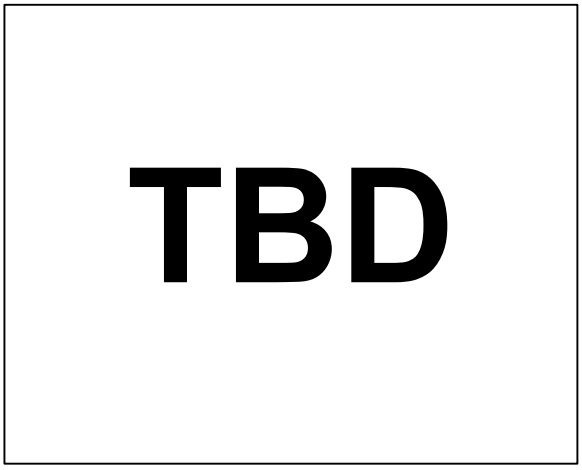


Figure 23. Bipolar Zero Error vs. Temperature (Two Traces)

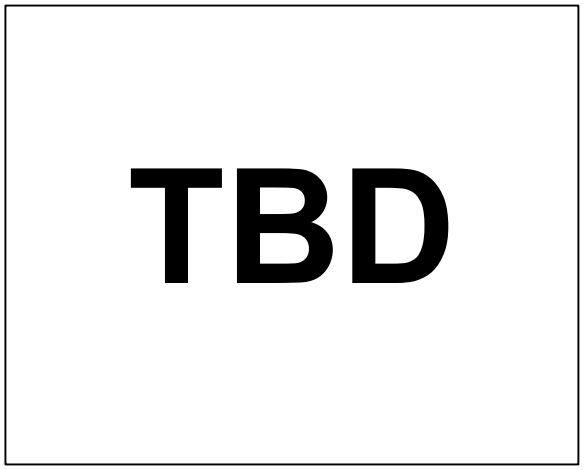


Figure 24. Gain Error vs. Temperature (Four Traces)

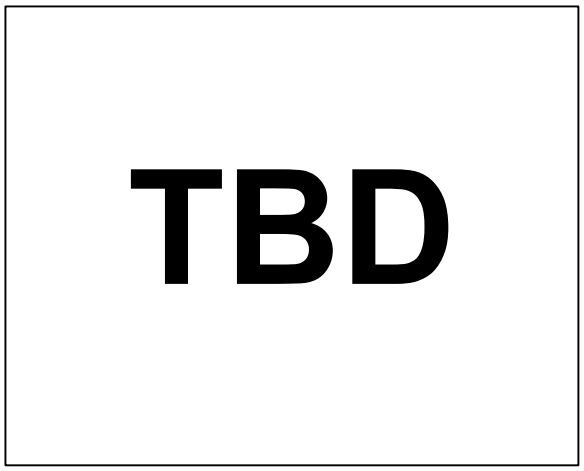


Figure 25. DI_{CC} vs. Logic Input Voltage Increasing and Decreasing

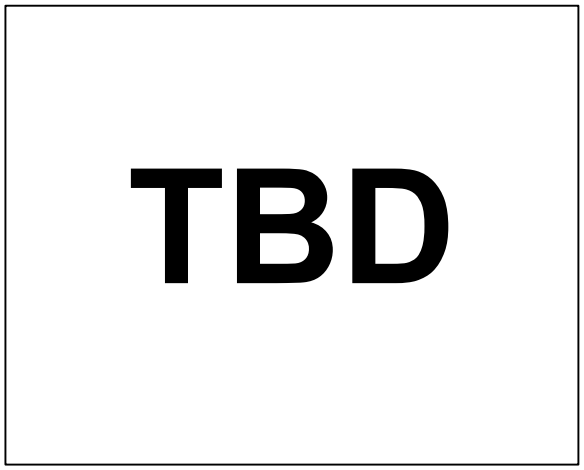


Figure 26. Output Amplifier Source and Sink Capability (Four Traces)

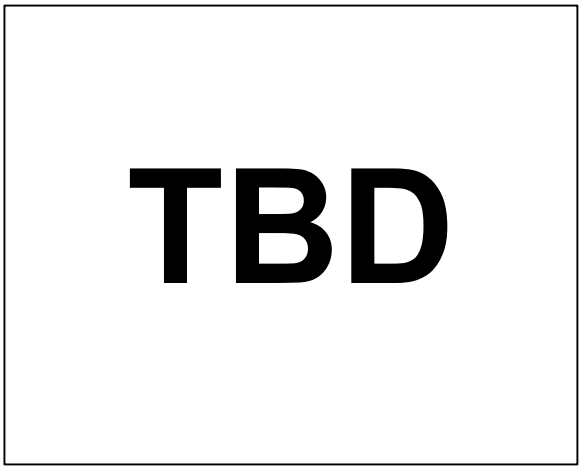


Figure 27. Full-Scale Settling Time, ±10 V Range (Two Traces)+ve & -ve

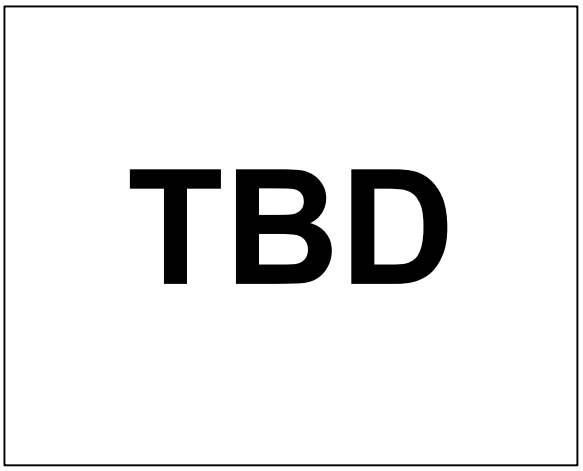


Figure 28. Full-Scale Settling Time, ±5 V Range (Two Traces)

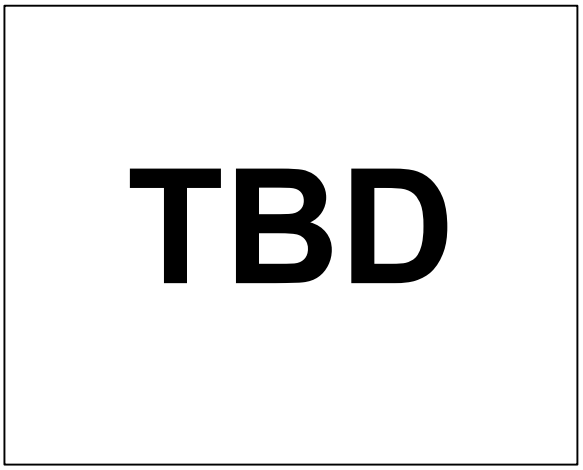


Figure 29. Full-Scale Settling Time, +10 V Range (Two Traces)

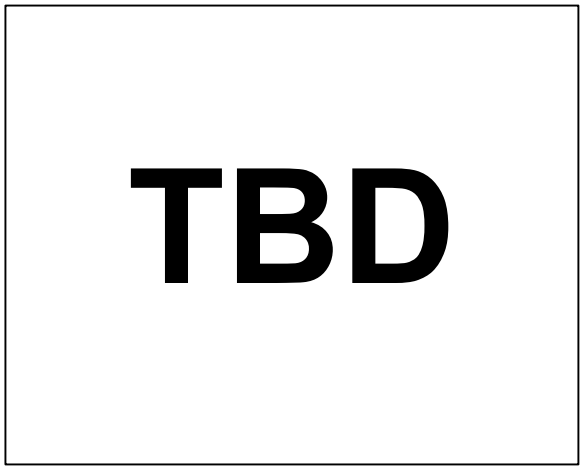


Figure 30. Full-Scale Settling Time, +5 V Range (Two Traces)

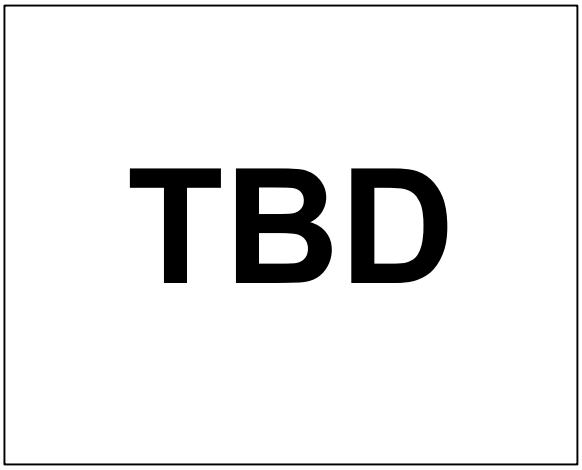


Figure 33. Peak-to-Peak Noise, 100 kHz Bandwidth, (Four Traces)

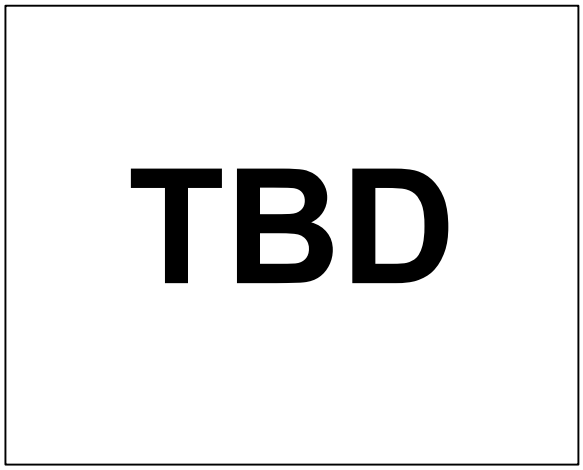


Figure 31. Digital-to-Analog Glitch Energy (Four Traces)

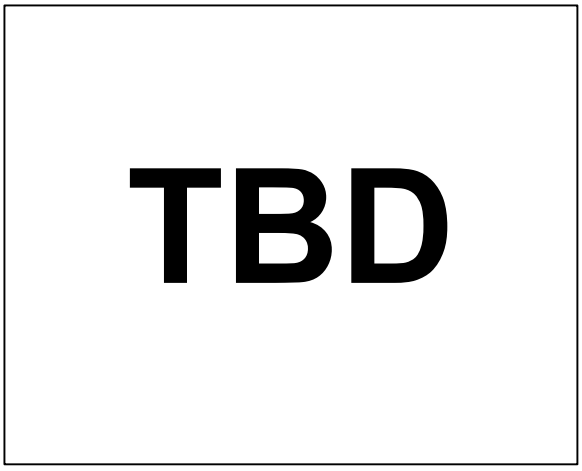


Figure 34. V_{OUT} vs. AV_{DD}/AV_{SS} on Power Up (Two Traces) (single and dual)

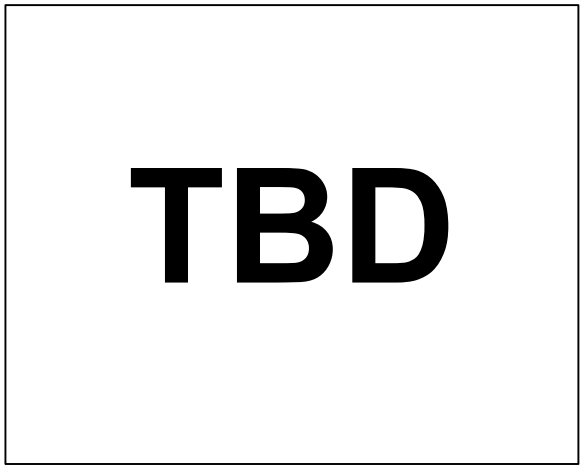


Figure 32. Peak-to-Peak Noise, 0.1 Hz to 10 Hz Bandwidth (Four Traces)

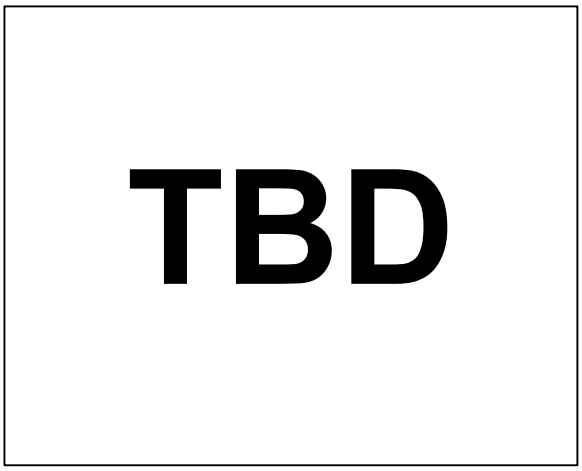


Figure 35. REFOUT Turn-On Transient

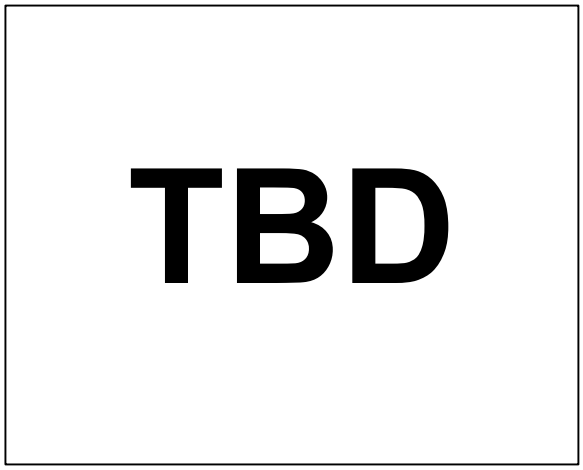


Figure 36. REFOUT Output Noise (100 kHz Bandwidth)

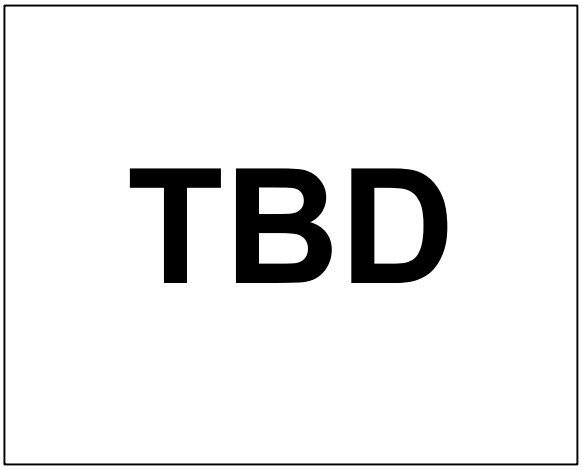


Figure 39. REFOUT Load Transient (Two Traces)

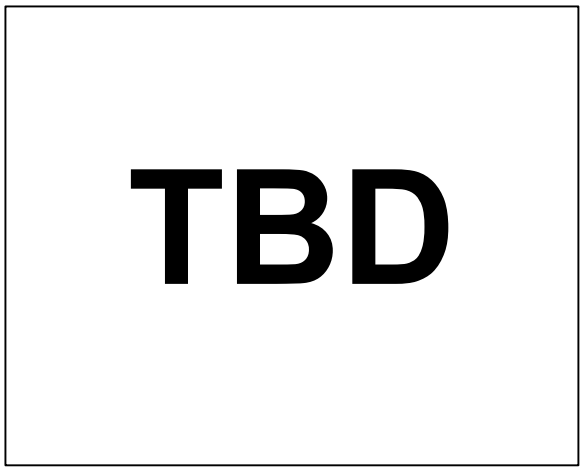


Figure 37. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

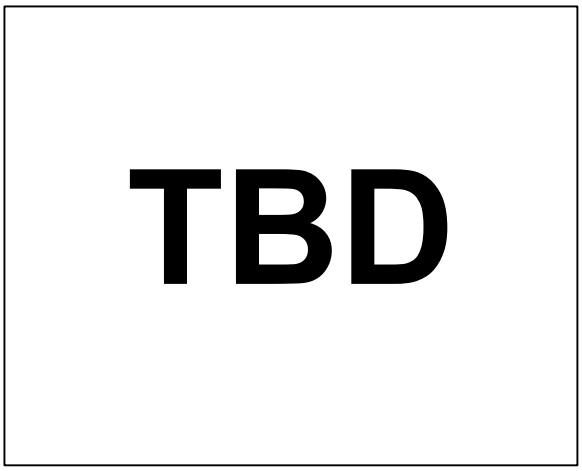


Figure 40. REFOUT Histogram of Thermal Hysteresis

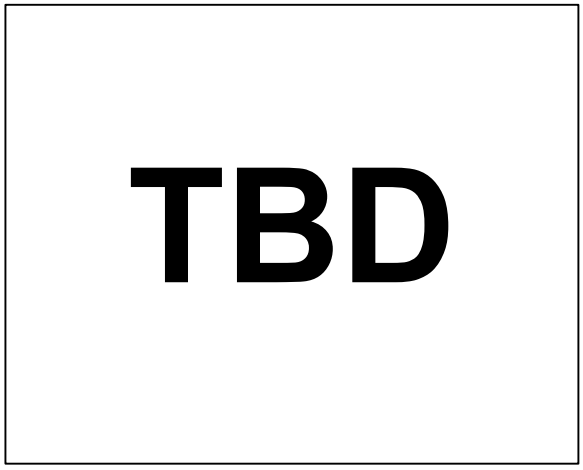


Figure 38. REFOUT Line Transient (Two Traces)

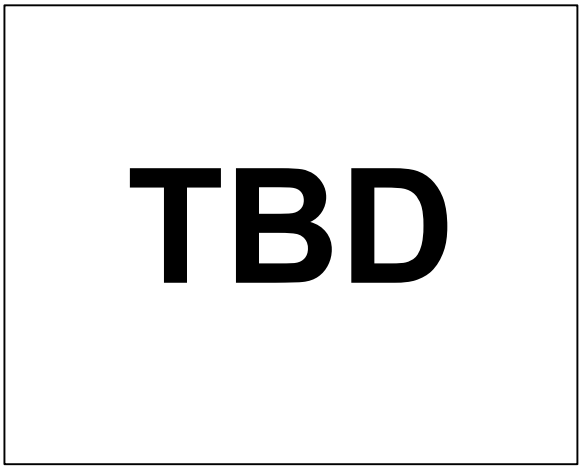


Figure 41. REFOUT Voltage vs. Load Current

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 6.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 9.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5724R/ AD5734R/AD5754R are monotonic over their full operating temperature range.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 23.

Bipolar Zero TC
Bipolar Zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Zero-Scale Error/Negative Full-Scale Error
Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be negative full-scale – 1 LSB. A plot of zero-scale error vs. temperature can be seen in Figure 22.

Zero-Scale TC
This is a measure of the change in zero-scale error with a change in temperature. Zero-Scale TC is expressed in ppm FSR/°C.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. A plot of settling time can be seen in Figure 27.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage output D/A converter is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/μs.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Figure 24.

Gain TC
This is a measure of the change in gain error with changes in temperature. Gain TC is expressed in ppm FSR/°C.

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 31.

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 31.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Sensitivity
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage, it is measured by superimposing a 50/60Hz, 200mVpk-pk sine wave on the supply voltages and measuring the proportion of the sine wave that transfers to the outputs.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in LSBs.

Digital Crosstalk

Digital crosstalk is a measure of the impulse injected into the analog output of one DAC from the digital inputs of another DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Voltage Reference TC

Reference TC is a measure of the change in the reference output voltage with a change in temperature. It is expressed in ppm/°C.

THEORY OF OPERATION

The AD5724R/AD5734R/AD5754R are quad, 12-/14-/16-bit, serial input, unipolar/bipolar, voltage output DACs. They operate from single supply voltages of +4.5 V to +16.5 V or dual supply voltages of ±4.5 V to ±16.5 V. In addition, the parts have software-selectable output ranges of +5 V, +10 V, +10.8 V, ±5 V, ±10 V, and ±10.8 V. Data is written to the AD5724R/AD5734R/AD5754R in a 24-bit word format via a 3-wire serial interface. The devices also offer an SDO pin to facilitate daisy chaining or readback.

The AD5724R/AD5734R/AD5754R incorporate a power-on reset circuit to ensure that the DAC registers power up loaded with 0x0000. When powered on, the outputs are clamped to 0 V via a low impedance path. The parts also feature on-chip reference and reference buffers.

ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 42 shows a block diagram of the DAC architecture. The reference input is buffered before being applied to the DAC.

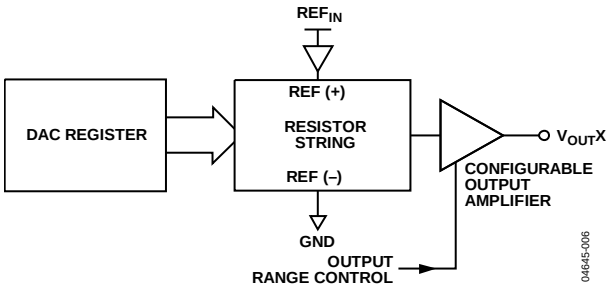


Figure 42. DAC Architecture Block Diagram

The resistor string structure is shown in Figure 43. It is a string of resistors, each of value R. The code loaded to the DAC register determines the node on the string where the voltage is to be tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

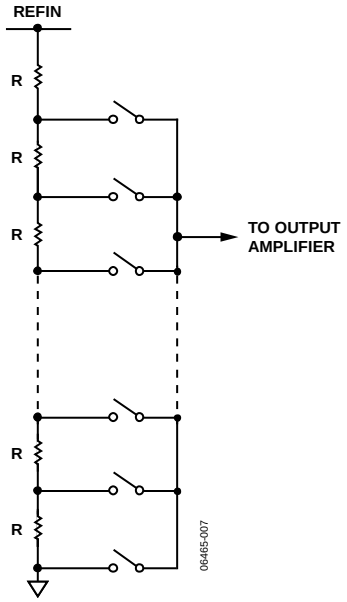


Figure 43. Resistor String Structure

Output Amplifiers

The output amplifiers are capable of generating both unipolar and bipolar output voltages. They are capable of driving a load of 2 kΩ in parallel with 4000 pF to GND. The source and sink capabilities of the output amplifiers can be seen in Figure 26. The slew rate is 4.5 V/μs with a full-scale settling time of 10 μs.

Reference Buffers

The AD5724R/AD5734R/AD5754R can operate with either an external or internal reference. The reference input has an input range of 2 V to 3 V with 2.5 V for specified performance. This input voltage is then buffered before it is applied to the DAC cores.

SERIAL INTERFACE

The AD5724R/AD5734R/AD5754R are controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with SPI®, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of a read/write bit, three register select bits, three DAC address bits, and 16 data bits. The timing diagram for this operation is shown in Figure 2.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if SYNC is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and SYNC must be taken high after the final clock to latch the data. The first falling edge of SYNC starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before SYNC is brought high again. If SYNC is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before SYNC is brought high, the input data is also invalid. The input register addressed is updated on the rising edge of SYNC. For another serial transfer to take place, SYNC must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.

When the data has been transferred into the chosen register of the addressed DAC, all DAC registers and outputs can be updated by taking LDAC low while SYNC is high.

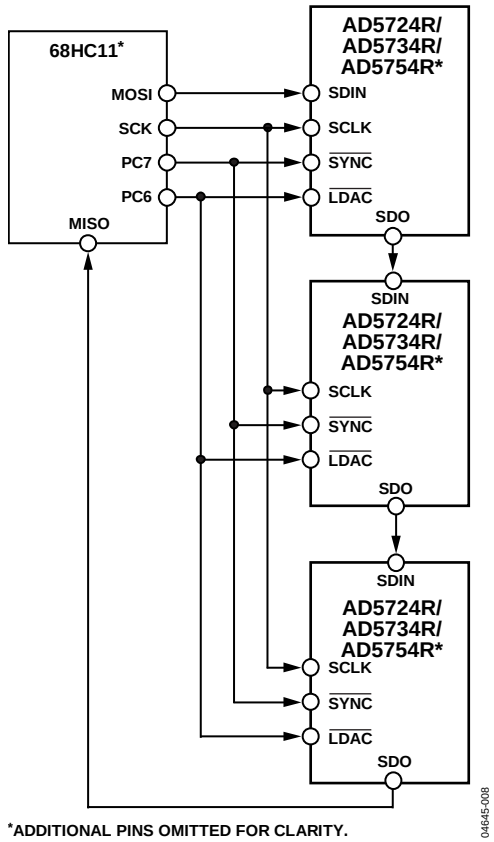


Figure 44. Daisy Chaining the AD5724R/AD5734R/AD5754R

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy chain several devices together. Daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of SYNC starts the write cycle. SCLK is continuously applied to the input shift register when SYNC is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × *N*, where *N* is the total number of AD5724R/AD5734R/AD5754R devices in the chain. When the serial transfer to all devices is complete, SYNC is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can only be used if SYNC is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and SYNC must be taken high after the final clock to latch the data.

Readback Operation

Readback mode is invoked by setting the R/$\overline{W}$ bit = 1 in the serial input register write. (If the SDO output is disabled via the SDO DISABLE bit in the control register, it is automatically enabled for the duration of the read operation after which it is disabled again) With R/$\overline{W}$ = 1, Bit A2 to Bit A0 in association with Bit REG2 to Bit REG0 select the register to be read. The remaining data bits in the write sequence are don't care bits. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the data register of Channel A, the following sequence should be implemented:

1. Write 0x800000 to the AD5724R/AD5734R/AD5754R input register. This configures the part for read mode with the data register of Channel A selected. Note that all the data bits, DB15 to DB0, are don't care bits.
2. Follow this with a second write, a NOP condition, 0x180000. During this write, the data from the register is clocked out on the SDO line.

LOAD DAC ($\overline{\text{LDAC}}$)

After data has been transferred into the input register of the DACs, there are two ways to update the DAC registers and DAC outputs. Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, one of two update modes is selected, individual DAC updating or simultaneous updating of all DACs.

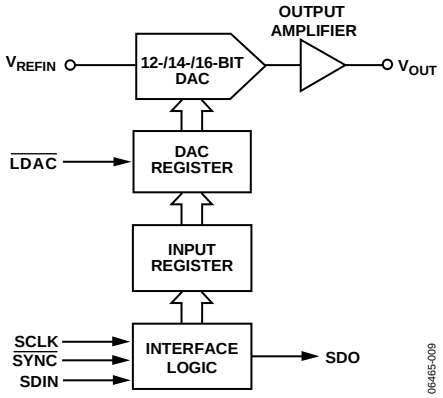


Figure 45. Simplified Diagram of Input Loading Circuitry for One DAC

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. All DAC outputs are asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

ASYNCHRONOUS CLEAR ($\overline{\text{CLR}}$)

$\overline{\text{CLR}}$ is an active low clear that allows the outputs to be cleared to either zero-scale code or mid-scale code. The clear code value is user-selectable via the CLR SELECT bit of the control register (see the Control Register section). It is necessary to maintain $\overline{\text{CLR}}$ low for a minimum amount of time to complete the operation (see Figure 2). When the $\overline{\text{CLR}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the $\overline{\text{CLR}}$ pin is low. A clear operation can also be performed via the clear command in the control register.

CONFIGURING THE AD5724R/AD5734R/AD5754R

When the power supplies are applied to the AD5724R/AD5734R/AD5754R, the power-on reset circuit ensures that all registers default to 0. This places all channels and the internal reference in power-down mode. The first communication to the AD5724R/AD5734R/AD5754R should be to set the required output range on all channels (default range is the 5 V unipolar range) by writing to the range select register. The user should then write to the power-control register to power-on the required channels and the internal reference, if required. If an external reference source is being used, the internal reference must remain in power-down mode. To program an output value on a channel, that channel must first be powered up; any writes to a channel while it is in power down mode are ignored. The AD5724R/AD5734R/AD5754R operate with a wide power supply range. It is important that the power supply applied to the parts provides adequate headroom to support the chosen output ranges.

TRANSFER FUNCTION

Table 9 to Table 17 show the relationships of the ideal input code to output voltage for the AD5754R, AD5734R, and AD5724R, respectively, for all output voltage ranges. For unipolar output ranges, the data coding is straight binary. For bipolar output ranges, the data coding is user-selectable via the BIN/$\overline{\text{2sCOMP}}$ pin and can be either offset binary or twos complement.

For a unipolar output range, the output voltage expression is given by

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right]$$

For a bipolar output range, the output voltage expression is given by

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right] - \frac{Gain \times V_{REFIN}}{2}$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.
V_{REFIN} is the reference voltage applied at the REFIN pin.
Gain is an internal gain the value of which depends on the output range selected by the user as shown in Table 8.

Table 8.

Output Range (V)	Gain Value
+5	2
+10	4
+10.8	4.32
±5	4
±10	8
±10.8	8.64

Ideal Output Voltage to Input Code Relationship—AD5754R

Table 9. Bipolar Output, Offset Binary Coding

Digital Input				Analog Output		
MSB			**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
1111	1111	1111	1111	+2 REFIN(32767/32768)	+4 REFIN(32767/32768)	+4.32 REFIN(32767/32768)
1111	1111	1111	1110	+2 REFIN(32766/32768)	+4 REFIN(32766/32768)	+4.32 REFIN(32766/32768)
–	–	–	–	–	–	–
1000	0000	0000	0001	+2 REFIN(1/32768)	+4 REFIN(1/32768)	+4.32 REFIN(1/32768)
1000	0000	0000	0000	0 V	0 V	0 V
0111	1111	1111	1111	−2 REFIN(1/32768)	−4 REFIN(1/32768)	−4.32 REFIN(32766/32768)
–	–	–	–	–	–	–
0000	0000	0000	0001	−2 REFIN(32766/32768)	−4 REFIN(32766/32768)	−4.32 REFIN(32766/32768)
0000	0000	0000	0000	−2 REFIN(32767/32768	−4 REFIN(32767/32768)	−4.32 REFIN(32767/32768)

Table 10. Bipolar Output, Twos Complement Coding

Digital Input				Analog Output		
MSB			**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
0111	1111	1111	1111	+2 REFIN(32767/32768)	+4 REFIN(32767/32768)	+4.32 REFIN(32767/32768)
0111	1111	1111	1110	+2 REFIN(32766/32768)	+4 REFIN(32766/32768)	+4.32 REFIN(32766/32768)
–	–	–	–	–	–	–
0000	0000	0000	0001	+2 REFIN(1/32768)	+4 REFIN(1/32768)	+4.32 REFIN(1/32768)
0000	0000	0000	0000	0 V	0 V	0 V
1111	1111	1111	1111	−2 REFIN(1/32768)	−4 REFIN(1/32768)	−4.32 REFIN(1/32768)
–	–	–	–	–	–	–
1000	0000	0000	0001	−2 REFIN(32766/32768)	−4 REFIN(32766/32768)	−4.32 REFIN(32766/32768)
1000	0000	0000	0000	−2 REFIN(32767/32768)	−4 REFIN(32767/32768)	−4.32 REFIN(32767/32768)

Table 11. Unipolar Output, Straight Binary Coding

Digital Input				Analog Input		
MSB			**LSB**	**+5 V Output Range**	**+10 V Output Range**	**+10.8 V Output Range**
1111	1111	1111	1111	+2 REFIN(65535/65536)	+4 REFIN(65535/65536)	+4.32 REFIN(65535/65536)
1111	1111	1111	1110	+2 REFIN(65534/65536)	+4 REFIN(65534/65536)	+4.32 REFIN(65534/65536)
–	–	–	–	–	–	–
1000	0000	0000	0001	+2 REFIN(32769/65536)	+4 REFIN(32769/65536)	+4.32 REFIN(32769/65536)
1000	0000	0000	0000	+2 REFIN(32768/65536)	+4 REFIN(32768/65536)	+4.32 REFIN(32768/65536)
0111	1111	1111	1111	+2 REFIN(32767/65536)	+4 REFIN(32767/65536)	+4.32 REFIN(32767/65536)
–	–	–	–	–	–	–
0000	0000	0000	0001	+2 REFIN(1/65536)	+4 REFIN(1/65536)	+4.32 REFIN(1/65536)
0000	0000	0000	0000	0 V	0 V	0 V

Ideal Output Voltage to Input Code Relationship—AD5734R

Table 12. Bipolar Output, Offset Binary Coding

Digital Input				Analog Output		
MSB			**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
11	1111	1111	1111	+2 REFIN(8191/8192)	+4 REFIN(8191/8192)	+4.32 REFIN(8191/8192)
11	1111	1111	1110	+2 REFIN(8190/8192)	+4 REFIN(8190/8192)	+4.32 REFIN(8190/8192)
–	–	–	–	–	–	–
10	0000	0000	0001	+2 REFIN(1/8192)	+4 REFIN(1/8192)	+4 REFIN(1/8192)
10	0000	0000	0000	0 V	0 V	0 V
01	1111	1111	1111	−2 REFIN(1/8192)	−4 REFIN(1/8192)	−4.32 REFIN(1/8192)
–	–	–	–	–	–	–
00	0000	0000	0001	−2 REFIN(8190/8192)	−4 REFIN(8190/8192)	−4.32 REFIN(8190/8192)
00	0000	0000	0000	−2 REFIN(8191/8191)	−4 REFIN(8191/8192)	−4.32 REFIN(8191/8192)

Table 13. Bipolar Output, Twos Complement Coding

Digital Input				Analog Output		
MSB			**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
01	1111	1111	1111	+2 REFIN(8191/8192)	+4 REFIN(8191/8192)	+4.32 REFIN(8191/8192)
01	1111	1111	1110	+2 REFIN(8190/8192)	+4 REFIN(8190/8192)	+4.32 REFIN(8190/8192)
–	–	–	–	–	–	–
00	0000	0000	0001	+2 REFIN(1/8192)	+4 REFIN(1/8192)	+4 REFIN(1/8192)
00	0000	0000	0000	0 V	0 V	0 V
11	1111	1111	1111	−2 REFIN(1/8192)	−4 REFIN(1/8192)	−4.32 REFIN(1/8192)
–	–	–	–	–	–	–
10	0000	0000	0001	−2 REFIN(8190/8192)	−4 REFIN(8190/8192)	−4.32 REFIN(8190/8192)
10	0000	0000	0000	−2 REFIN(8191/8192)	−4 REFIN(8191/8192)	−4.32 REFIN(8191/8192)

Table 14. Unipolar Output, Straight Binary Coding

Digital Input				Analog Output		
MSB			**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
11	1111	1111	1111	+2 REFIN(16383/16384)	+4 REFIN(16383/16384)	+4.32 REFIN(16383/16384)
11	1111	1111	1110	+2 REFIN(16382/16384)	+4 REFIN(16382/16384)	+4.32 REFIN(16382/16384)
–	–	–	–	–	–	–
10	0000	0000	0001	+2 REFIN(8193/16384)	+4 REFIN(8193/16384)	+4.32 REFIN(8193/16384)
10	0000	0000	0000	+2 REFIN(8192/16384)	+4 REFIN(8192/16384)	+4.32 REFIN(8192/16384)
01	1111	1111	1111	+2 REFIN(8191/16384)	+4 REFIN(8191/16384)	+4.32 REFIN(8191/16384)
–	–	–	–	–	–	–
00	0000	0000	0001	+2 REFIN(1/16384)	+4 REFIN(1/16384)	+4.32 REFIN(1/16384)
00	0000	0000	0000	0 V	0 V	0 V

Ideal Output Voltage to Input Code Relationship—AD5724R

Table 15. Bipolar Output, Offset Binary Coding

Digital Input			Analog Output		
MSB		**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
1111	1111	1111	+2 REFIN(2047/2048)	+4 REFIN(2047/2048)	+4.32 REFIN(2047/2048)
1111	1111	1110	+2 REFIN(2046/2048)	+4 REFIN(2046/2048)	+4.32 REFIN(2046/2048)
–	–	–	–	–	–
1000	0000	0001	+2 REFIN(1/2048)	+4 REFIN(1/2048)	+4 REFIN(1/2048)
1000	0000	0000	0 V	0 V	0 V
0111	1111	1111	−2 REFIN(1/2048)	−4 REFIN(1/2048)	−4.32 REFIN(1/2048)
–	–	–	–	–	–
0000	0000	0001	−2 REFIN(2046/2048)	−4 REFIN(2046/2048)	−4.32 REFIN(2046/2048)
0000	0000	0000	−2 REFIN(2047/2047)	−4 REFIN(2047/2048)	−4.32 REFIN(2047/2048)

Table 16. Bipolar Output, Twos Complement Coding

Digital Output			Analog Output		
MSB		**LSB**	**±5 V Output Range**	**±10 V Output Range**	**±10.8 V Output Range**
0111	1111	1111	+2 REFIN(2047/2048)	+4 REFIN(2047/2048)	+4.32 REFIN(2047/2048)
0111	1111	1110	+2 REFIN(2046/2048)	+4 REFIN(2046/2048)	+4.32 REFIN(2046/2048)
–	–	–	–	–	–
0000	0000	0001	+2 REFIN(1/2048)	+4 REFIN(1/2048)	+4 REFIN(1/2048)
0000	0000	0000	0 V	0 V	0 V
1111	1111	1111	−2 REFIN(1/2048)	−4 REFIN(1/2048)	−4.32 REFIN(1/2048)
–	–	–	–	–	–
1000	0000	0001	−2 REFIN(2046/2048)	−4 REFIN(2046/2048)	−4.32 REFIN(2046/2048)
1000	0000	0000	−2 REFIN(2047/2048)	−4 REFIN(2047/2048)	−4.32 REFIN(2047/2048)

Table 17. Unipolar Output, Straight Binary Coding

Digital Input			Analog Output		
MSB		**LSB**	**+5 V Output Range**	**+10 V Output Range**	**+10.8 V Output Range**
1111	1111	1111	+2 REFIN(4095/4096)	+4 REFIN(4095/4096)	+4.32 REFIN(4095/4096)
1111	1111	1110	+2 REFIN(4094/4096)	+4 REFIN(4094/4096)	+4.32 REFIN(4094/4096)
–	–	–	–	–	–
1000	0000	0001	+2 REFIN(2049/4096)	+4 REFIN(2049/4096)	+4.32 REFIN(2049/4096)
1000	0000	0000	+2 REFIN(2048/4096)	+4 REFIN(2048/4096)	+4.32 REFIN(2048/4096)
0111	1111	1111	+2 REFIN(2047/4096)	+4 REFIN(2047/4096)	+4.32 REFIN(2047/4096)
–	–	–	–	–	–
0000	0000	0001	+2 REFIN(1/4096)	+4 REFIN(1/4096)	4.32 REFIN(1/4096)
0000	0000	0000	0 V	0 V	0 V

INPUT REGISTER

The input register is 24 bits wide and consists of a read/write bit, a reserved bit, three register select bits, three DAC address bits, and 12-/14-/16 data bits. The register data is clocked in MSB first on the SDIN pin. Table 18 shows the register format while Table 19 describes the function of each bit in the register. All registers are read/write registers.

Table 18. Input Register Format

MSB								LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB18**	**DB17**	**DB16**	**DB15 to DB0**
R/$\overline{W}$	0	REG2	REG1	REG0	A2	A1	A0	DATA

Table 19. Input Register Bit Functions

Bit Mnemonic	Description			
R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
REG2, REG1, REG0	Used in association with the address bits to determine if a write operation is to the data register, output range select register, power control register or control register.			
	REG2	**REG1**	**REG0**	**Function**
	0	0	0	Data Register
	0	0	1	Output Range Select Register
	0	1	0	Power Control Register
	0	1	1	Control Register
A2, A1, A0	These bits are used to decode the DAC channels.			
	A2	**A1**	**A0**	**Channel Address**
	0	0	0	DAC A
	0	0	1	DAC B
	0	1	0	DAC C
	0	1	1	DAC D
	1	0	0	All Four DACs
DB15 to DB0	Data bits.			

DATA REGISTER

The data register is addressed by setting the three REG bits to 000. The DAC address bits select the DAC channel where the data transfer is to take place (see Table 19). The data bits are in positions DB15 to DB0 for the AD5754R (see Table 20), DB15 to DB2 for the AD5734R (see Table 21), and DB15 to DB4 for the AD5724R (see Table 22).

Table 20. Programming the AD5754R Data Register

MSB						LSB
REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB0**
0	0	0	DAC Address			16-Bit DAC Data

Table 21. Programming the AD5734R Data Register

MSB								LSB
REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB2**	**DB1**	**DB0**
0	0	0	DAC Address			14-Bit DAC Data	X	X

Table 22. Programming the AD5724R Data Register

MSB										LSB
REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	0	0	DAC Address			12-Bit DAC Data	X	X	X	X

OUTPUT RANGE SELECT REGISTER

The output range select register is addressed by setting the three REG bits to 001. The DAC address bits select the DAC channel, while, the range bits (R2, R1, R0) select the required output range (see Table 23 and Table 24).

Table 23. Programming the Required Output Range

MSB									LSB
REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB3**	**DB2**	**DB1**	**DB0**
0	0	1	DAC Address			Don't Care	R2	R1	R0

Table 24. Output Range Options

R2	R1	R0	Output Range (V)
0	0	0	+5
0	0	1	+10
0	1	0	+10.8
0	1	1	±5
1	0	0	±10
1	0	1	±10.8

CONTROL REGISTER

The control register is addressed by setting the three REG bits to 011. The value written to the address and data bits determines the control function selected. The control register options are shown in Table 25 and Table 26.

Table 25. Control Register Format

MSB										LSB
REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	1	0	0	0	NOP, Data = Don't Care				

REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	1	0	0	1	Don't Care	TSD ENABLE	CLAMP ENABLE	CLR SELECT	SDO DISABLE

REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	1	1	0	0	CLEAR, Data = Don't Care				

REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	1	1	0	1	LOAD, Data = Don't Care				

Table 26. Control Register Functions

Option	Description
NOP	No operation instruction used in readback operations.
CLEAR	Addressing this function sets the DAC registers to the clear code and updates the outputs.
LOAD	Addressing this function updates the DAC registers and consequently, the DAC outputs.
SDO DISABLE	Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default).
CLR SELECT	See Table 27 for a description of the CLR SELECT operation.
CLAMP ENABLE	Set by the user to enable the current limit clamp (default). The channel does not power down on detection of overcurrent; the current is clamped at 20 mA. Cleared by the user to disable the current-limit clamp. The channel powers down on detection of overcurrent.
TSD ENABLE	Set by the user to enable the thermal shutdown feature. Cleared by the user to disable the thermal shutdown feature (default).

Table 27. CLR Select Options

CLR SELECT	Output CLR Value	
Setting	**Unipolar Output Range**	**Bipolar Output Range**
0	0 V	0 V
1	Mid-Scale	Negative Full-Scale

POWER CONTROL REGISTER

The power control register is addressed by setting the three REG bits to 010. This register allows the user to control and determine the power and thermal status of the AD5724R/AD5734R/AD5754R. The power control register options are shown in Table 28 and Table 29.

Table 28. Power Control Register Format

MSB																	LSB
REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**DB15 to DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	0	0	0	0	Don't Care	OC_D	OC_C	OC_B	OC_A	0	TSD	PU_{REF}	PU_D	PU_C	PU_B	PU_A

Table 29. Power Control Register Functions

Option	Description
PU_A	DAC A Power-Up. When set, this bit places DAC A in normal operating mode. When cleared, this bit places DAC A in power-down mode (default). If the CLAMP ENABLE bit of the control register is cleared, DACA will power down automatically on detection of an over-current, PU_A will be cleared to reflect this.
PU_B	DAC B Power-Up. When set, this bit places DAC B in normal operating mode. When cleared, this bit places DAC B in power-down mode (default). If the CLAMP ENABLE bit of the control register is cleared, DACB will power down automatically on detection of an over-current, PU_B will be cleared to reflect this.
PU_C	DAC C Power-Up. When set, this bit places DAC C in normal operating mode. When cleared, this bit places DAC C in power-down mode (default). If the CLAMP ENABLE bit of the control register is cleared, DACC will power down automatically on detection of an over-current, PU_C will be cleared to reflect this.
PU_D	DAC D Power-Up. When set, this bit places DAC D in normal operating mode. When cleared, this bit places DAC D in power-down mode (default). If the CLAMP ENABLE bit of the control register is cleared, DACD will power down automatically on detection of an over-current, PU_D will be cleared to reflect this.
PU_{REF}	Reference Power-Up. When set, this bit places the internal reference in normal operating mode. When cleared, this bit places the internal reference in power-down mode (default).
TSD	Thermal Shutdown Alert. Read-Only Bit. In the event of an over-temperature situation, this bit is set.
OC_A	DAC A Overcurrent Alert. Read-Only Bit. In the event of an overcurrent situation on DAC A, this bit is set.
OC_B	DAC B Overcurrent Alert. Read-Only Bit. In the event of an overcurrent situation on DAC B, this bit is set.
OC_C	DAC C Overcurrent Alert. Read-Only Bit. In the event of an overcurrent situation on DAC C, this bit is set.
OC_D	DAC D Overcurrent Alert. Read-Only Bit. In the event of an overcurrent situation on DAC D, this bit is set.

FEATURES

ANALOG OUTPUT CONTROL

In many industrial process control applications, it is vital that the output voltage be controlled during power-up. When the supply voltages change during power-up, the V_{OUT} pins are clamped to 0 V via a low impedance path (approxiamately 4kΩ). To prevent the output amplifiers from being shorted to 0 V during this time, Transmission Gate G1 is also opened (see Figure 46). These conditions are maintained until the power supplies have stabilized and a valid word is written to a DAC register. At this time, G2 opens and G1 closes.

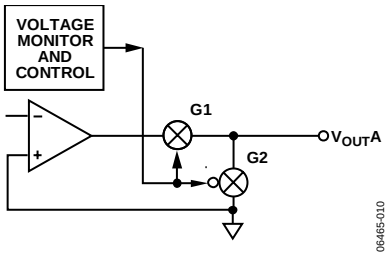


Figure 46. Analog Output Control Circuitry

POWER-DOWN MODE

Each DAC channel of the AD5724R/AD5734R/AD5754R can be individually powered-down. By default all channels are in power-down mode. The power status is controlled by the POWER CONTROL register, see Table 28 and Table 29 for details. When a channel is in power-down mode its output pin is clamped to ground through a resistance of approx. 4kΩ and the output of the amplifier is disconnected from the output pin.

OVERCURRENT PROTECTION

Each DAC channel of the AD5724R/AD5734R/AD5754R incorporates individual overcurrent protection. The user has two options for the configuration of the overcurrent protection, constant current clamp, or automatic channel power-down. The configuration of the overcurrent protection is selected via the CLAMP ENABLE bit in the control register.

Constant Current Clamp (CLAMP ENABLE = 1)

If a short circuit occurs, in this configuration the current is clamped at 20 mA. This event is signaled to the user by the setting of the appropriate overcurrent (OC_X) bit in the power control register. Upon removal of the short-circuit fault, the OC_X bit is cleared.

Automatic Channel Power-Down (CLAMP ENABLE = 0)

If a short circuit occurs, in this configuration the shorted channel powers down and its output is clamped to ground via a resistance of approx. 4kΩ, also at this time the output of the amplifier is disconnected from the output pin. The short-circuit event is signaled to the user via the overcurrent (OC_X) bits, while the power-up (PU_X) bits indicate which channels have powered down. After the fault is rectified, the channels can be powered up again by setting the PU_X bits.

THERMAL SHUTDOWN

The AD5724R/AD5734R/AD5754R incorporate a thermal shutdown feature that automatically shuts down the device if the core temperature exceeds approximately 150°C. The thermal shutdown feature is disabled by default and can be enabled via the TSD ENABLE bit of the control register. In the event of a thermal shutdown, the TSD bit of the power control register is set.

INTERNAL REFERENCE

The on-chip voltage reference is powered down by default. If an external voltage reference source is to be used, the internal reference must remain powered down at all times. If the internal reference is to be used as the reference source, it must be powered up via the PU_{REF} bit of the power control register. The internal reference voltage is accessible at the REFIN/REFOUT pin for use as a reference source for other devices within the system. If the internal reference is to be used external to the AD5724R/AD5734R/AD5754R, it must first be buffered.

APPLICATIONS INFORMATION

+5V / ±5V OPERATION

When operating from a single +5V supply or a dual ±5V supply an output range of +5V or ±5V is not achievable as sufficient headroom for the output amplifier is not available. In this situation a reduced reference voltage can be used, for instance a 2V reference will produce an output range of +4V or ±4V, the 1V of headroom is more than enough for full operation. A standard value voltage reference of 2.048V can be used to produce output ranges of +4.096V and ±4.096V. Refer to the Typical Performance Characteristics plots for performance data at a range of voltage reference values.

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5724R/AD5734R/AD5754R are mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5724R/AD5734R/AD5754R are in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5724R/AD5734R/AD5754R should have an ample supply bypassing of a 10 µF capacitor in parallel with 0.1 µF capacitor on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5724R/AD5734R/AD5754R should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (this is not required on a multilayer board that has a separate ground plane, but separating the lines does help). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler® family of products from Analog Devices provides voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5724R/AD5734R/AD5754R make them ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 47 shows a 4-channel isolated interface to the AD5724R/AD5734R/AD5754R using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

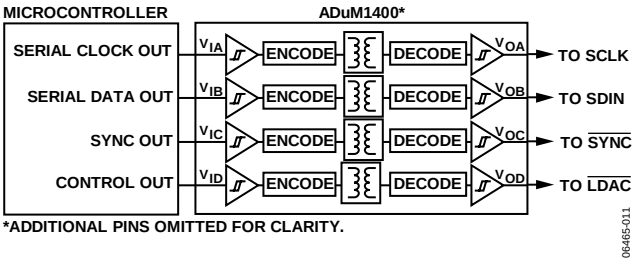


Figure 47. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5724R/AD5734R/AD5754R is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5724R/AD5734R/AD5754R require a 24-bit data-word with data valid on the falling edge of SCLK.

For all interfaces, the DAC output update can be initiated automatically when all the data is clocked in, or it can be performed under the control of $\overline{\text{LDAC}}$. The contents of the registers can be read using the readback function.

AD5724R/AD5734R/AD5754R to Blackfin® DSP interface

Figure 48 shows how the AD5724R/AD5734R/AD5754R can be interfaced to Analog Devices Blackfin DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5724R/AD5734R/AD5754R and the programmable I/O pins that can be used to set the state of a digital input such as the $\overline{\text{LDAC}}$ pin.

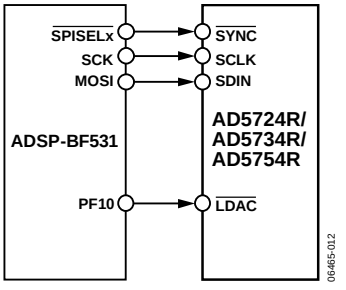
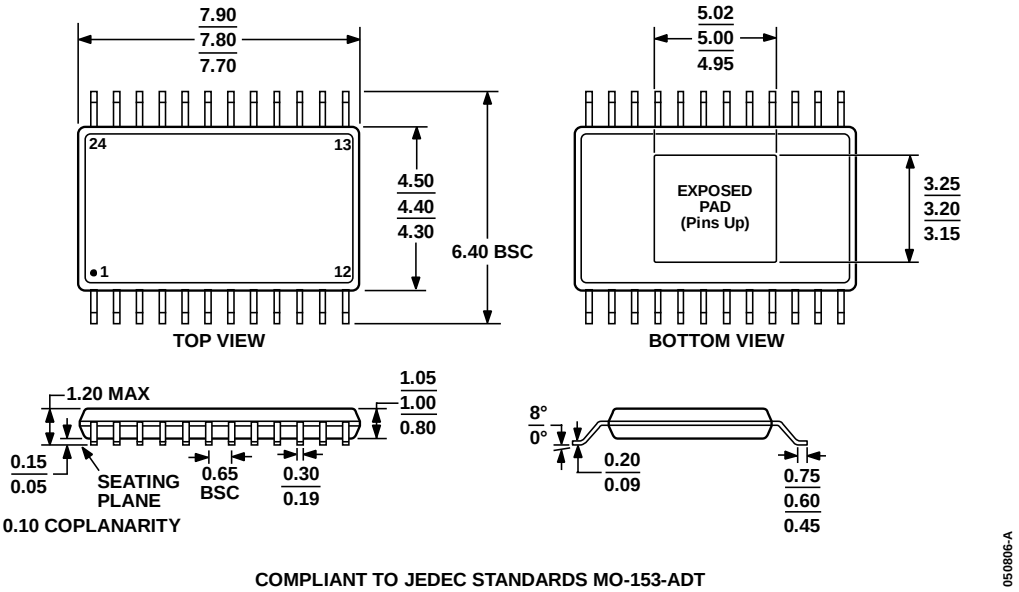


Figure 48. AD5724R/AD5734R/AD5754R to Blackfin Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-ADT

Figure 49. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP_EP]
(RE-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	Temperature Range	INL	Package Description	Package Option
AD5724RBREZ[1]	12	–40°C to 85°C	±1 LSB	24-Lead TSSOP_EP	RE-24
AD5724RBREZ-REEL7[1]	12	–40°C to 85°C	±1 LSB	24-Lead TSSOP_EP	RE-24
AD5734RBREZ[1]	14	–40°C to 85°C	±4 LSB	24-Lead TSSOP_EP	RE-24
AD5734RBREZ-REEL7[1]	14	–40°C to 85°C	±4 LSB	24-Lead TSSOP_EP	RE-24
AD5754RBREZ[1]	16	–40°C to 85°C	±16 LSB	24-Lead TSSOP_EP	RE-24
AD5754RBREZ-REEL7[1]	16	–40°C to 85°C	±16 LSB	24-Lead TSSOP_EP	RE-24

[1] Z = Pb-free part.

PR06465-0-11/07(PrC)