NEC

MOS INTEGRATED CIRCUIT

μPD780053, 780054, 780055, 780056, 780058, 780058B, 780053Y, 780054Y, 780055Y, 780056Y, 780058BY

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

★ The μPD780053, 780054, 780055, 780056, 780058, and 780058B (hereafter, referred to as μPD78005x) are products of the μPD780058 Subseries in the 78K/0 Series.

★ The μPD780053Y, 780054Y, 780055Y, 780056Y, and 780058BY (hereafter referred to as μPD78005xY) are products of the μPD780058Y Subseries in the 78K/0 Series.

These microcontrollers show a reduction in the EMI (Electro Magnetic Interference) noise generated internally compared to the conventional type, the μPD78054 Subseries. Also they have provided is an 8-bit resolution A/D converter, 8-bit resolution D/A converter, timers, serial interfaces, real-time output ports, interrupt functions, and various other peripheral hardware.

The μPD780058Y Subseries is based on the μPD780058 Subseries but with the addition of an I^2C bus interface function supporting multi-master.

Flash memory versions, the μPD78F0058 and 78F0058Y and various development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780058, 780058Y Subseries User's Manual: U12013E
78K/0 Series User's Manual - Instruction: U12326E

FEATURES

Item / Part Number	Program Memory (ROM)	Data Memory		
		Internal High-Speed RAM	Internal Buffer RAM	Internal Expansion RAM
μPD780053, 780053Y	24 KB	1,024 bytes	32 bytes	None
μPD780054, 780054Y	32 KB			
μPD780055, 780055Y	40 KB			
μPD780056, 780056Y	48 KB			
★ μPD780058B, 780058BY 780058	60 KB			1,024 bytes

- Internal high-capacity ROM & RAM
- External memory expansion space: 64 KB
- Minimum instruction execution time can be changed from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 68 (N-ch open-drain: 4)
- 8-bit resolution A/D converter: 8 channels (V_{DD} = 1.8 to 5.5 V[Note])
- 8-bit resolution D/A converter: 2 channels (V_{DD} = 1.8 to 5.5 V[Note])
- Serial interface: 3 channels
- Timer: 5 channels
- Supply voltage: V_{DD} = 1.8 to 5.5 V

Note The operation voltage of the A/D converter and D/A converter of the μPD780058 is V_{DD} = 2.7 to 5.5 V.

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The mark ★ shows major revised points.

APPLICATIONS

Car audio systems, cellular phones, pagers, printers, AV equipment, cameras, PPCs, vending machines, etc.

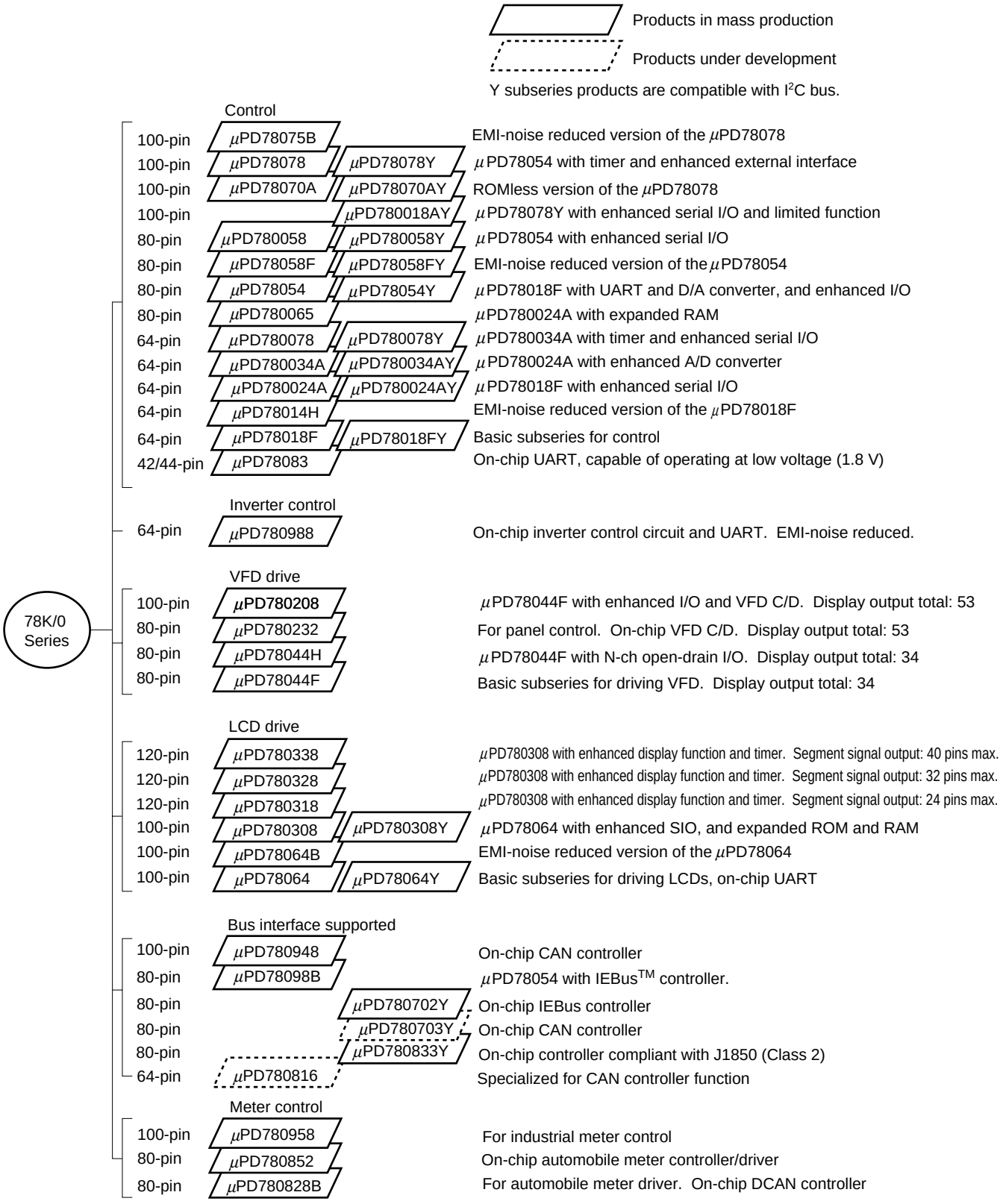
ORDERING INFORMATION

	Part Number	Package
	μPD780053GC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780053GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780054GC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780054GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780055GC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780055GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780056GC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780056GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780058GC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780058GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
★	μPD780058BGC-×××-8BT	80-pin plastic QFP (14 × 14)
★	μPD780058BGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780053YGC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780053YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780054YGC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780054YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780055YGC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780055YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
	μPD780056YGC-×××-8BT	80-pin plastic QFP (14 × 14)
	μPD780056YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
★	μPD780058BYGC-×××-8BT	80-pin plastic QFP (14 × 14)
★	μPD780058BYGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)

Remark ××× indicates ROM code suffix.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries name.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

- Non-Y subseries

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Yes
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	Yes
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	Yes
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash-board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K									59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

The major functional differences among the subseries are listed below.

• Y subseries

Subseries Name \ Function		ROM Capacity	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch, I^2C: 1 ch)	88	1.8 V	√
	μPD78070AY	–									61	2.7 V	
	μPD780018AY	48 K to 60 K							–	3 ch (I^2C: 1ch)	88		
	μPD780058Y	24 K to 60 K	2 ch						2 ch	3 ch (time-division UART: 1 ch, I^2C: 1 ch)	68	1.8 V	
	μPD78058FY	48 K to 60 K								3 ch (UART: 1 ch, I^2C: 1 ch)	69	2.7 V	
	μPD78054Y	16 K to 60 K										2.0 V	
	μPD780078Y	48 K to 60 K		2 ch			–	8 ch	–	4 ch (UART: 2 ch, I^2C: 1 ch)	52	1.8 V	
	μPD780034AY	8 K to 32 K		1 ch						3 ch (UART: 1 ch, I^2C: 1 ch)	51		
	μPD780024AY						8 ch	–					
	μPD78018FY	8 K to 60 K								2 ch (I^2C:1 ch)	53		
LCD drive	μPD780308Y	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time-division UART: 1 ch, I^2C: 1 ch)	57	2.0 V	–
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I^2C: 1 ch)			
Bus interface supported	μPD780701Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	–	–	4 ch (UART: 1 ch, I^2C: 1 ch)	67	3.5 V	–
	μPD780703Y												
	μPD780833Y										65	4.5 V	

Remark Functions other than the serial interface are common to both the Y and non-Y subseries.

OVERVIEW OF FUNCTIONS

★ ★ Item \ Product Name		μPD780053 μPD780053Y	μPD780054 μPD780054Y	μPD780055 μPD780055Y	μPD780056 μPD780056Y	μPD780058B μPD780058BY	μPD780058
Internal memory	ROM	24 KB	32 KB	40 KB	48 KB	60 KB	
	High-speed RAM	1,024 bytes					
	Buffer RAM	32 bytes					
	Expanded RAM	None				1,024 bytes	
Memory space		64 KB					
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Minimum instruction execution time		On-chip minimum instruction execution time variable function					
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0 MHz operation)					
	When subsystem clock is selected	122 μs (@32.768 kHz operation)					
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.					
I/O ports		Total: 68 • CMOS input : 2 • CMOS I/O : 62 • N-ch open-drain I/O: 4					
A/D converter		• 8-bit resolution × 8 channels					
★	Operating voltage range	V_{DD} = 1.8 to 5.5 V					V_{DD} = 2.7 to 5.5
D/A converter		• 8-bit resolution × 2 channels					
★	Operating voltage range	V_{DD} = 1.8 to 5.5 V					V_{DD} = 2.7 to 5.5
Serial interface		• 3-wire serial I/O/2-wire serial I/O/SBI[Note 1]/I²C bus[Note 2] mode selectable: 1 channel • 3-wire serial I/O mode (automatic data transmit/receive function for up to 32 bytes provided on-chip): 1 channel • 3-wire serial I/O/UART mode (time division transfer function provided on-chip) selectable: 1 channel					
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel					
Timer outputs		3 (14-bit PWM output × 1)					
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@5.0 MHz operation with main system clock) 32.768 kHz (@32.768 kHz operation with subsystem clock)					
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@5.0 MHz operation with main system clock)					
Vectored interrupt sources	Maskable	Internal: 13, External: 6					
	Non-maskable	Internal: 1					
	Software	1					
Test inputs		Internal: 1, external: 1					
Supply voltage		V_{DD} = 1.8 to 5.5 V					
Operating ambient temperature		T_A = –40 to +85°C					
Package		• 80-pin plastic QFP (14 × 14) • 80-pin plastic TQFP (fine pitch) (12 × 12)					

Notes 1. μPD78005x only

2. μPD78005xY only

CONTENTS

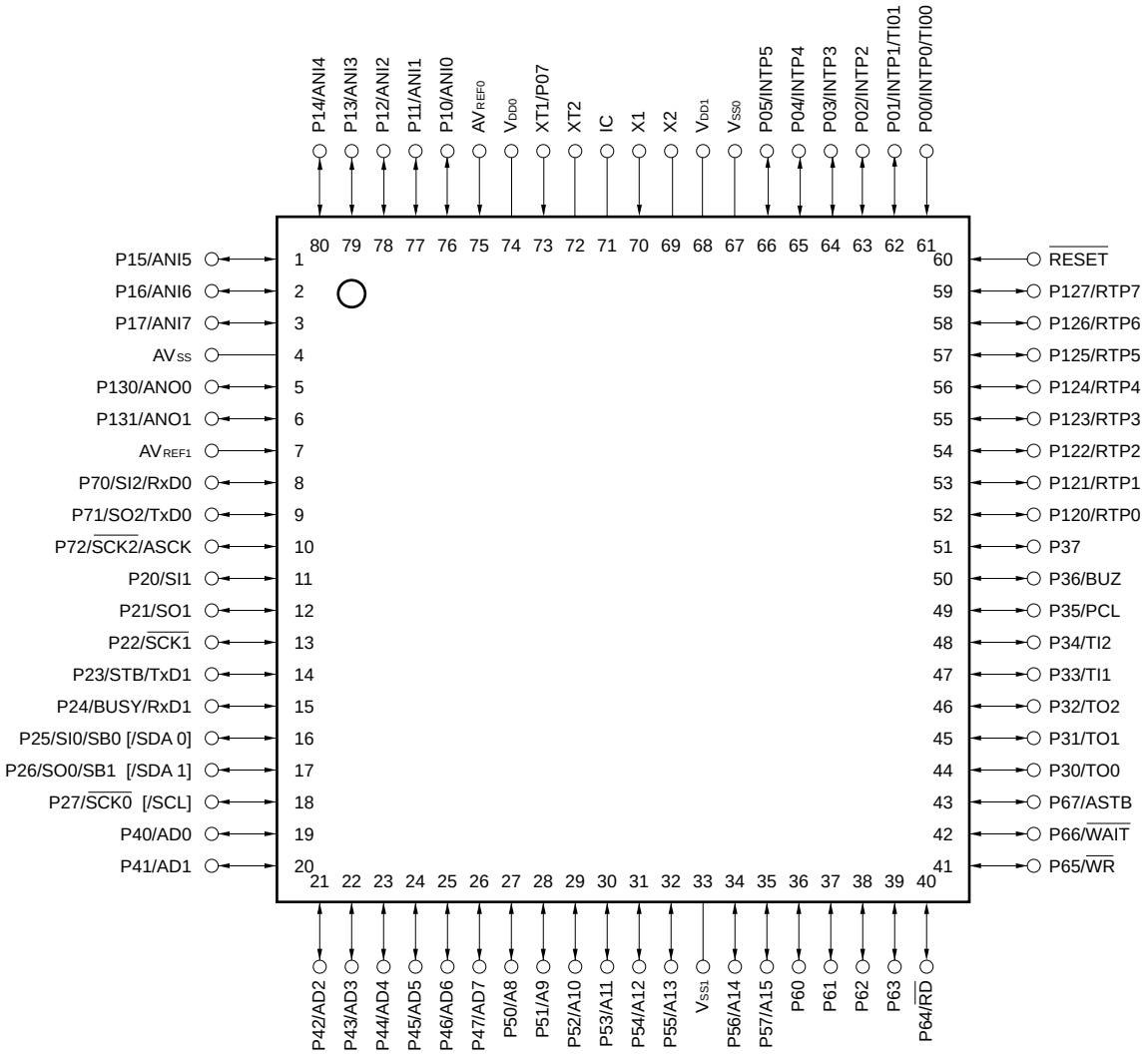
1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14)**

  μPD780053GC-×××-8BT, 780054GC-×××-8BT, 780055GC-×××-8BT, 780056GC-×××-8BT, 780058GC-×××-8BT,
★ 780058BGC-×××-8BT, 780053YGC-×××-8BT, 780054YGC-×××-8BT, 780055YGC-×××-8BT, 780056YGC-×××-8BT,
★ 780058BYGC-×××-8BT

- **80-pin plastic TQFP (fine pitch) (12 × 12)**

  μPD780053GK-×××-9EU, 780054GK-×××-9EU, 780055GK-×××-9EU, 780056GK-×××-9EU, 780058GK-×××-9EU,
★ 780058BGK-×××-9EU, 780053YGK-×××-9EU, 780054YGK-×××-9EU, 780055YGK-×××-9EU, 780056YGK-×××-9EU,
★ 780058BYGK-×××-9EU



Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

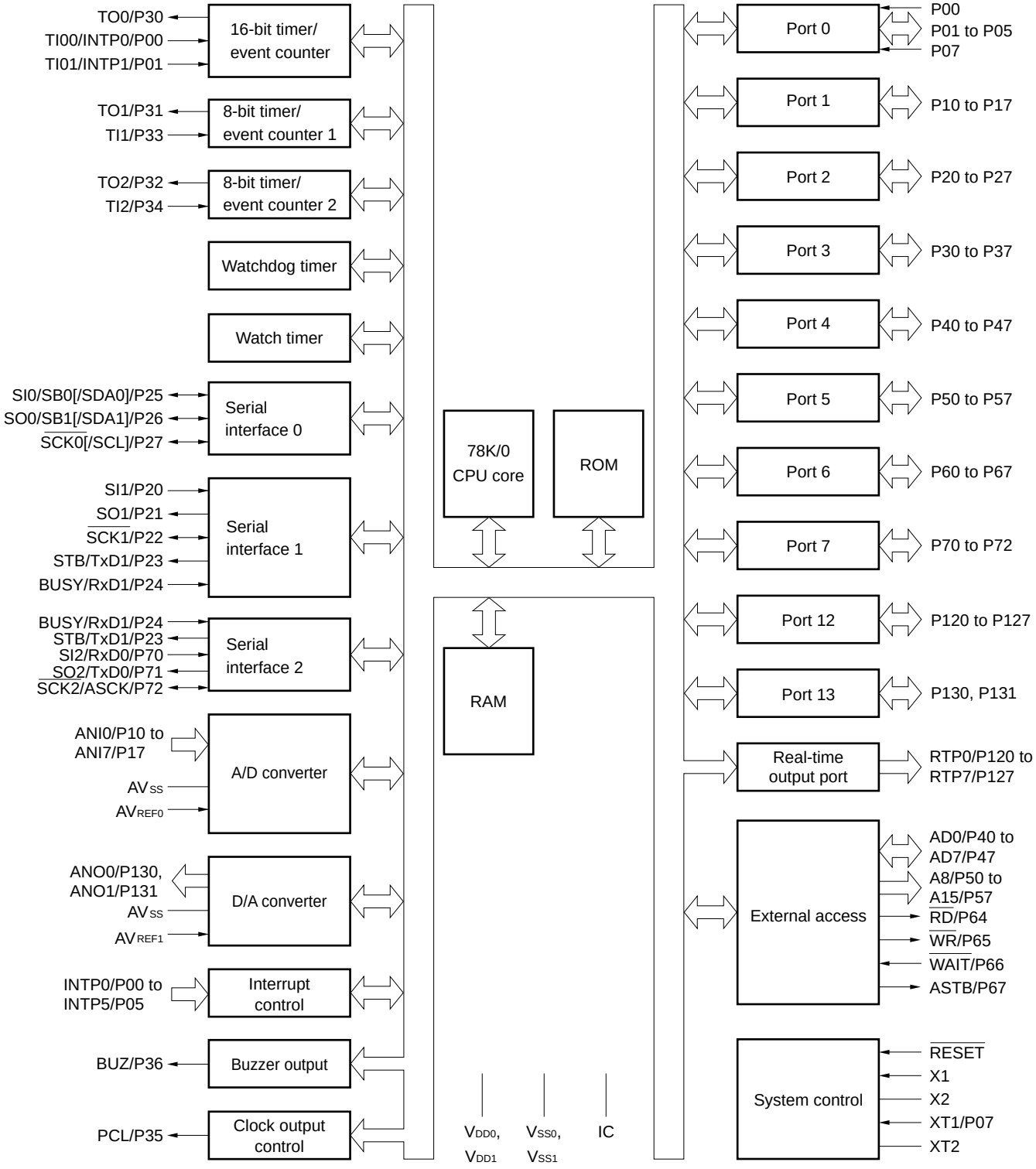
Remarks 1. [ ]: μPD78005xY only

2. When the microcontroller is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

PIN IDENTIFICATION

A8 to A15:	Address bus
AD0 to AD7:	Address/data bus
ANI0 to ANI7:	Analog input
ANO0, ANO1:	Analog output
ASCK:	Asynchronous serial clock
ASTB:	Address strobe
AV_{REF0}, AV_{REF1}:	Analog reference voltage
AV_{SS}:	Analog ground
BUSY:	Busy
BUZ:	Buzzer clock
IC:	Internally connected
INTP0 to INTP5:	Interrupt from peripherals
P00 to P05, P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P72:	Port 7
P120 to P127:	Port 12
P130, P131:	Port 13
PCL:	Programmable clock
$\overline{RD}$:	Read strobe
$\overline{RESET}$:	Reset
RTP0 to RTP7:	Real-time output port
RxD0, RxD1:	Receive data
SB0, SB1:	Serial bus
$\overline{SCK0}$ to $\overline{SCK2}$:	Serial clock
SCL:	Serial clock
SDA0, SDA1:	Serial data
SI0 to SI2:	Serial input
SO0 to SO2:	Serial output
STB:	Strobe
TI00, TI01:	Timer input
TI1, TI2:	Timer input
TO0 to TO2:	Timer output
TxD0, TxD1:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{SS0}, V_{SS1}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR}$:	Write strobe
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (subsystem clock)

2. BLOCK DIAGRAM



Remarks 1. The internal ROM and RAM capacity varies depending on the product.

2. [ ]: μPD78005xY only

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 7-bit I/O port	Input only	Input	INTP0/TI00
P01	I/O		Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07Note 1	Input		Input only	Input	XT1
P10 to P17	I/O	Port 1 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by softwareNote 2.		Input	ANI0 to ANI7
P20	I/O	Port 2 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB/TxD1
P24					BUSY/RxD1
P25					SI0/SB0[/SDA0]
P26					SO0/SB1[/SDA1]
P27					$\overline{\text{SCK0}}$ [/SCL]
P30	I/O	Port 3 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software. The test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pins as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1. Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, set port 1 to the input mode. At this time, on-chip pull-up resistors are automatically disconnected.

Remark [ ] μPD78005xY only

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	I/O	Port 5 8-bit I/O port. LEDs can be driven directly. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.		Input	A8 to A15
P60	I/O	Port 6 8-bit I/O port. Input/output can be specified in 1-bit units.	N-ch open-drain input/ output port. An on-chip pull-up resistor can be specified by the mask option. LEDs can be driven directly.	Input	–
P61					
P62					
P63					
P64			When used as an input port, an on-chip pull-up resistor can be specified by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	I/O	Port 7 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.		Input	SI2/RxD0
P71					SO2/TxD0
P72					$\overline{SCK2}$/ASCK
P120 to P127	I/O	Port 12 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistor can be specified by software.		Input	RTP0 to RTP7
P130, P131	I/O	Port 13 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.		Input	ANO0, ANO1

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input	Input	P25/SB0 [/SDA0]
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output	Input	P26/SB1 [/SDA1]
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0 [/SDA0]
SB1				P26/SO0 [/SDA1]
SDA0		μPD78005xY only		P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	I/O	Serial interface serial clock input/output	Input	P27 [/SCL]
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL		μPD78005xY only		P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23/TxD1
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24/RxD1
RxD0	Input	Asynchronous serial interface serial data input	Input	P70/SI2
RxD1				P24/BUSY
TxD0	Output	Asynchronous serial interface serial data output	Input	P71/SO2
TxD1				P23/STB
ASCK	Input	Asynchronous serial interface serial clock input	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port from which data is output in synchronization with a trigger	Input	P120 to P127
AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47

Remark [ ]: μPD78005xY only

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input (also used for analog power supply)	–	–
AV_{REF1}	Input	D/A converter reference voltage input	–	–
AV_{SS}	–	A/D converter and D/A converter ground potential Use at the same potential as V_{SS0}.	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	Input	P07
XT2	–		–	–
V_{DD0}	–	Port block positive power supply	–	–
V_{SS0}	–	Port block ground potential	–	–
V_{DD1}	–	Positive power supply (except for port and analog blocks)	–	–
V_{SS1}	–	Ground potential (except for port and analog blocks)	–	–
IC	–	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the I/O circuit configuration of each type, see Figure 3-1.

Table 3-1. Pin I/O Circuit Type (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection
P00/INTP0/TI00	2	Input	Connect to V_{SS0}.
P01/INTP1/TI01	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{DD0}.
P10/ANI0 to P17/ANI7	11-D	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P20/SI1	8-C		
P21/SO1	5-H		
P22/$\overline{SCK1}$	8-C		
P23/STB/TxD1	5-H		
P24/BUSY/RxD1	8-C		
P25/SI0/SB0 [/SDA0]	10-B		
P26/SO0/SB1 [/SDA1]			
P27/$\overline{SCK0}$ [/SCL]			
P30/TO0	5-H		
P31/TO1			
P32/TO2			
P33/TI1	8-C		
P34/TI2			
P35/PCL	5-H		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-N		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P50/A8 to P57/A15	5-H		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P60 to P63	13-J		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P64/$\overline{RD}$	5-H		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Remark [ ]: μPD78005xY only.

Table 3-1. Pin I/O Circuit Type (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection
P70/SI2/RxD0	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P71/SO2/TxD0	5-H		
P72/$\overline{SCK2}$/ASCK	8-C		
P120/RTP0 to P127/RTP7	5-H		
P130/ANO0, P131/ANO1	12-C		Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
$\overline{RESET}$	2	Input	–
XT2	16	–	Leave open.
AV_{REF0}	–		Connect to V_{SS0}.
AV_{REF1}			Connect to V_{DD0}.
AV_{SS}			Connect to V_{SS0}.
IC			Directly connect to V_{SS0} or V_{SS1}.

Figure 3-1. Pin I/O Circuits (1/2)

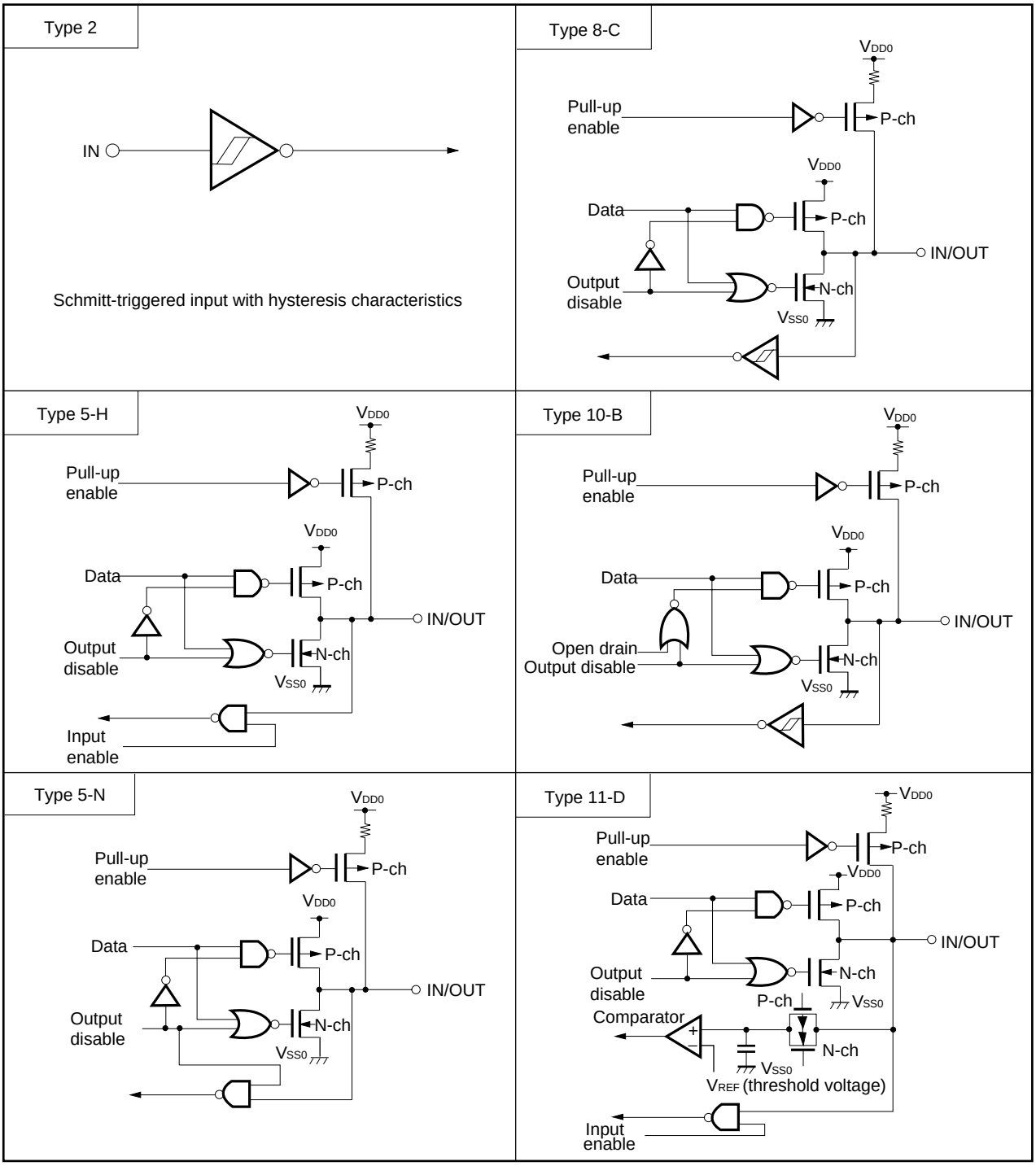
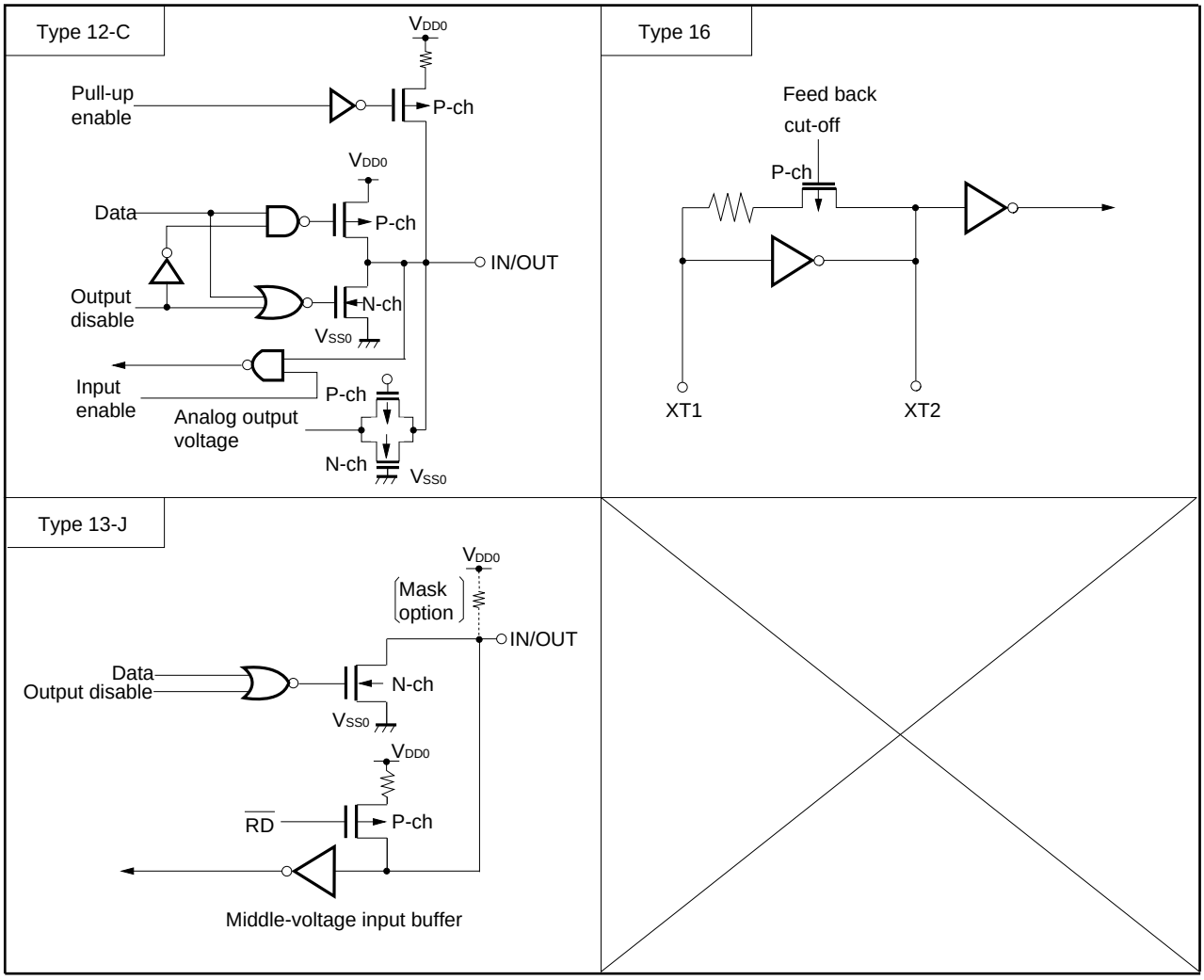


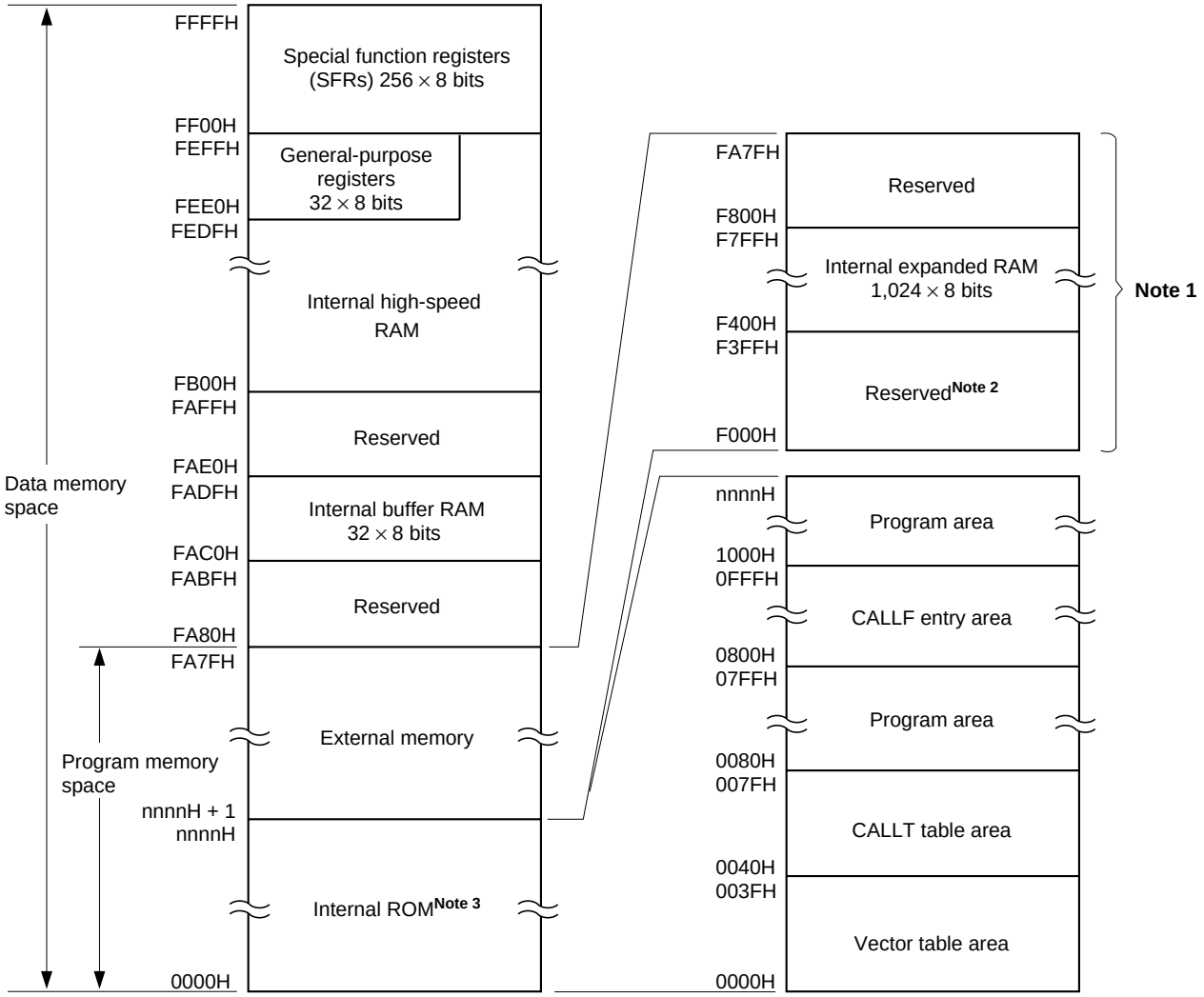
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD78005x and 78005xY.

Figure 4-1. Memory Map



★ **Notes 1.** μPD780058, 780058B, 780058BY only

★ **2.** If external device expansion functions are to be employed for the μPD780058, 780058B, or 780058BY, set the size of the internal ROM to 56 KB or less using internal the memory size switching register (IMS).

3. The internal ROM capacity depends on the product (see the table below).

Part Number	Last Address of Internal ROM nnnnH
μPD780053, 780053Y	5FFFH
μPD780054, 780054Y	7FFFH
μPD780055, 780055Y	9FFFH
μPD780056, 780056Y	BFFFH
★ μPD780058B, 780058BY, 780058	EFFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following three types of I/O ports are available.

- CMOS input (P00, P07): 2
- CMOS I/O (P01 to P05, port 1 to port 5, P64 to P67, port 7, port 12, port 13): 62
- N-ch open-drain I/O (P60 to P63): 4

Total: 68

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00, P07	Input only
	P01 to P05	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 1	P10 to P17	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 3	P30 to P37	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 4	P40 to P47	I/O port. Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software. The test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software. LEDs can be driven directly.
Port 6	P60 to P63	N-ch open-drain I/O port. Input/output can be specified in 1-bit units. On-chip pull-up resistor can be used by mask option. LEDs can be driven directly.
	P64 to P67	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 7	P70 to P72	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 12	P120 to P127	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 13	P130, P131	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.

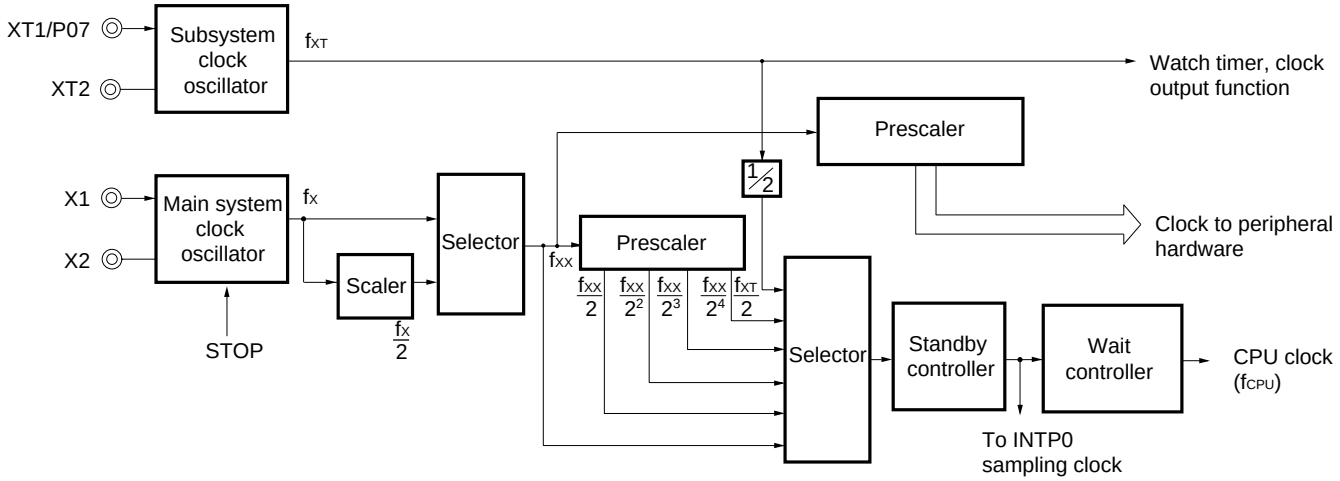
5.2 Clock Generator

Two types of generators, a main system clock generator and a subsystem clock generator, are available.

The minimum instruction execution time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0 MHz operation with main system clock)
- 122 μs (@32.768 kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

Five timer/event counter channels are incorporated.

- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Operations of Timer/Event Counter

		16-Bit Timer/ Event Counter	8-Bit Timer/ Event Counter	Watch Timer	Watchdog Timer
Operation mode	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	–	–
Function	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width measurement	1 input	–	–	–
	Square wave output	1 output	2 outputs	–	–
	One-shot pulse output	1 output	–	–	–
	Interrupt request	2	2	2	1

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter

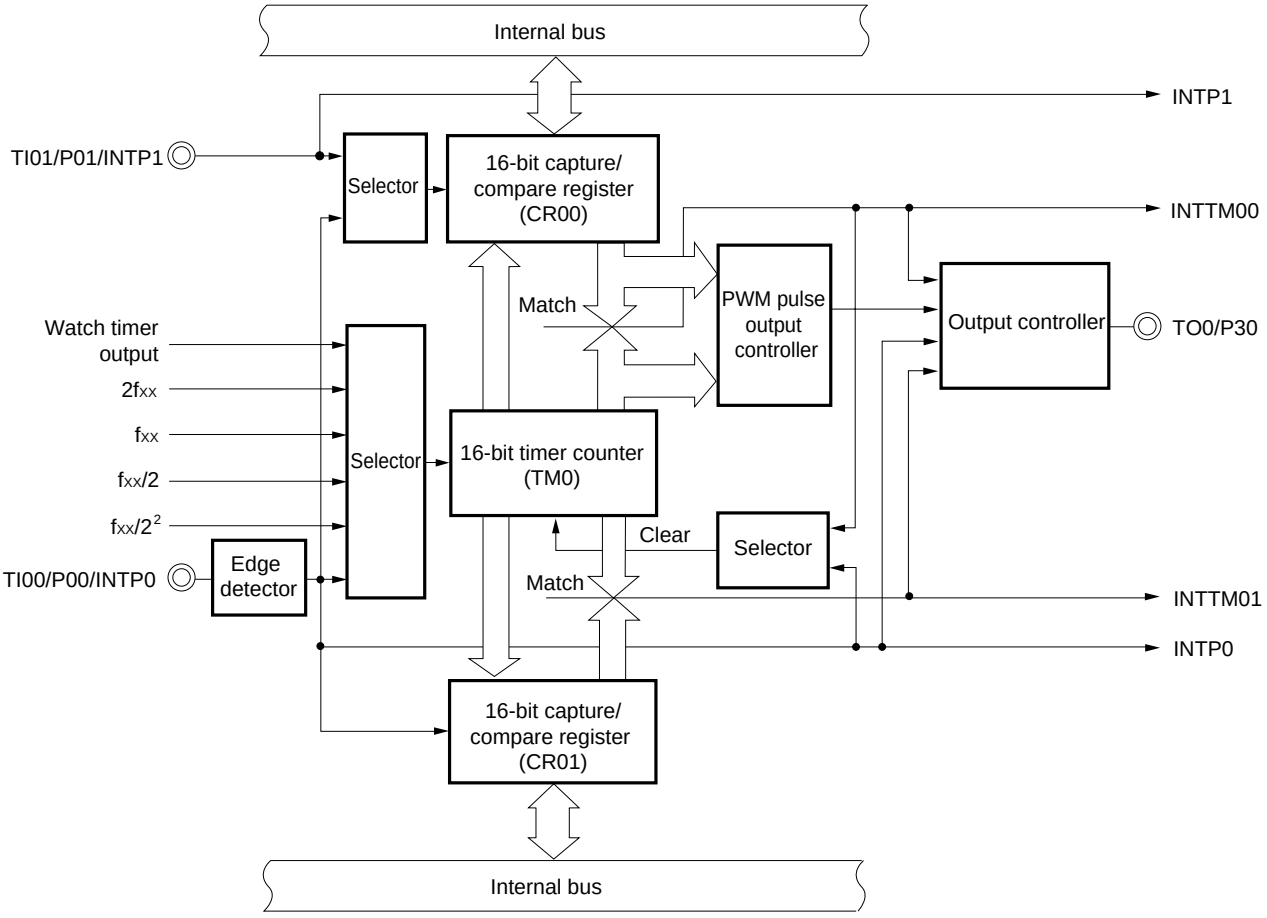


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter

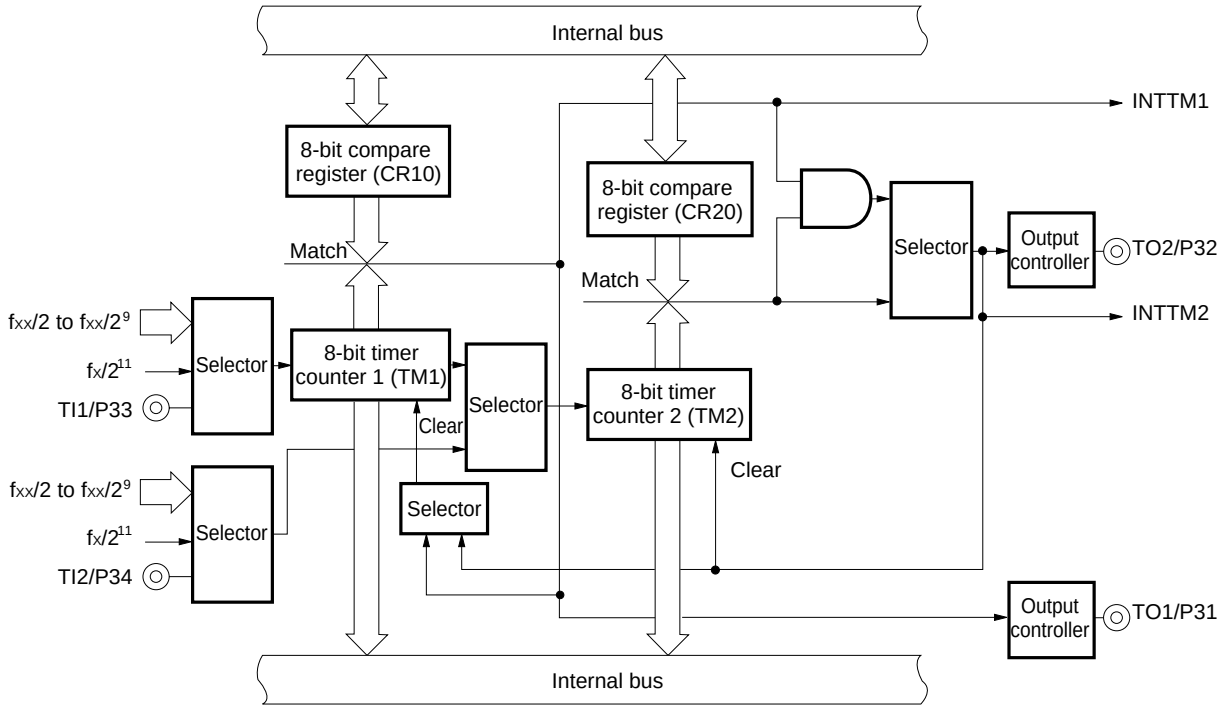


Figure 5-4. Block Diagram of Watch Timer

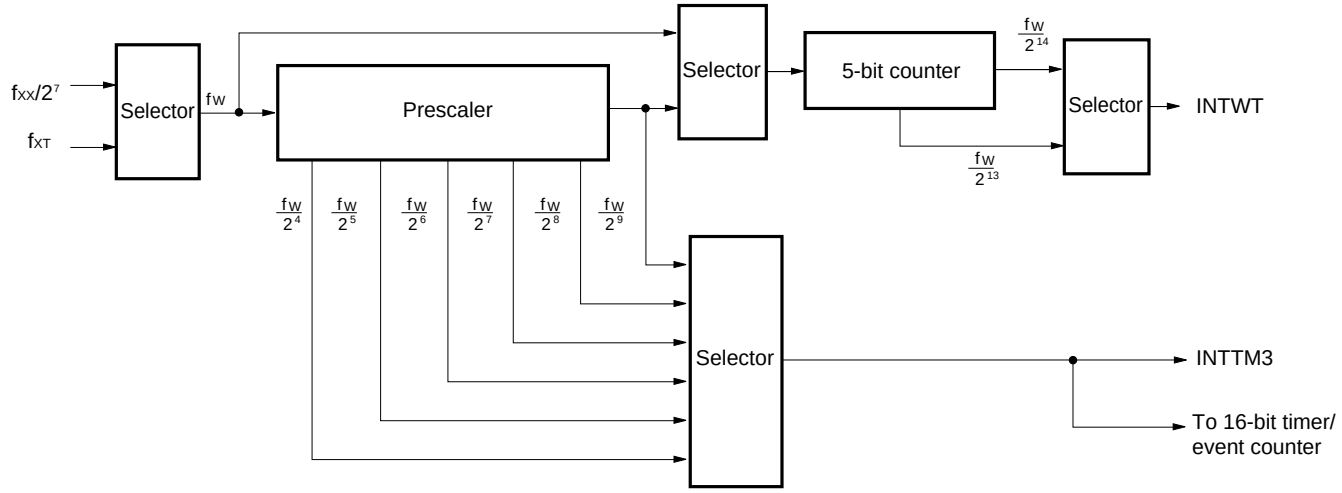
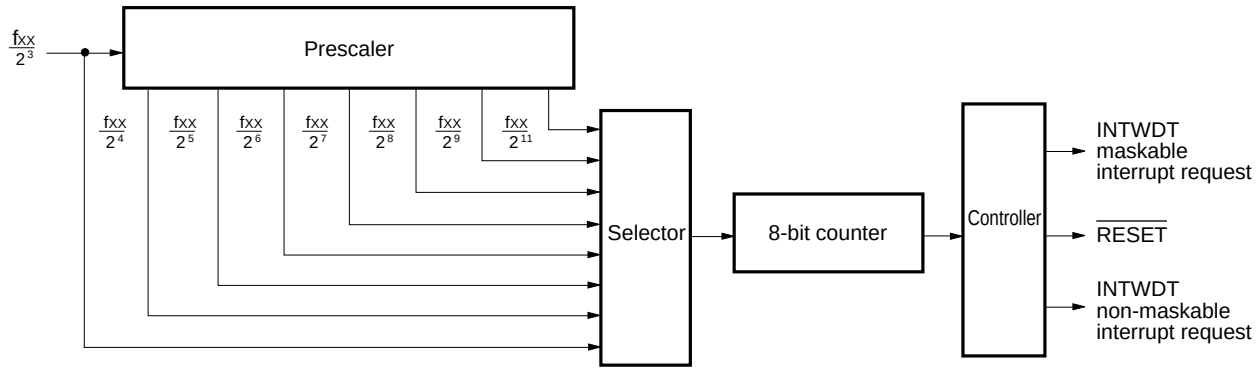


Figure 5-5. Block Diagram of Watchdog Timer

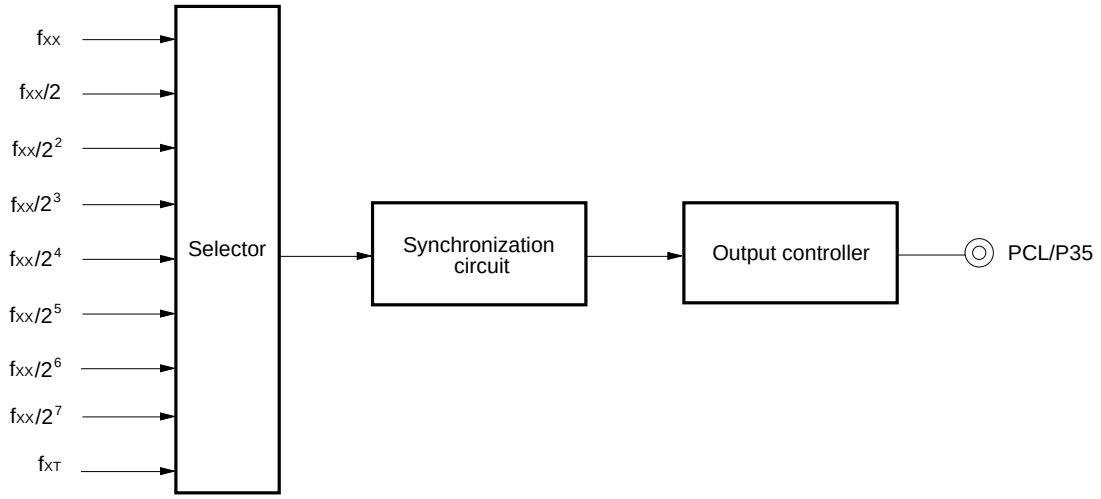


5.4 Clock Output Controller

Clocks with the following frequencies can be output as the clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (@5.0 MHz operation with main system clock)
- 32.768 kHz (@32.768 kHz operation with subsystem clock)

Figure 5-6. Block Diagram of Clock Output Controller

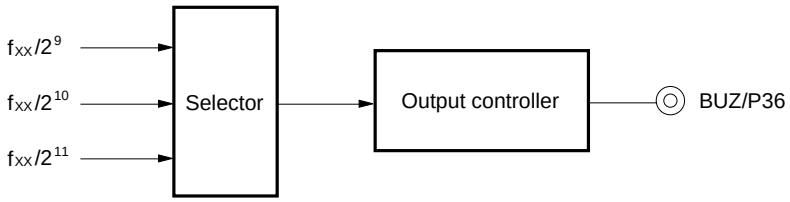


5.5 Buzzer Output Controller

Clocks with the following frequencies can be output as the buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (@5.0 MHz operation with main system clock)

Figure 5-7. Block Diagram of Buzzer Output Controller



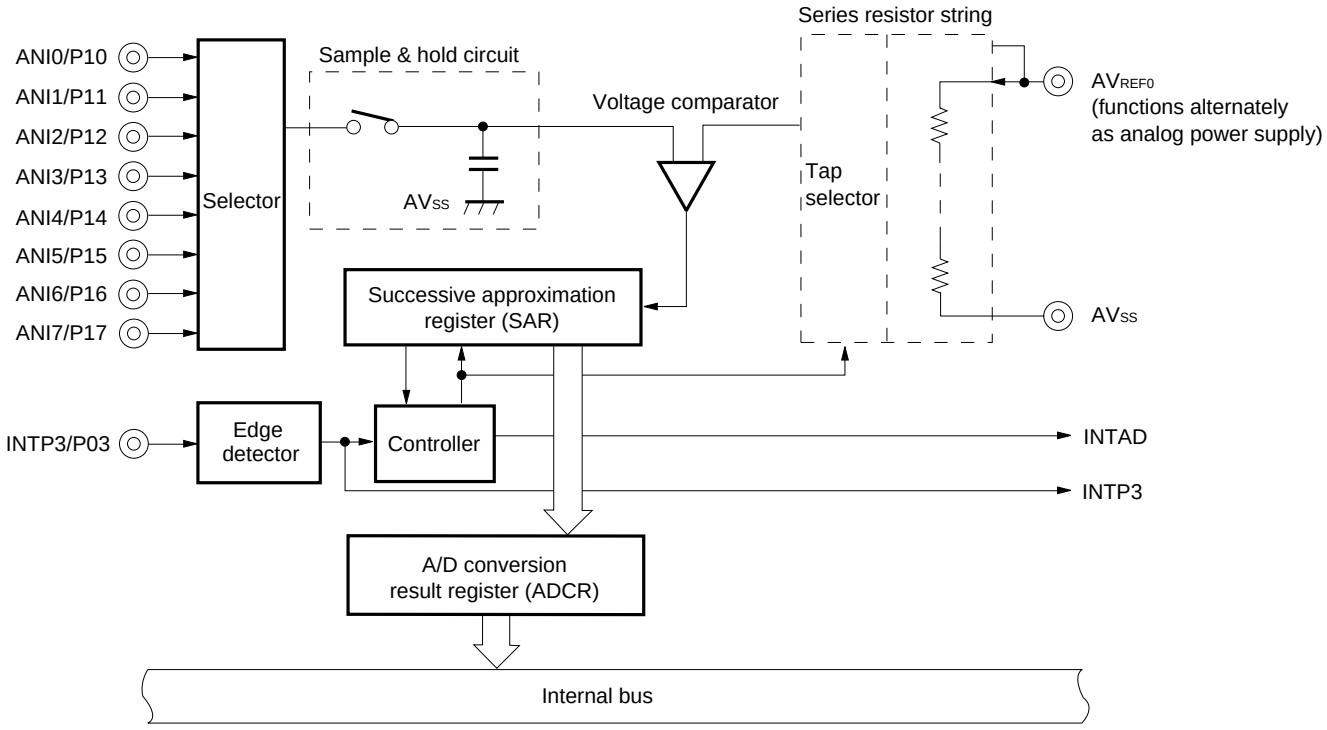
5.6 A/D Converter

An A/D converter consists of eight 8-bit resolution channels is incorporated.

The following two types of the A/D conversion operation startup methods are available.

- Hardware start
- Software start

Figure 5-8. Block Diagram of A/D Converter

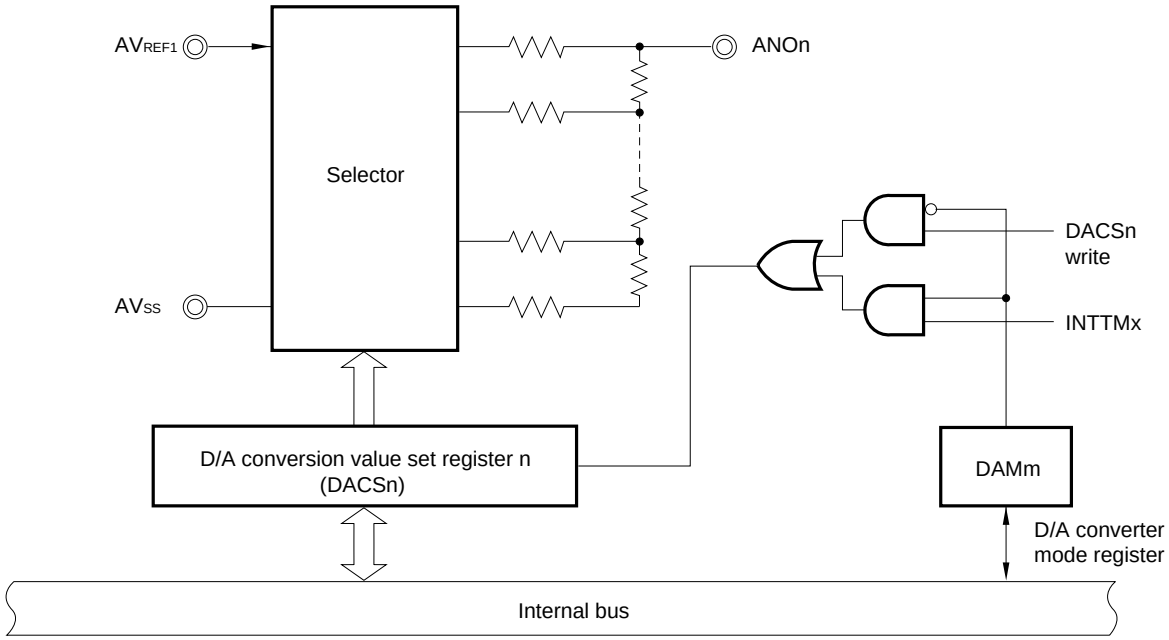


5.7 D/A Converter

A D/A converter consisting of two 8-bit resolution channels is incorporated.

The conversion method is the R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1

m = 4, 5

x = 1, 2

5.8 Serial Interfaces

Three clocked serial interface channels are incorporated.

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interface

Function	Serial Interface Channel 0		Serial Interface Channel 1	Serial Interface Channel 2
	μPD78005x	μPD78005xY		
3-wire serial I/O mode	√ (MSB/LSB first switching possible)		√ (MSB/LSB first switching possible)	√ (MSB/LSB first switching possible)
3-wire serial I/O mode with automatic transmit/receive function	–		√ (MSB/LSB first switching possible)	–
SBI (serial bus interface) mode	√ (MSB first)	–	–	–
I^2C bus mode	–	√ (MSB first)	–	–
2-wire serial I/O mode	√ (MSB first)		–	–
Asynchronous serial interface (UART) mode (on-chip time division transfer function)	–		–	√ (On-chip dedicated baud rate generator)

Figure 5-10. Block Diagram of Serial Interface Channel 0 (1/2)

(a) μPD78005x

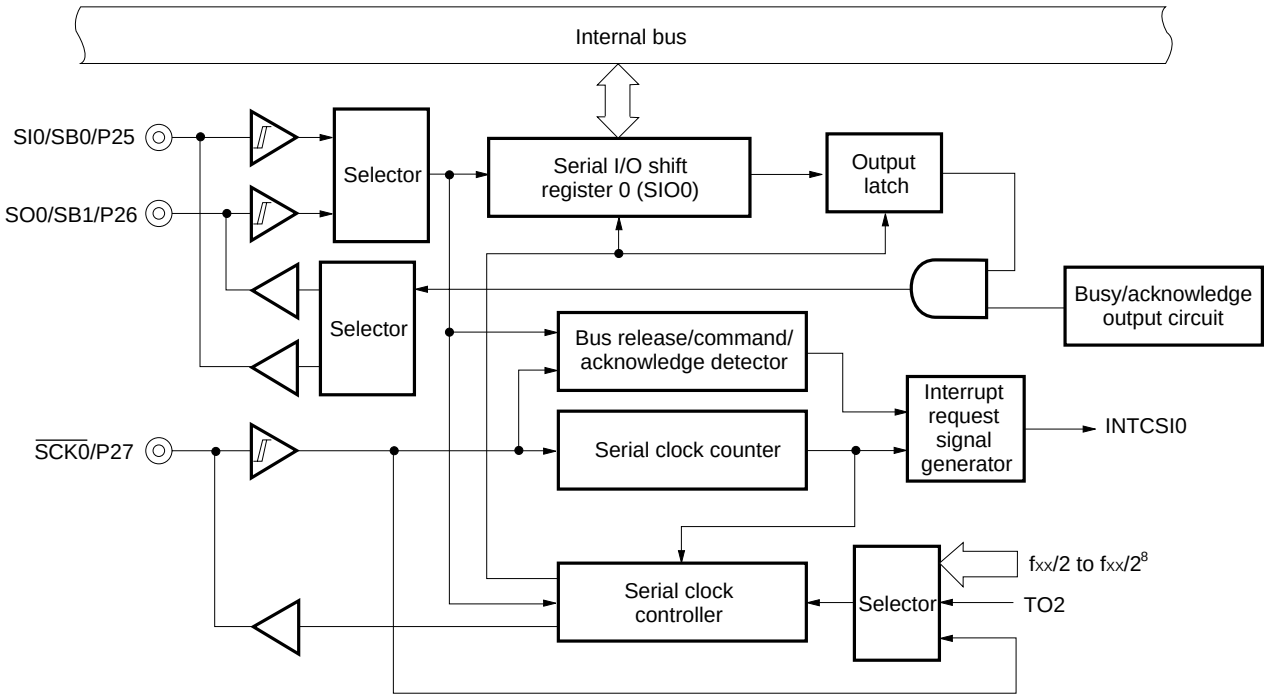


Figure 5-10. Block Diagram of Serial Interface Channel 0 (2/2)

(b) μPD78005xY

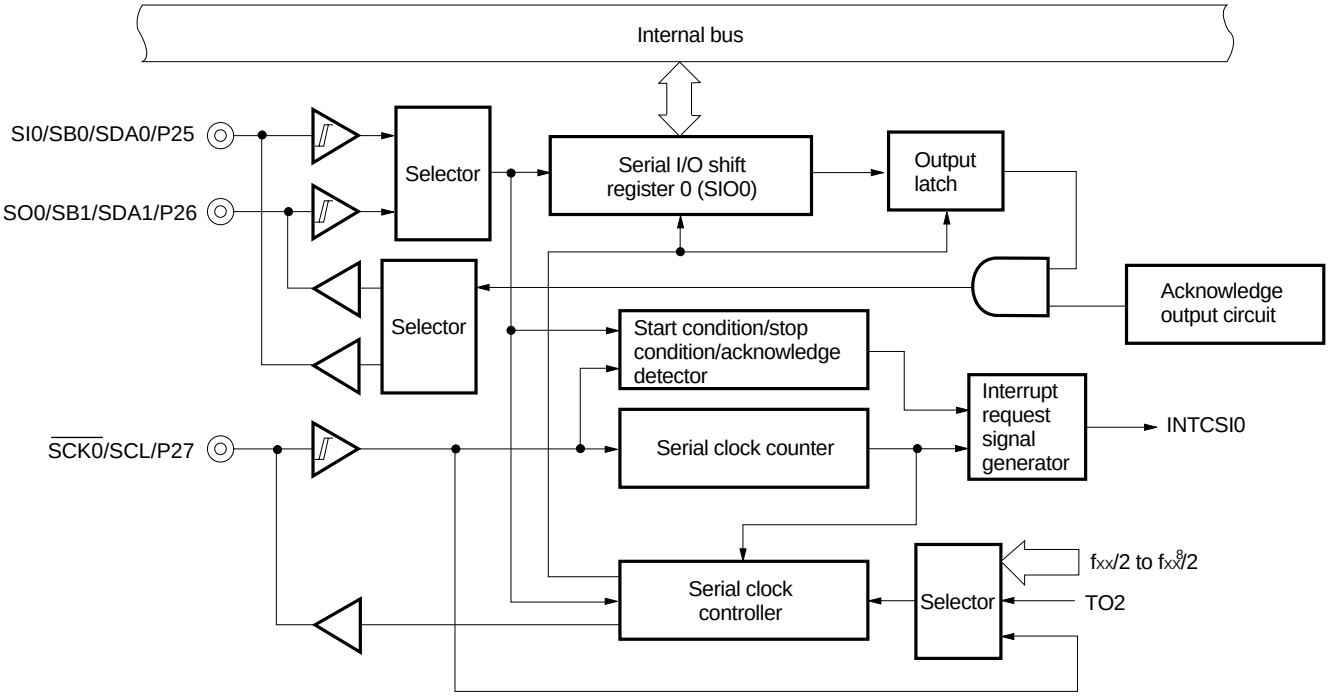


Figure 5-11. Block Diagram of Serial Interface Channel 1

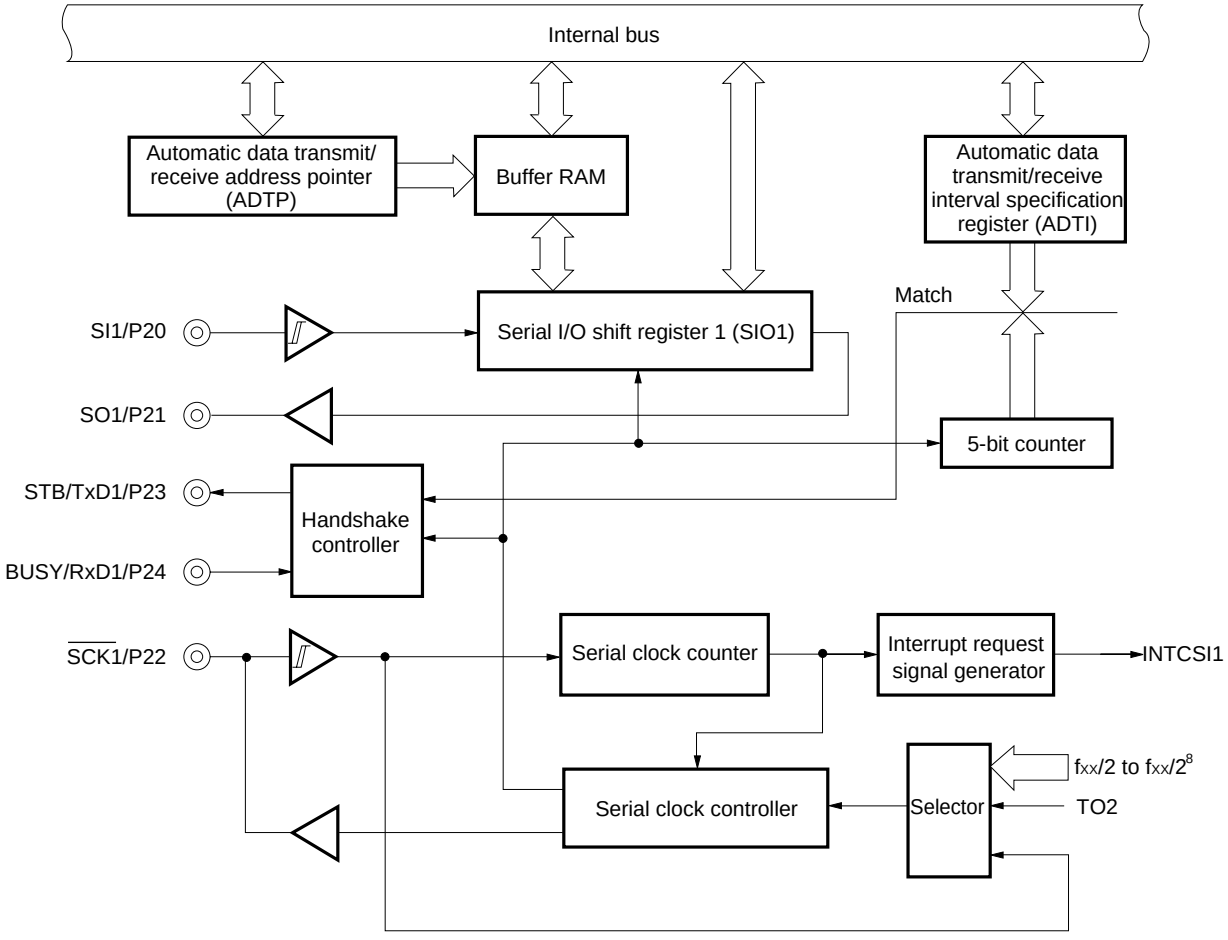
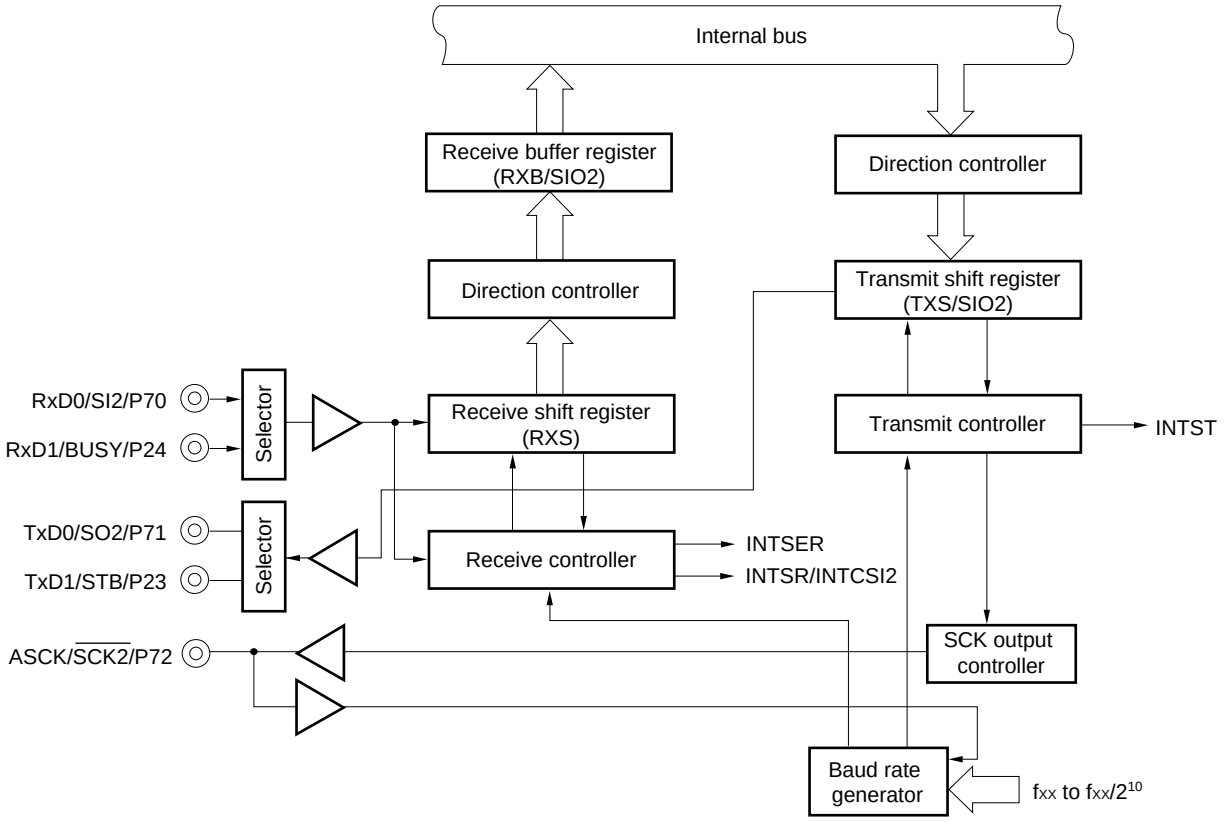


Figure 5-12. Block Diagram of Serial Interface Channel 2

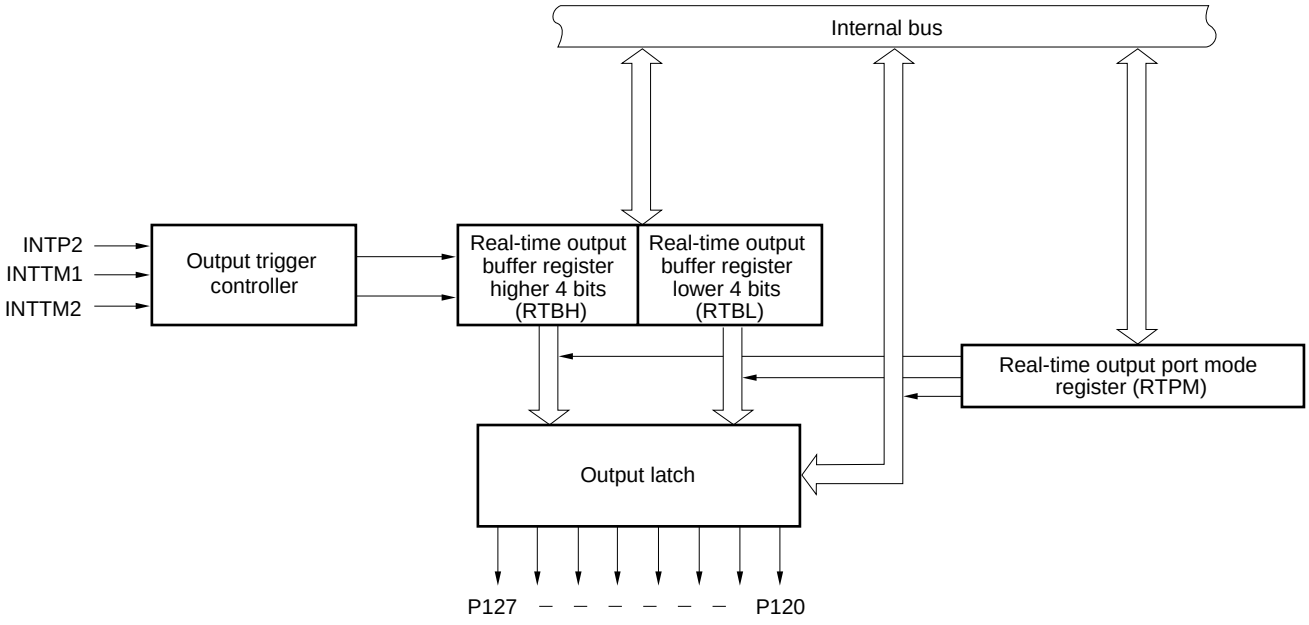


5.9 Real-Time Output Ports

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt request and external interrupt request generation in order to output off-chip. This is the real-time output function. Pins used to output off-chip are called real-time output ports.

By using a real-time output port, a signal with no jitter can be output. This is most applicable to control of stepper motors, etc.

Figure 5-13. Block Diagram of Real-Time Output Port



6. INTERRUPT AND TEST FUNCTIONS

6.1 Interrupt Functions

The interrupt function includes, three different kinds of interrupts from 21 sources, as shown below.

- Non-maskable: 1
- Maskable: 19
- Software: 1

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	(B)
	8	INTCSI1	End of serial interface channel 1 transfer		0016H	
	9	INTSER	Occurrence of serial interface channel 2 UART reception error		0018H	
	10	INTSR	End of serial interface channel 2 UART reception		001AH	
		INTCSI2	End of serial interface channel 2 3-wire transfer			
	11	INTST	End of serial interface channel 2 UART transmission		001CH	

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated simultaneously. 0 is the highest order and 17 is the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Remark There are two types of interrupt source for the watchdog timer: Non-maskable interrupts and maskable interrupts (internal). Only one of these interrupts can be selected.

Table 6-1. Interrupt Source List (2/2)

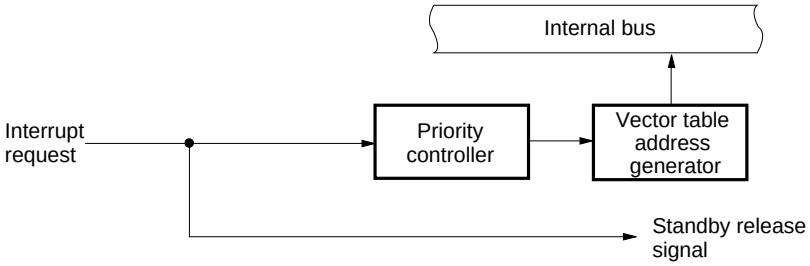
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Maskable	12	INTTM3	Reference time interval signal from watch timer	Internal	001EH	(B)
	13	INTTM00	Generation of match signal of 16-bit timer counter and capture/compare register (CR00)		0020H	
	14	INTTM01	Generation of match signal of 16-bit timer counter and capture/compare register (CR01)		0022H	
	15	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	16	INTTM2	Generation of match signal of 8-bit timer/ event counter 2		0026H	
	17	INTAD	End of conversion by A/D converter		0028H	
Software	–	BRK	Execution of BRK instruction	–	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated simultaneously. 0 is the highest order and 17 is the lowest.

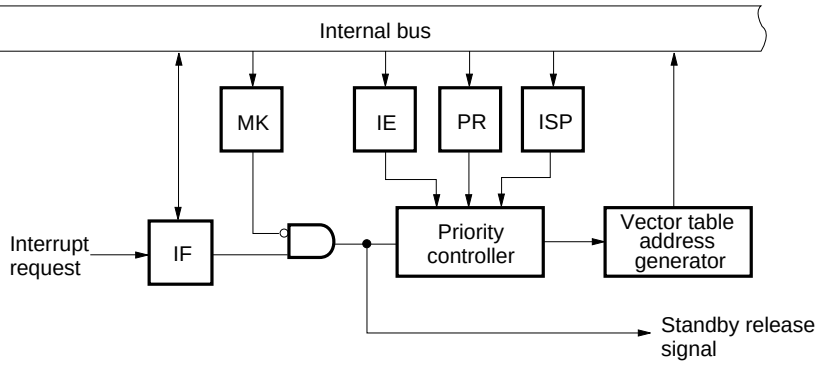
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

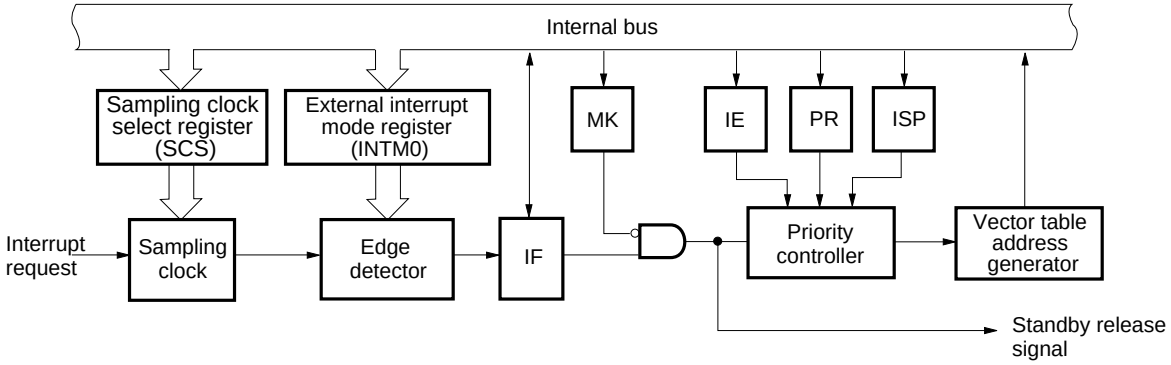
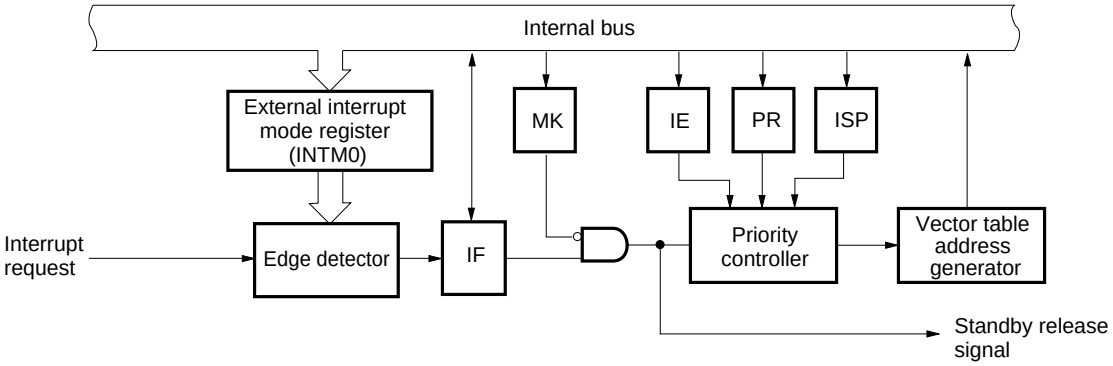
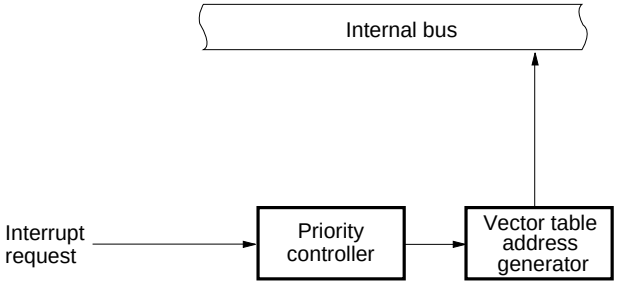


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

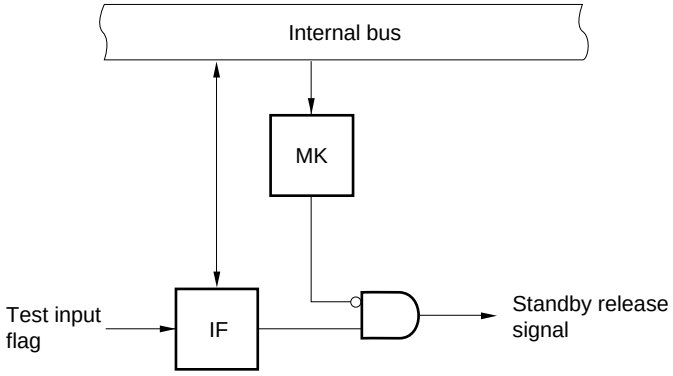
6.2 Test Functions

The test function includes the two test input sources shown in Table 6-2 below.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Basic Configuration of Test Function



IF: Test input flag

MK: Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

The external device expansion function connects external devices to areas other than the internal ROM, RAM, and SFR areas.

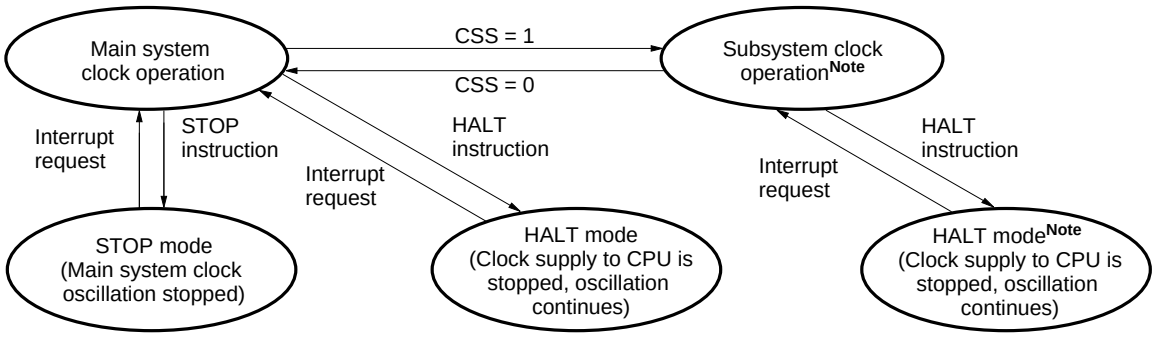
Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operating clock is stopped.
  The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used, resulting in extremely small power consumption.

Figure 8-1. Standby Function



Note The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set the MCC (bit 7 of the processor clock control register (PCC)) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark CSS: Bit 4 of the processor clock control register (PCC).

9. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer program loop time detection

10. MASK OPTION

The μPD78005x and 78005xY have the following mask options.

- Pull-up resistor
  An on-chip pull-up resistor for P60 to P63 (I/O port) can be specified in 1-bit units.
  <1> Specifies on-chip pull-up resistor.
  <2> Does not specify on-chip pull-up resistor.

11. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + Byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + Byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOV, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second Operand / First Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand / First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second Operand / First Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

12. ELECTRICAL SPECIFICATIONS

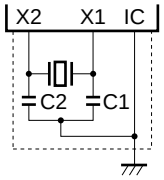
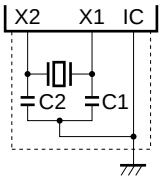
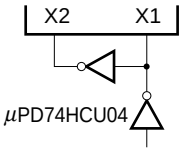
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P05, P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch open drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P01 to P05, P30 to P37, P56, P57, P60 to P67, P120 to P127		–15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		–15	mA
Output current, low	I_{OL}**Note**	Per pin	Peak value	30	mA
			rms value	15	mA
		Total for P50 to P55	Peak value	100	mA
			rms value	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			rms value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	Peak value	50	mA
			rms value	20	mA
		Total for P01 to P05, P30 to P37, P64 to P67, P120 to P127	Peak value	50	mA
			rms value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

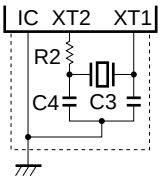
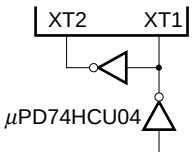
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P05, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P05, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch open drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			Note	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P05, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			Note	0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P05, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open drain, pulled-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When P07/XT1 pin is used as P07, the inverse phase of P07 should be input to XT2 pin using an inverter.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P05, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P05, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3 Note	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63		20	40	120	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01 to P05, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131		15	30	90	kΩ

Note When pull-up resistors are not connected to P60 to P63 (specified by the mask option), a low-level input leakage current of –200 μA (MAX.) flows only for 1.5 clocks (without wait) after a read instruction has been executed to port 6 (P6) or port mode register 6 (PM6). At times other than this 1.5-clock interval, a –3 μA (MAX.) current flows.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 5]	I_{DD1}	5.0 MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ±10%[Note 1]		3.5	7.7	mA
			V_{DD} = 3.0 V ±10%[Note 2]		0.92	2.2	mA
			V_{DD} = 2.0 V ±10%[Note 2]		0.47	1.2	mA
		5.0 MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ±10%[Note 1]		6.1	12.3	mA
			V_{DD} = 3.0 V ±10%[Note 2]		1.6	3.5	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ±10%				
			Peripheral functions operating			5.5	mA
			Peripheral functions not operating		0.97	2.4	mA
			V_{DD} = 3.0 V ±10%				
			Peripheral functions operating			2.1	mA
			Peripheral functions not operating		0.38	0.92	mA
			V_{DD} = 2.0 V ±10%				
			Peripheral functions operating			1.1	mA
			Peripheral functions not operating		0.19	0.46	mA
		5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ±10%				
			Peripheral functions operating			7.5	mA
			Peripheral functions not operating		1.2	2.9	mA
			V_{DD} = 3.0 V ±10%				
			Peripheral functions operating			3.3	mA
			Peripheral functions not operating		0.48	1.2	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 6]	V_{DD} = 5.0 V ±10%		46	92	μA
			V_{DD} = 3.0 V ±10%		25	50	μA
			V_{DD} = 2.0 V ±10%		12.5	25	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 6]	V_{DD} = 5.0 V ±10%		22.5	50	μA
			V_{DD} = 3.0 V ±10%		3.2	13.2	μA
			V_{DD} = 2.0 V ±10%		1.5	11.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ±10%		1.0	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
			V_{DD} = 2.0 V ±10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

2. Low-speed mode operation (when the PCC is set to 04H).

3. Operation with main system clock $f_{XX} = f_X/2$ (when the oscillation mode select register (OSMS) is set to 00H)

4. Operation with main system clock $f_{XX} = f_X$ (when OSMS is set to 01H)

5. Refer to the current flowing to the V_{DD0} and V_{DD1} pins. The current flowing to the A/D converter, D/A converter, and on-chip pull-up resistor is not included.

6. When the main system clock operation is stopped.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	Operating with main system clock (f_{XX} = 2.5 MHz)**Note 1**	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		Operating with main system clock (f_{XX} = 5.0 MHz)**Note 2**	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
			2.7 V ≤ V_{DD} ≤ 3.5 V	0.8		32	μs
		Operating on subsystem clock		40**Note 3**	122	125	μs
TI00 input high-/low-level width	t_{TIH00}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$ + 0.1**Note 4**			μs
	t_{TIL00}	2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$ + 0.2**Note 4**			μs
				$2/f_{sam}$ + 0.5**Note 4**			μs
TI01 input high-/low-level width	t_{TIH01}	V_{DD} = 2.7 to 5.5 V		10			μs
	t_{TIL01}			20			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high-/low-level width	t_{TIH1}	V_{DD} = 4.5 to 5.5 V		100			ns
	t_{TIL1}			1.8			μs
Interrupt request input high-/low-level width	t_{INTH}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1**Note 4**			μs
	t_{INTL}		2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$ + 0.2**Note 4**			μs
				$2/f_{sam}$ + 0.5**Note 4**			μs
		INTP1 to INTP5, P40 to P47	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

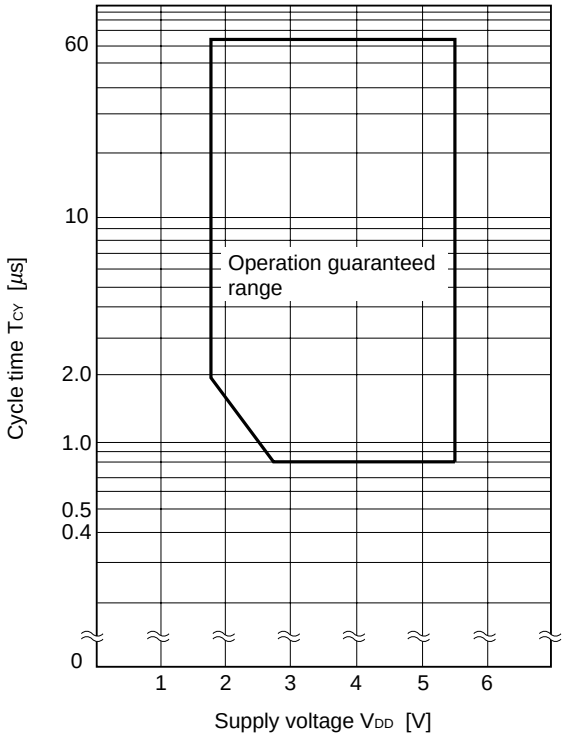
Notes 1. Operation with main system clock $f_{XX} = f_X/2$ (when the oscillation mode select register (OSMS) is set to 00H)

2. Operation with main system clock $f_{XX} = f_X$ (when OSMS is set to 01H)

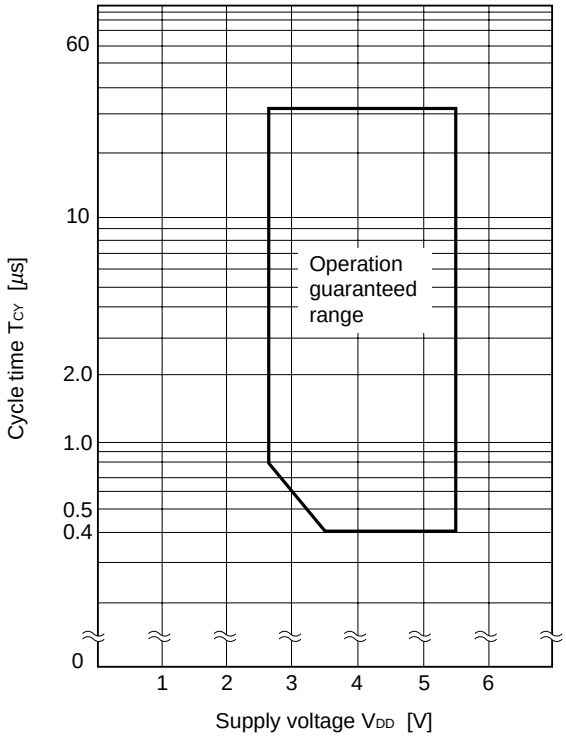
3. Value when external clock is used. When a crystal resonator is used, it is 114 μs (MIN.)

4. Selection of $f_{sam} = f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ is possible with bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register (SCS) (when N= 0 to 4).

T_{CY} vs. V_{DD} (@$f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs. V_{DD} (@$f_{XX} = f_X$ main system clock operation)



(2) Read/write operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Time from address to data input	t_{ADD1}			(2.85 + 2n) t_{CY} – 80	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 100	ns
Time from $\overline{RD}\downarrow$ to data input	t_{RDD1}			(2 + 2n) t_{CY} – 100	ns
	t_{RDD2}			(2.85 + 2n) t_{CY} – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(2 + 2n) t_{CY} – 60		ns
	t_{RDL2}		(2.85 + 2n) t_{CY} – 60		ns
Time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
Time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1.15 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.85 + 2n) t_{CY} – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.85 + 2n) t_{CY} – 60		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		25		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
Time from $\overline{RD}\uparrow$ to address hold at external fetch	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
Time from $\overline{RD}\uparrow$ to write data output	t_{RDWD}		40		ns
Time from $\overline{WR}\downarrow$ to write data output	t_{WRWD}		0	50	ns
Time from $\overline{WR}\uparrow$ to address hold	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}$ + 40	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) When MCS = 0 or PCC2 to PCC0 ≠ 000B (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Time from address to data input	t_{ADD1}			(3 + 2n) t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 200	ns
Time from $\overline{RD}\downarrow$ to data input	t_{RDD1}			(1.4 + 2n) t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n) t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n) t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n) t_{CY} – 20		ns
Time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
Time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n) t_{CY} – 60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4 + 2n) t_{CY} – 20		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		0.4t_{CY} – 30		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		1.4t_{CY} – 30		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Time from $\overline{RD}\uparrow$ to address hold at external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Time from $\overline{RD}\uparrow$ to write data output	t_{RDWD}		0.4t_{CY} – 20		ns
Time from $\overline{WR}\downarrow$ to write data output	t_{WRWD}		0	60	ns
Time from $\overline{WR}\uparrow$ to address hold	t_{WRADH}		t_{CY}	t_{CY} + 60	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(c) When MCS = 0 or PCC2 to PCC0 ≠ 000B (T_A = –40 to +85°C, V_{DD} = 1.8 to 2.7 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 150		ns
Address setup time	t_{ADS}		t_{CY} – 150		ns
Address hold time	t_{ADH}		0.37t_{CY} – 40		ns
Time from address to data input	t_{ADD1}			(3 + 2n) t_{CY} – 320	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 300	ns
Time from $\overline{RD}\downarrow$ to data input	t_{RDD1}			(1.37 + 2n) t_{CY} – 120	ns
	t_{RDD2}			(2.37 + 2n) t_{CY} – 120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.37 + 2n) t_{CY} – 20		ns
	t_{RDL2}		(2.37 + 2n) t_{CY} – 20		ns
Time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{RDWT1}			t_{CY} – 200	ns
	t_{RDWT2}			2t_{CY} – 200	ns
Time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{WRWT}			2t_{CY} – 200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.37 + 2n) t_{CY} – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.37 + 2n) t_{CY} – 20		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		0.37t_{CY} – 50		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		1.37t_{CY} – 50		ns
Delay time from $\overline{RD}\uparrow$ to ASTB at external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Time from $\overline{RD}\uparrow$ to address hold at external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Time from $\overline{RD}\uparrow$ to write data output	t_{RDWD}		0.37t_{CY} – 40		ns
Time from $\overline{WR}\downarrow$ to write data output	t_{WRWD}		0	120	ns
Time from $\overline{WR}\uparrow$ to address hold	t_{WRADH}		t_{CY}	t_{CY} + 120	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		0.63t_{CY} + 350	2.63t_{CY} + 350	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		0.63t_{CY} + 240	2.63t_{CY} + 240	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3,200			ns
			4,800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
Delay time from $\overline{SCK0}$↓ to SO0 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SCK0 and SO0 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3,200			ns
				4,800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,600			ns
				2,400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	2.0 V ≤ V_{DD} ≤ 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
Delay time from $\overline{SCK0}$↓ to SO0 output	t_{KSO2}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5V			300	ns
						500	ns
$\overline{SCK0}$ rise/fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note C is the load capacitance of the SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	1,600			ns
			2.0 V ≤ V_{DD} ≤ 2.7 V	3,200			ns
				4,800			ns
$\overline{SCK0}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 5.5 V	t_{KCY3}/2 – 160			ns
				t_{KCY3}/2 – 190			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	t_{KCY3}/2 – 50			ns
				t_{KCY3}/2 – 100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			600			ns
							ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO3}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	2.7 V ≤ V_{DD} ≤ 5.5 V		1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3,200			ns
				4,800			ns
$\overline{SCK0}$ high-level width	t_{KH4}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,300			ns
				2,100			ns
$\overline{SCK0}$ low-level width	t_{KL4}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,600			ns
				2,400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		800	ns
$\overline{SCK0}$ rise/fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) SBI mode ($\overline{SCK0}$... Internal clock output) (μPD78005x only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3,200			ns
				4,800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH5}, t_{KL5}	4.5 V ≤ V_{DD} ≤ 5.5 V		t_{KCY5}/2 – 50			ns
				t_{KCY5}/2 – 150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			t_{KCY5}/2			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1,000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY5}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY5}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY5}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY5}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(vi) SBI mode ($\overline{SCK0}$... External clock input) (μPD78005x only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3,200			ns
				4,800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH6}, t_{KL6}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.0 V ≤ V_{DD} < 4.5 V		1,600			ns
				2,400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			t_{KCY6}/2			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1,000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY6}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY6}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY6}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY6}			ns
$\overline{SCK0}$ rise/fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(vii) I²C bus mode (SCL ... Internal clock output) (μPD78005xY only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 KΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V_{DD} < 2.7 V	20			μs
				30			μs
SCL high-level width	t_{KH7}		V_{DD} = 2.7 to 5.5 V	t_{KCY7} – 160			ns
				t_{KCY7} – 190			ns
SCL low-level width	t_{KL7}		V_{DD} = 4.5 to 5.5 V	t_{KCY7} – 50			ns
				t_{KCY7} – 100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}		2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} < 2.7 V	300			ns
				400			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
Delay time from SCL↓ to SDA0, SDA1 output	t_{KSO7}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↓	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}		V_{DD} = 2.0 to 5.5 V	400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines.

(viii) I²C bus mode (SCL ... External clock input) (μPD78005xY only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1,000			ns
SCL high-/low-level width	t_{KH8}, t_{KL8}	V_{DD} = 2.0 to 5.5 V		400			ns
				600			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		200			ns
				300			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
Delay time from SCL↓ to SDA0, SDA1 output	t_{KSO8}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}	V_{DD} = 2.0 to 5.5 V		400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}	V_{DD} = 2.0 to 5.5 V		500			ns
				800			ns
SCL rise/fall time	t_{R8}, t_{F8}	When using external device expansion function				160	ns
		When not using external device expansion function				1	μs

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3,200			ns
			4,800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2 – 50			ns
			t_{KCY9}/2 – 100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
Delay time from $\overline{SCK1}$↓ to SO1 output	t_{KSO9}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3,200			ns
				4,800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10},t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,600			ns
				2,400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KIS10}			400			ns
Delay time from $\overline{SCK1}$↓ to SO1 output	t_{KSO10}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3,200			ns
			4,800			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH11},t_{KL11}	V_{DD} = 4.5 to 5.5 V	t_{KCY11}/2 – 50			ns
			t_{KCY11}/2 – 100			ns
SI1 setup time (to $\overline{\text{SCK1}}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{\text{SCK1}}$↑)	t_{KSI11}		400			ns
Delay time from $\overline{\text{SCK1}}$↓ to SO1 output	t_{KSO11}	C = 100 pF[Note]			300	ns
STB↑ from $\overline{\text{SCK1}}$↑	t_{SBD}		t_{KCY11}/2 – 100		t_{KCY11}/2 + 100	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} < 5.5 V	t_{KCY11} – 30		t_{KCY11} + 30	ns
		2.0 V < V_{DD} < 2.7 V	t_{KCY11} – 60		t_{KCY11} + 60	ns
			t_{KCY11} – 90		t_{KCY11} + 90	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{\text{SCK1}}$↓ from busy inactive	t_{SPS}				2t_{KCY11}	ns

Note C is the load capacitance of the $\overline{\text{SCK1}}$ and SO1 output lines.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3,200			ns
				4,800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,600			ns
				2,400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK12}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI12}			400			ns
Delay time from $\overline{SCK1}$↓ to SO1 output	t_{KSO12}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise/fall time	t_{R12}, t_{F12}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3,200			ns
			4,800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH13}, t_{KL13}	V_{DD} = 4.5 to 5.5 V	$t_{KCY13}/2 - 50$			ns
			$t_{KCY13}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK13}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI13}		400			ns
Delay time from $\overline{SCK2}$↓ to SO2 output	t_{KSO13}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY14}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3,200			ns
				4,800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH14}, t_{KL14}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1,600			ns
				2,400			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK14}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI14}			400			ns
Delay time from $\overline{SCK2}$↓ to SO2 output	t_{KSO14}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise/fall time	t_{R14}, t_{F14}	Other than below				160	ns
		V_{DD} = 4.5 to 5.5 V When not using external device expansion function				1	μs

Note C is the load capacitance of the SO2 output line.

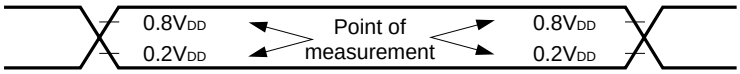
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78,125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39,063	bps
		2.0 V ≤ V_{DD} < 2.7 V			19,531	bps
					9,766	bps

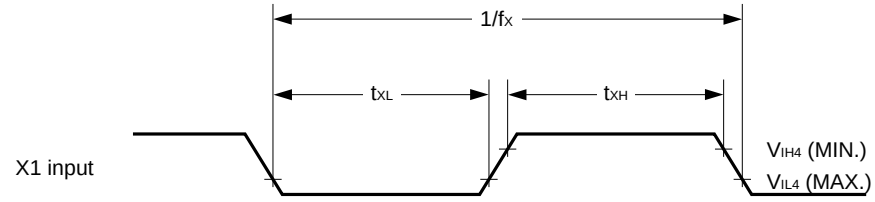
(iv) UART mode (External clock input)

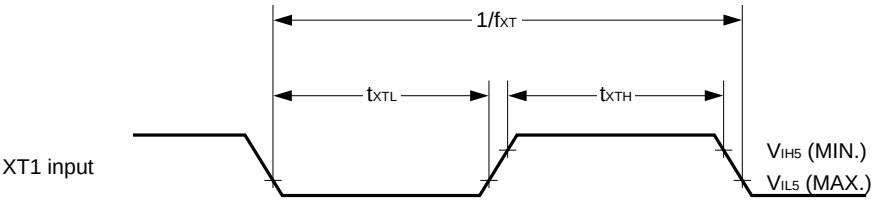
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY15}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3,200			ns
			4,800			ns
ASCK high-/low-level width	t_{KH15}, t_{KL15}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1,600			ns
			2,400			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39,063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19,531	bps
		2.0 V ≤ V_{DD} < 2.7 V			9,766	bps
					6,510	bps
ASCK rise/fall time	t_{R15}, t_{F15}	V_{DD} = 4.5 to 5.5 V, when not using external device expansion function.			1,000	ns
					160	ns

AC Timing Measurement Points (Excluding X1, XT1 Inputs)

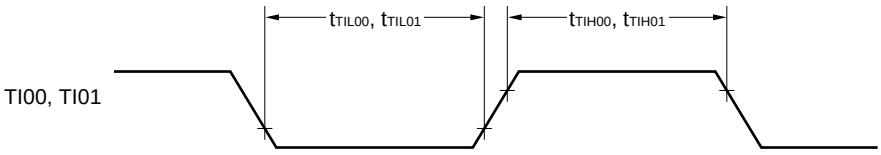


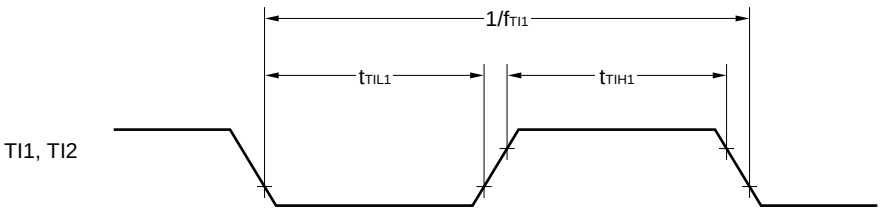
Clock Timing





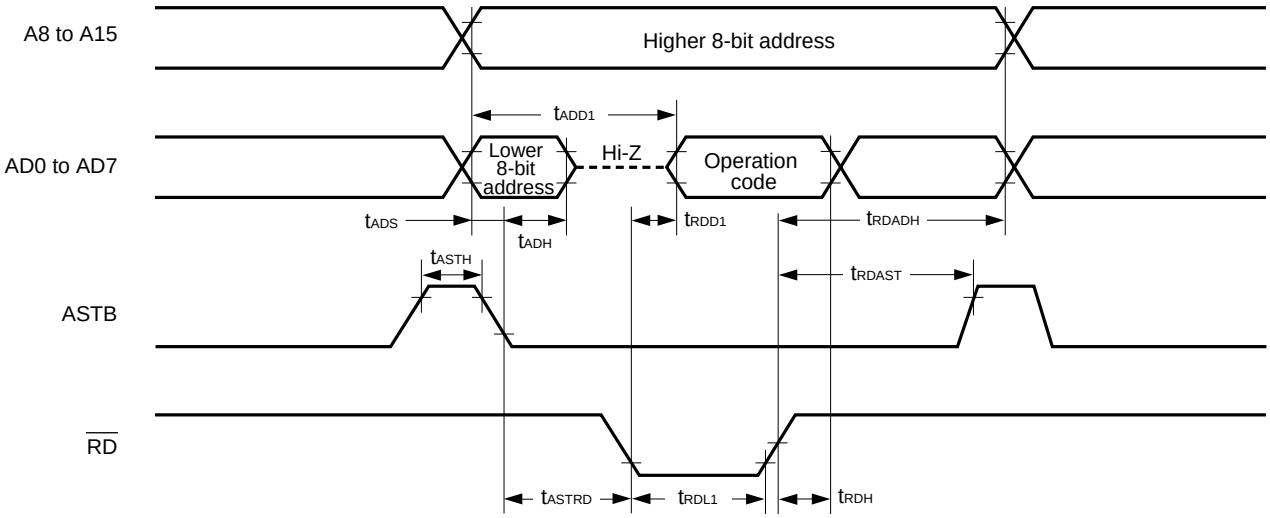
TI Timing



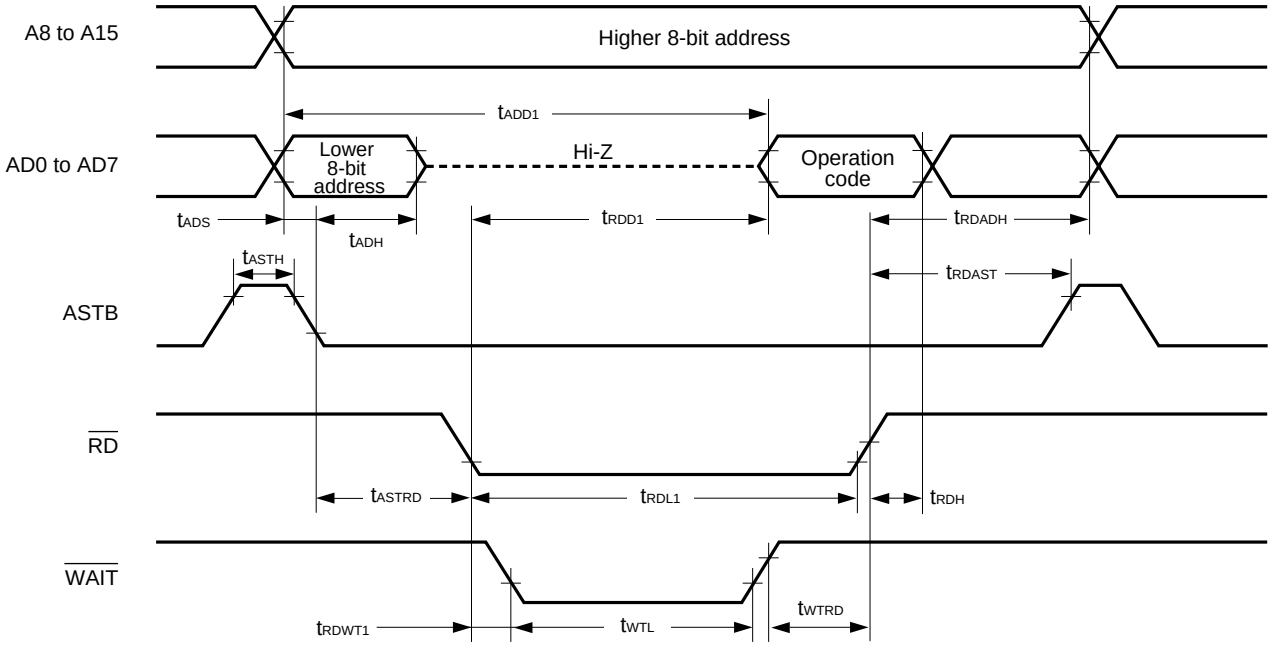


Read/Write Operation

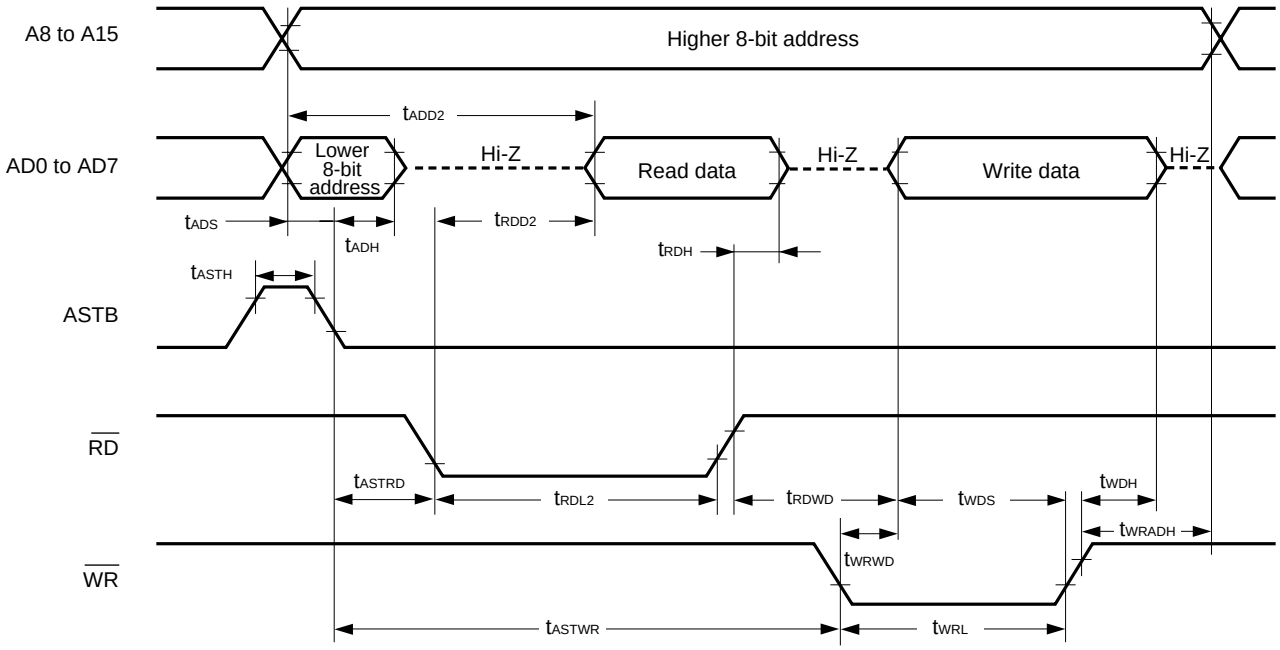
External fetch (no wait):



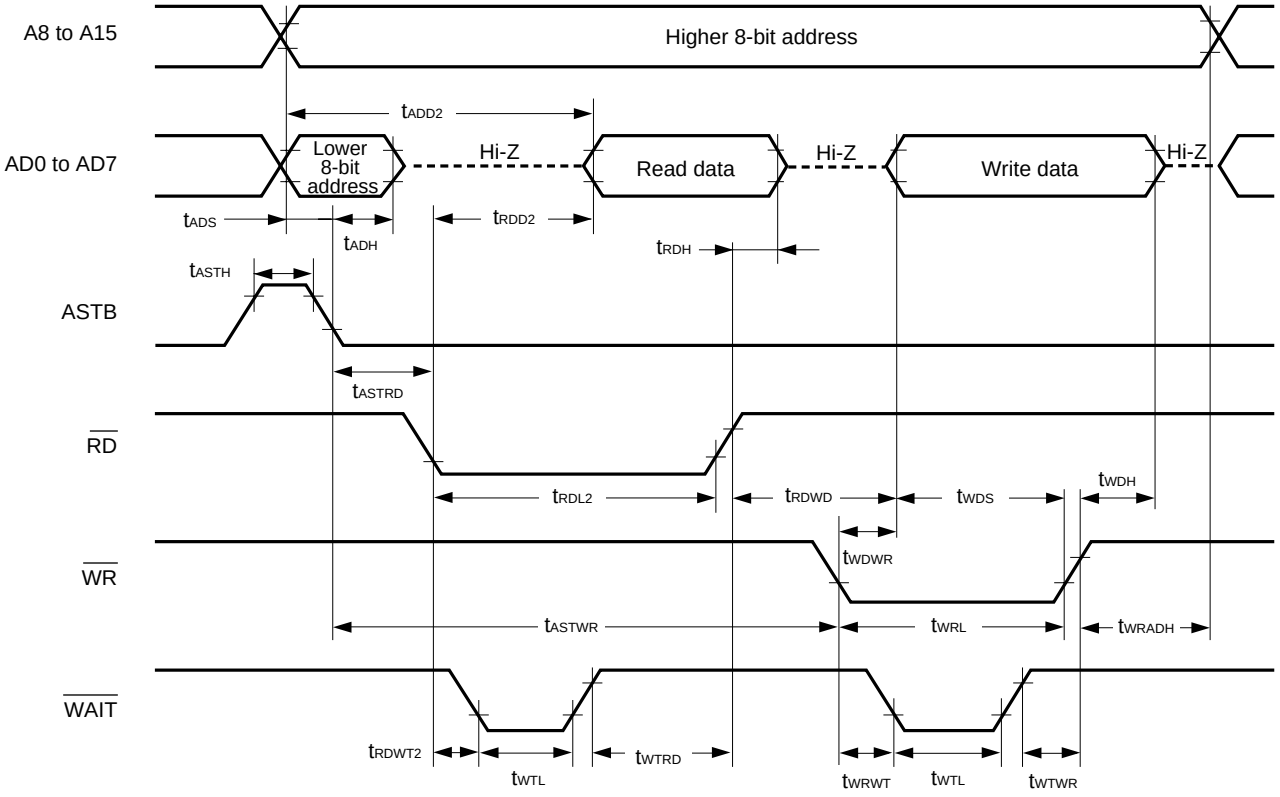
External fetch (wait insertion):



External data access (no wait):

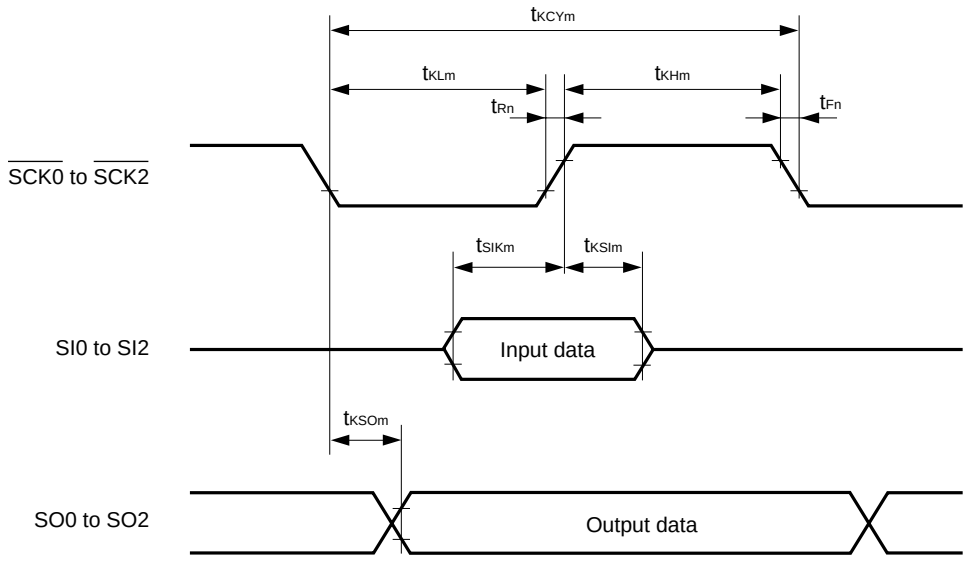


External data access (wait insertion):



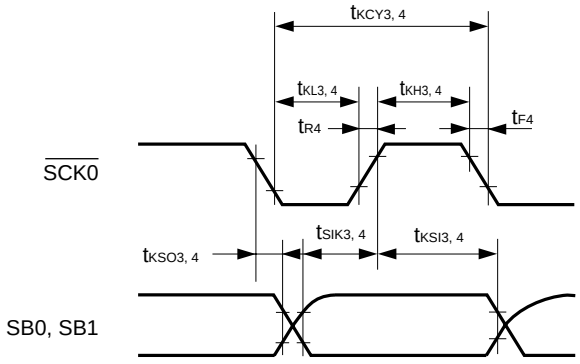
Serial Transfer Timing

3-wire serial I/O mode:

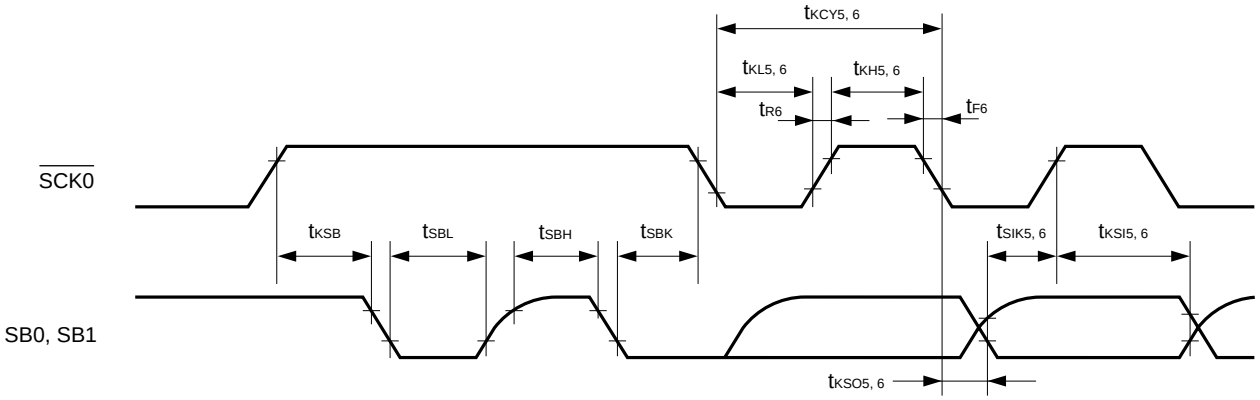


m = 1, 2, 9, 10, 13, 14
n = 2, 10, 14

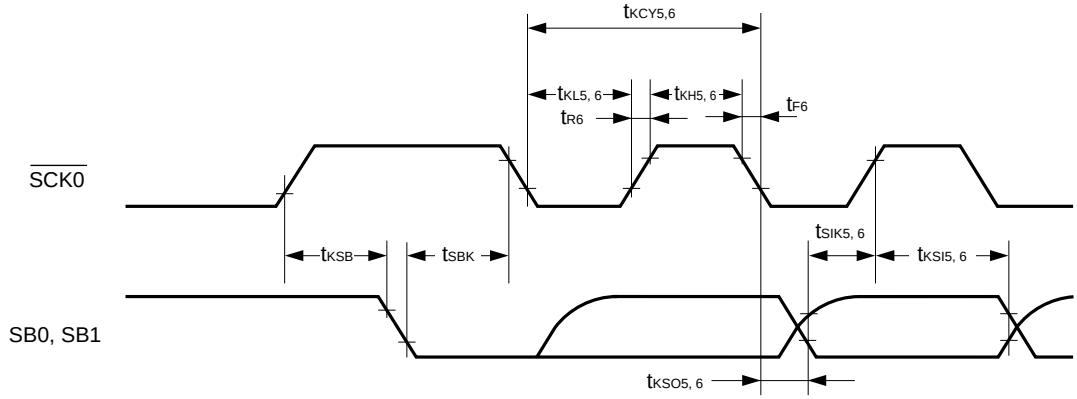
2-wire serial I/O mode:



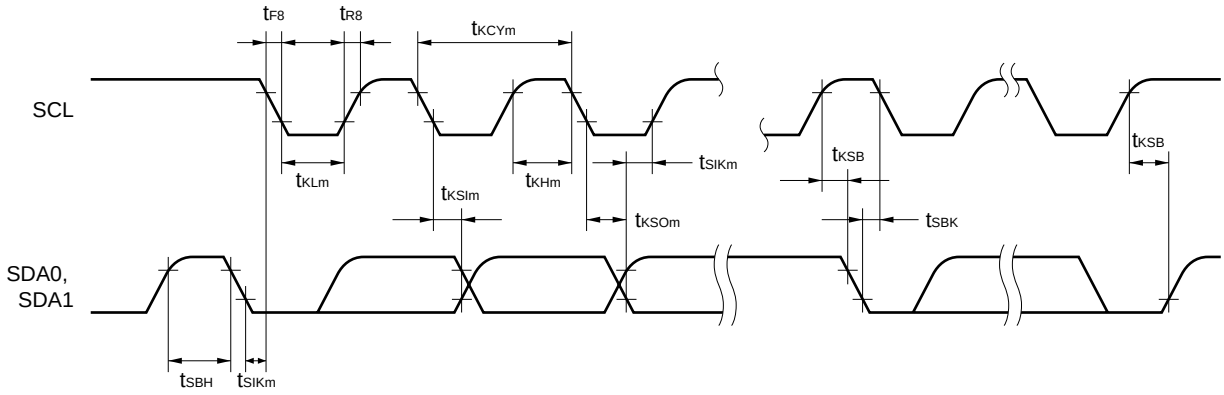
SBI mode (bus release signal transfer):



SBI mode (command signal transfer):

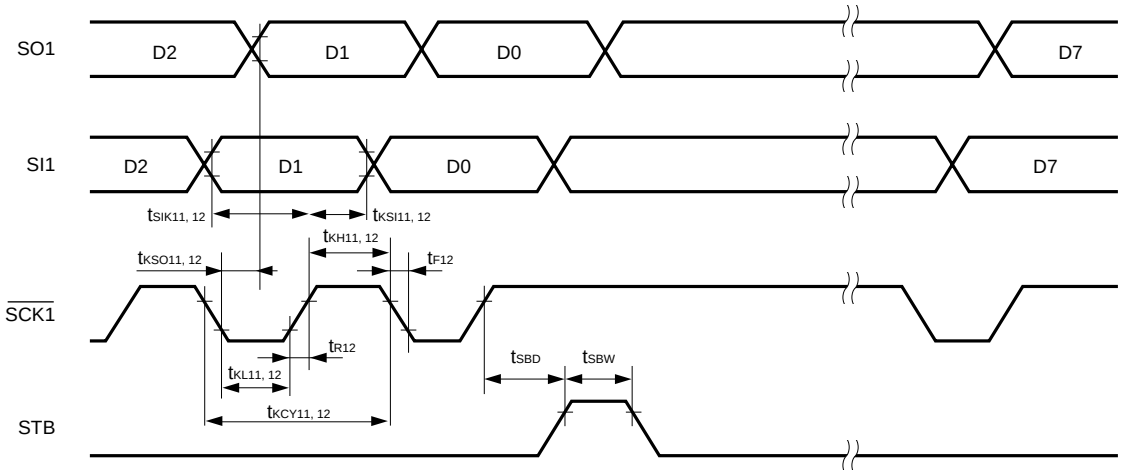


I²C bus mode:



m = 7, 8

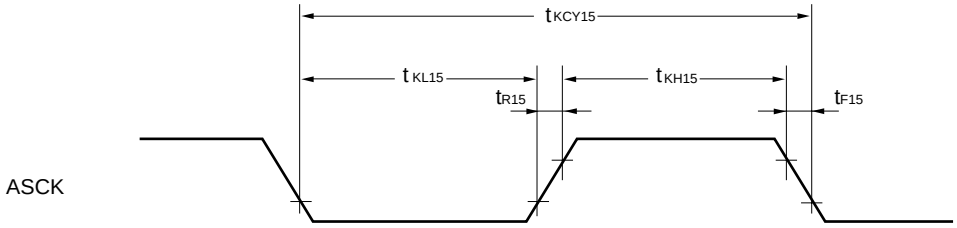
3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):

Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART mode (external clock input):



★ **A/D Converter Characteristics**

(μPD780053, 780054, 780055, 780056, 780058B, 780053Y, 780054Y, 780055Y, 780056Y, 780058BY)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]		1.8 V ≤ AV_{REF0} < 2.7 V			±1.4	%FSR
		2.7 V ≤ AV_{REF0} < 5.5 V			±0.6	%FSR
Conversion time	T_{CONV1}	1.8 V ≤ AV_{REF0} < 2.7 V	40		100	μs
	T_{CONV2}	2.7 V ≤ AV_{REF0} < 5.5 V	16		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		1.8		V_{DD}	V
AV_{REF0} current	I_{REF0}	When A/D converter is operating[Note 2]		500	1,500	μA
		When A/D converter is not operating[Note 3]		0	3	μA

Notes 1. Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value (%FSR).
2. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 1.
3. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 0.

A/D Converter Characteristics (μPD780058)

(T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]					±0.6	%FSR
Conversion time	T_{CONV}		16		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		V_{DD}	V
AV_{REF0} current	I_{REF0}	When A/D converter is operating[Note 2]		500	1,500	μA
		When A/D converter is not operating[Note 3]		0	3	μA

Notes 1. Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value (%FSR).
2. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 1.
3. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 0.

Caution The operating voltage range of the A/D converter and D/A converter of the μPD780058 is V_{DD} = 2.7 to 5.5 V.

★ **D/A Converter Characteristics**

(μPD780053, 780054, 780055, 780056, 780058B, 780053Y, 780054Y, 780055Y, 780056Y, 780058BY)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error		R = 2 MΩ[Note 1]			1.2	%
		R = 4 MΩ[Note 1]			0.8	%
		R = 10 MΩ[Note 1]			0.6	%
Settling time		C = 30 pF[Note 1], AV_{REF1} = 1.8 to 2.7 V			10	μs
		C = 30 pF[Note 1]			15	μs
Output resistance	R_O	**Note 2**		8		kΩ
Analog reference voltage	AV_{REF1}		1.8		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note 2**			2.5	mA
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]	4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance, respectively.

2. Value for one D/A converter channel

Remark DACS0 and DACS1: D/A conversion value setting registers 0, 1

D/A Converter Characteristics (μPD780058)

(T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error		R = 2 MΩ[Note 1]			1.2	%
		R = 4 MΩ[Note 1]			0.8	%
		R = 10 MΩ[Note 1]			0.6	%
Settling time		C = 30 pF[Note 1]			15	μs
Output resistance	R_O	**Note 2**		8		kΩ
Analog reference voltage	AV_{REF1}		2.7		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note 2**			2.5	mA
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]	4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance, respectively.

2. Value for one D/A converter channel

Remark DACS0 and DACS1: D/A conversion value setting registers 0, 1

Caution The operating voltage range of the A/D converter and D/A converter of the μPD780058 is V_{DD} = 2.7 to 5.5 V.

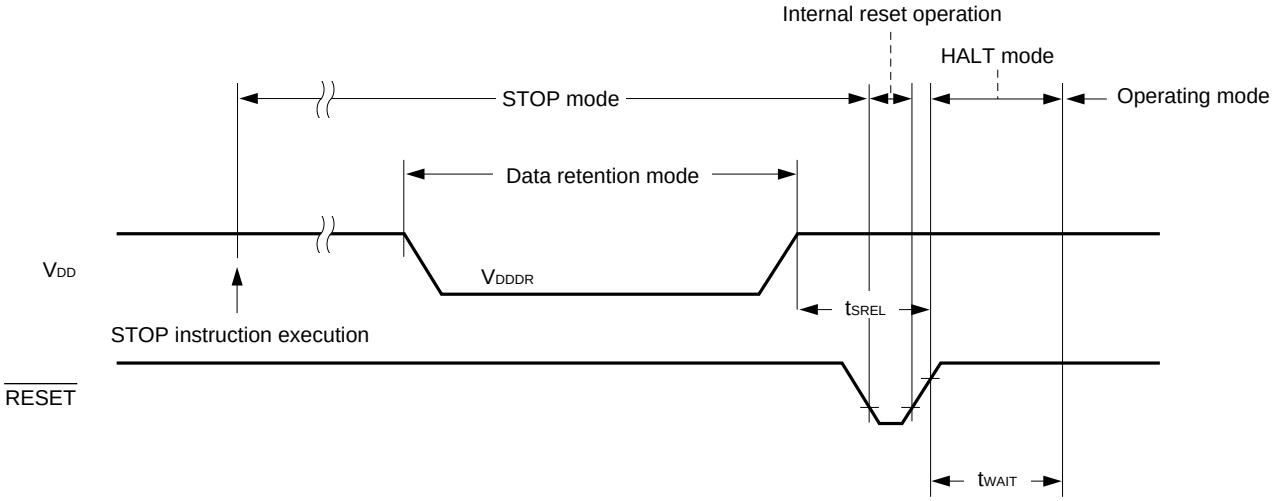
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

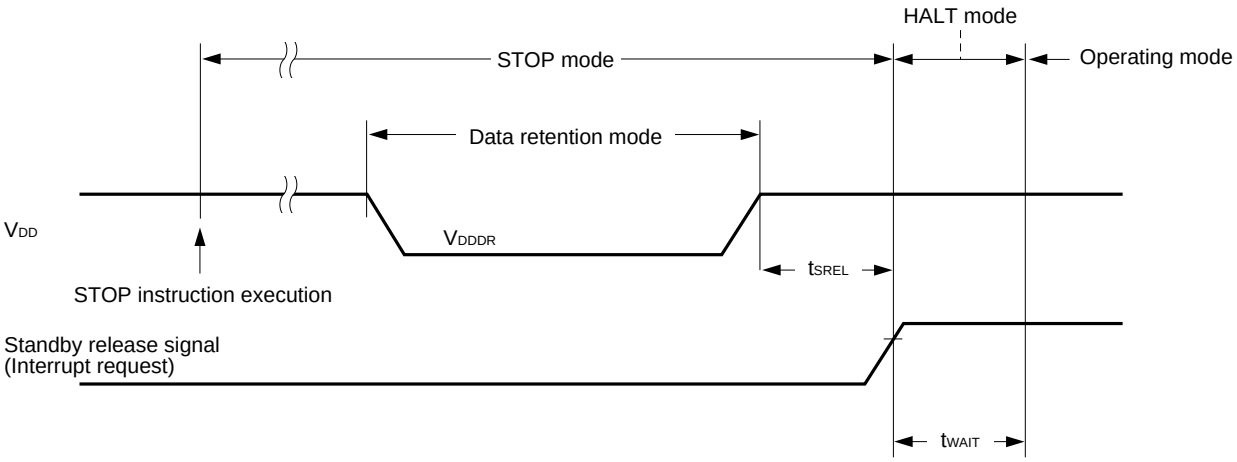
Note Selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

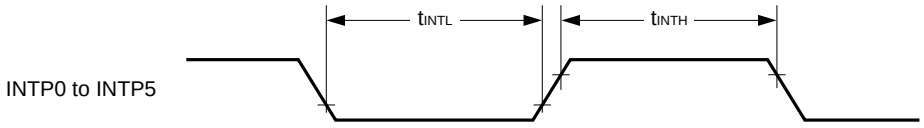
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



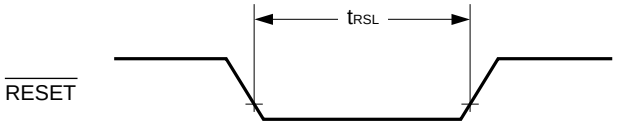
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

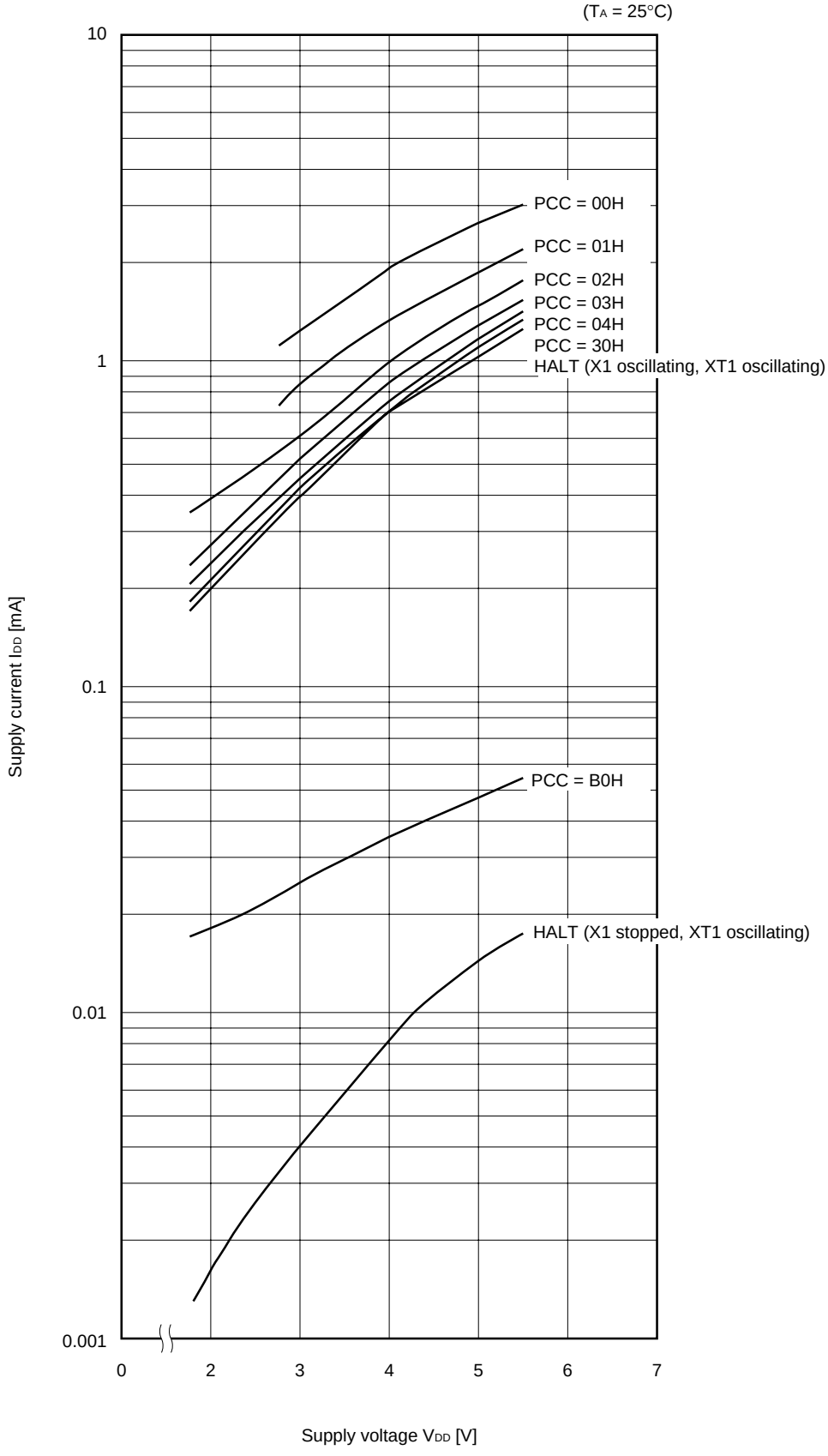


$\overline{\text{RESET}}$ Input Timing

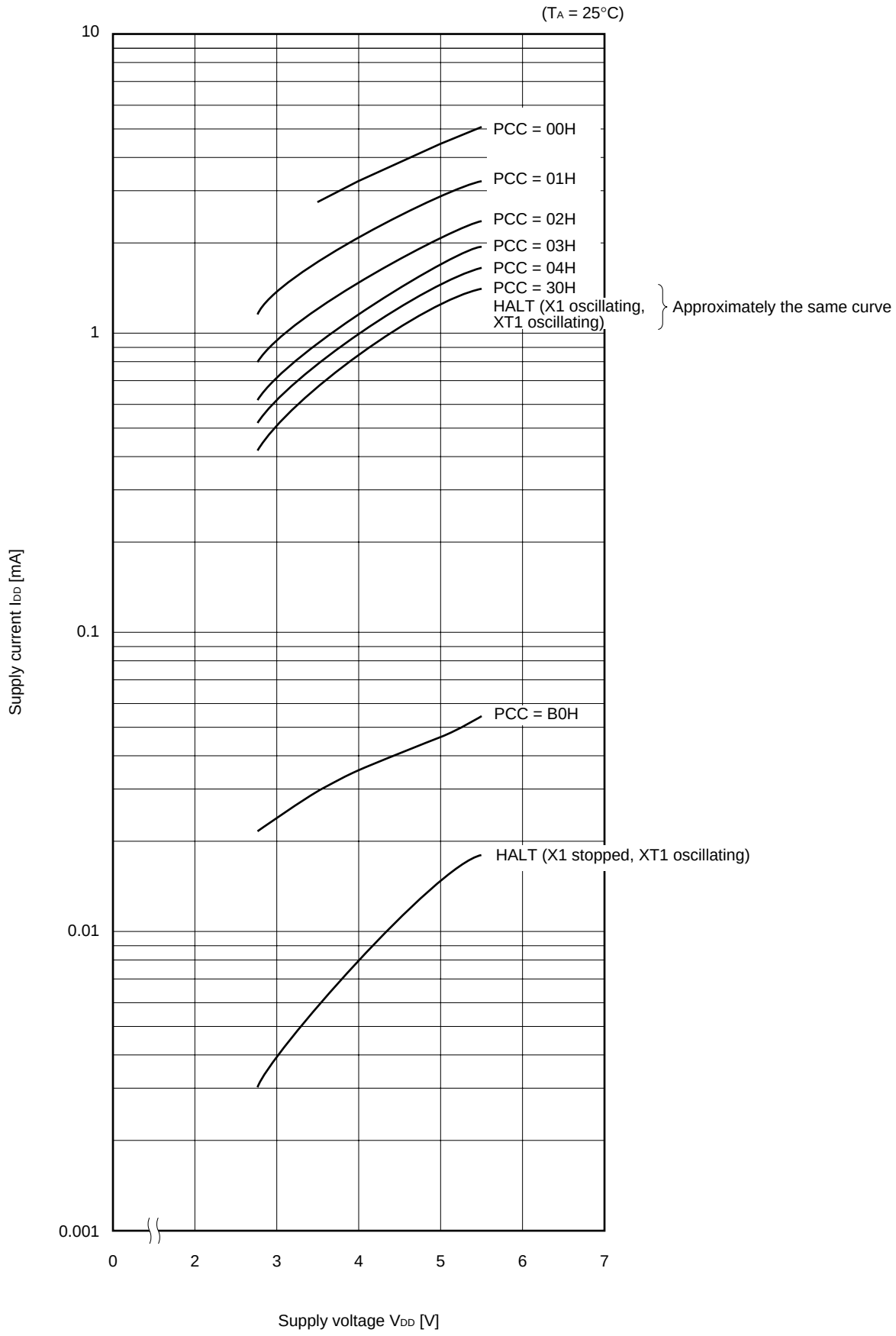


13. CHARACTERISTICS CURVES (REFERENCE VALUES)

V_{DD} vs I_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)

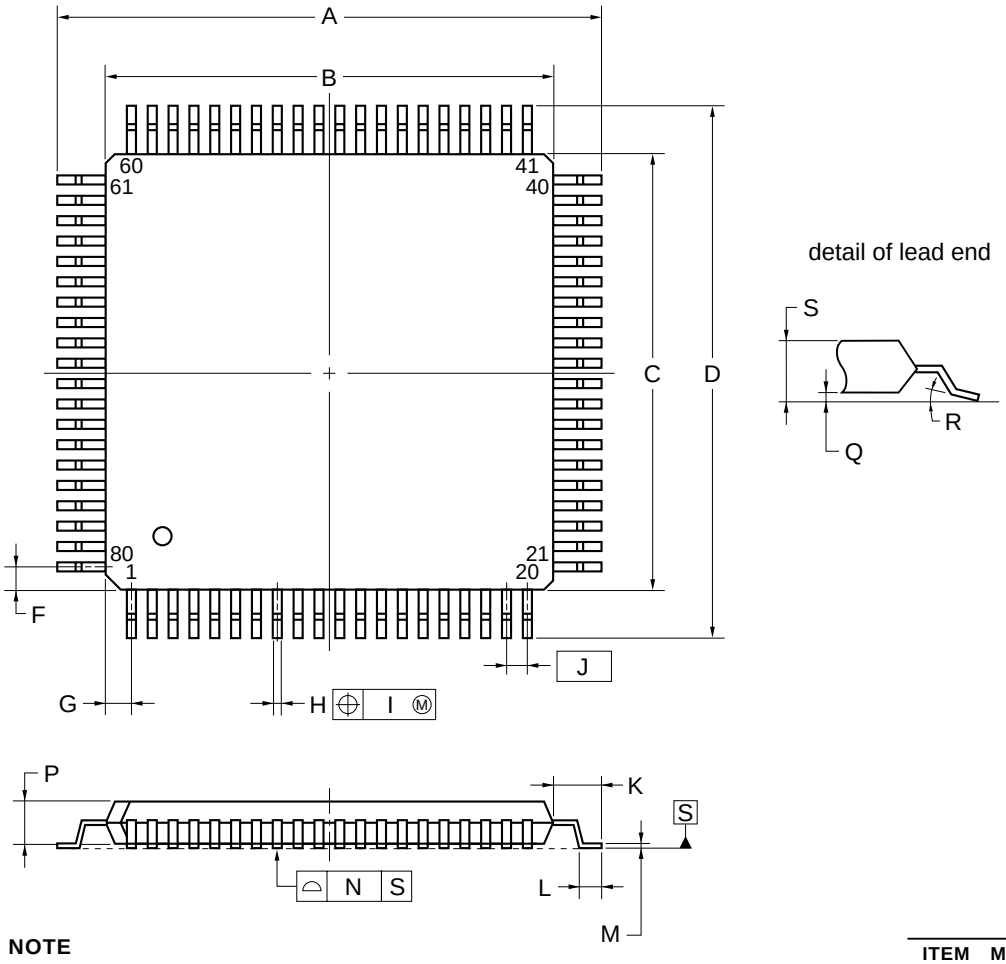


V_{DD} vs I_{DD} ($f_X = f_{XX}$ = 5.0 MHz)



14. PACKAGE DRAWINGS

80-PIN PLASTIC QFP (14x14)



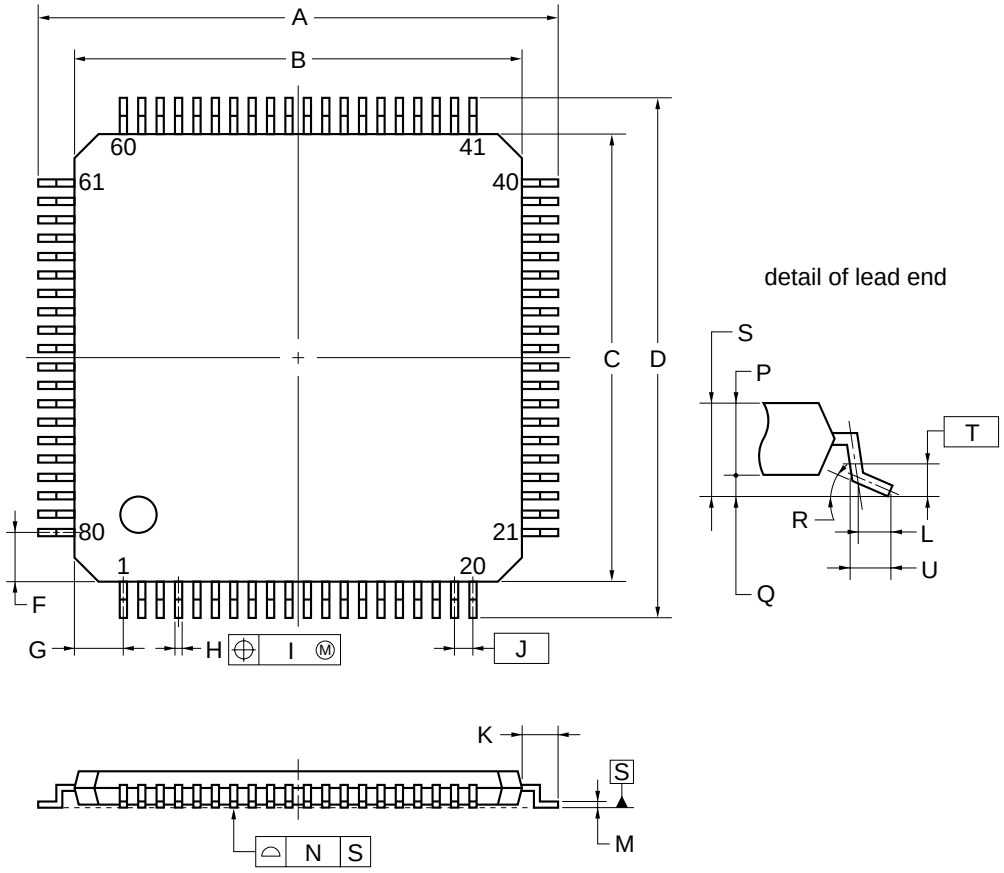
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

15. RECOMMENDED SOLDERING CONDITIONS

The μPD78005x and 78005xY should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 15-1. Surface Mounting Type Soldering Conditions (1/2)

μPD780053GC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780054GC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780055GC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780056GC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780058GC-×××-8BT: 80-pin plastic QFP (14 × 14)
★ μPD780058BGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780053YGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780054YGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780055YGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD780056YGC-×××-8BT: 80-pin plastic QFP (14 × 14)
★ μPD780058BYGC-×××-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Soldering bath temperature: 260°C or less, Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or less, Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 15-1. Surface Mounting Type Soldering Conditions (2/2)

μPD780053GK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780054GK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780055GK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780056GK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780058GK-×××-9EU: 80-pin plastic TQFP (12 × 12)
★ μPD780058BGK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780053YGK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780054YGK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780055YGK-×××-9EU: 80-pin plastic TQFP (12 × 12)
μPD780056YGK-×××-9EU: 80-pin plastic TQFP (12 × 12)
★ μPD780058BYGK-×××-9EU: 80-pin plastic TQFP (12 × 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	–	–
Partial heating	Pin temperature: 300°C or less, Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780058 and 780058Y Subseries. Also, refer to **(6) Cautions on using development tools.**

(1) Software package

SP78K0	CD-ROM that integrates the development tools (software) common to the 78K/0 Series in one package

(2) Language processing software

RA78K0	Assembler package common to the 78K/0 Series
CC78K0	C compiler package common to the 78K/0 Series
DF780058	Device file for the μPD780058, 780058Y Subseries
CC78K0-L	C compiler library source file common to the 78K/0 Series

(3) Flash memory writing tools

Flashpro III (Part number: FL-PR3, PG-FL3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-80GC-8BT FA-80GK-9EU	Adapter for flash memory writing

(4) Debugging tools

- **When using the IE-78K0-NS, IE-78K0-NS-A in-circuit emulator**

IE-78K0-NS	In-circuit emulator common to the 78K/0 Series
IE-78K0-NS-PA	Performance board to enhance and expand the functions of the IE-78K0-NS
IE-78K0-NS-A	In-circuit emulator that combines IE-78K0-NS and IE-78K0-NS-PA
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS and IE-78K0-NS-A
IE-70000-98-IF-C	Interface adapter used when a PC-9800 series PC (except notebook types) is used as the host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable used when a PC-9800 series notebook-types PC is used as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter necessary when an IBM PC/AT™ or compatible is used as the host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter necessary when using a PC with PCI bus as the host machine
IE-780308-NS-EM1	Emulation board common to the μPD780308 Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NP-80GK	Emulation probe for 80-pin plastic TQFP (GK-9EU type)
TGK-080SDW	Conversion adapter to connect the NP-80GK and a target system board 80-pin plastic TQFP (GK-9EU type) can be mounted
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-8BT type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to the 78K/0 Series

- **When using the IE-78001-R-A in-circuit emulator**

IE-78001-R-A	In-circuit emulator common to the 78K/0 Series
IE-70000-98-IF-C	Adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-780308-R-EM	Emulation board common to the μPD780308 Subseries
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (GK-9EU type)
TGK-080SDW	Conversion adapter to connect the EP-78054GK-R and a target system on which an 80-pin plastic TQFP (GK-9EU type) can be mounted
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-8BT type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	78K/0 Series common system simulator
DF780058	Device file for the μPD780058, 780058Y Subseries

(5) Real-time OS

RX78K0	Real-time OS for the 78K/0 Series

(6) Cautions on using development tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780058.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780058.
- The FL-PR3, FA-80GC-8BT, FA80GK-9EU, NP-80GC, and NP-80GK are products of Naito Densei Machida ★ Mfg. Co., Ltd. (TEL: +81-45-475-4191).
- TGK-080SDW is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL: +81-3-3820-7112)
  Osaka Electronics Department (TEL: +81-6-6-244-6672)
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E).**
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC PC-9800 series [Japanese Windows™] IBM PC/AT compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™]
SP78K0	√	–
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K0	√Note	√

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780058, 780058Y Subseries User's Manual	U12013E
μPD780053, 780054, 780055, 780056, 780058, 780058B, 780053Y, 780054Y, 780055Y, 780056Y, 780058BY Data Sheet	This document
μPD780053(A), 780054(A), 780055(A), 780056(A), 780058B(A), 780053Y(A), 780054Y(A), 780055Y(A), 780056Y(A), 780058BY(A) Data Sheet	U15443E
μPD78F0058, 78F0058Y Data Sheet	U12092E
78K/0 Series User's Manual Instruction	U12326E
78K/0 Series Application Note Basic (III)	U10182E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Assembly Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K0S, SM78K0 System Simulator Ver.2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver.2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver.2.00 or Later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E
RX78K0 Real-Time OS	Fundamental	U11537E
	Installation	U11536E
Project Manager Ver. 3.12 or Later (Windows-Based)		U14610E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
IE-78K0-NS In-Circuit Emulator	U13731E
IE-78K0-NS-A In-Circuit Emulator	U14889E
IE-780308-NS-EM1 Emulation Board	U13304E
IE-78001-R-A In-Circuit Emulator	U14142E
IE-780308-R-EM Emulation Board	U11362E

Documents Related to Flash ROM Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE -Products & Packages-	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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