TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

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2M x 8 SRAM MODULE

SYS82000FK - 020/025/35

Issue 1.2 : February 2000

Description

The SYS82000FK is a plastic 16Mbit Static RAM Module housed in a JEDEC standard 36 pin Dual In-Line package organised as 2Mx8.

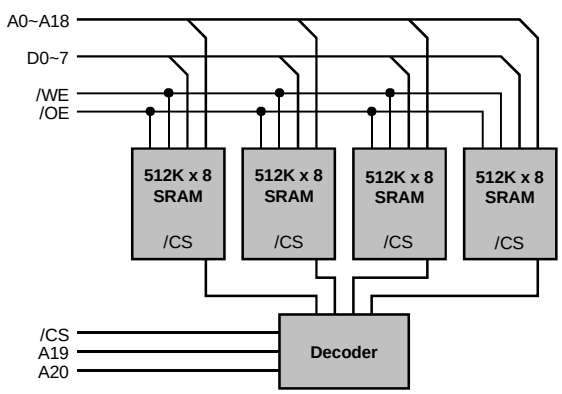
The module utilises 512Kx8 SRAM's housed in SOJ packages, and uses double sided surface mount techniques, buried decoder and dual board construction to achieve a very high density module, emulating the 16Mbit monolithic pinout.

Access times of 20 to 35 ns are available. The $\overline{OE}$ pin allows faster access times than address access during a read cycle.

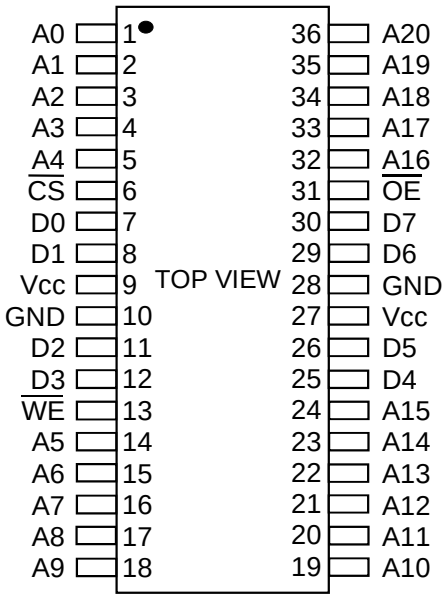
Features

- Access Times of 20/25/35 ns.
- 36 Pin JEDEC standard Dual-In-Line package.
- 5 Volt Supply ± 10%.
- Low Power Dissipation:
  Average (min cycle) 2.15W (max).
  Standby (-L Version CMOS) 220mW (max).
- Completely Static Operation.
- Low Voltage V_{CC} Data Retention.
- Equal Access and Cycle Times.
- On-board Supply Decoupling Capacitors.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 ~ A20**
Data Input/Output	**D0 ~ D7**
Chip Select	**$\overline{CS}$**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 36 Pin 0.6" Dual-In-Line Package.(DIP)

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage on any pin relative to V_{SS}	V_T (2)	-0.3	-	7.0	V
Power Dissipation	P_T	-	1.0	-	W
Storage Temperature	T_{STG}	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

Parameter		*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C

DC Electrical Characteristics (V_{CC}=5V±10%) TA 0 to 70 °C

Parameter		*Symbol*	*Test Condition*	*Min*	*Typ*	*max*	*Unit*
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-20	-	20	µA
Output Leakage Current		I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC} , $\overline{OE}$=V_{IH}	-20	-	20	µA
Operating Supply Current		I_{CC1}	Min. Cycle, $\overline{CS}$ = V_{IL},$V_{IL} \le V_{IN} \le V_{IH}$	-	-	390	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$ = V_{IH}	-	-	240	mA
	CMOS levels	I_{SB2}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2 \le V_{IN} \le V_{CC}$-0.2V	-	-	60	mA
Output Voltage		V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

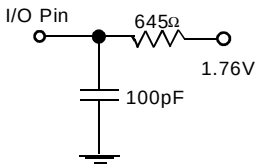
Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance (Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	V_{IN} = 0V	35	pF
Input Capacitance (other)	C_{IN2}	V_{IN} = 0V	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	47	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



Operation Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*DATA PINS*	*SUPPLY CURRENT*	*MODE*
H	X	X	High Impedance	I_{SB1} , I_{SB2}	Standby
L	L	H	Data Out	I_{CC1}	Read
L	X	L	Data In	I_{CC1}	Write
L	H	H	High-Impedance	I_{SB1} , I_{SB2}	High-Z

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1}	2.0 ≤ Vcc ≤ 5.5V,$\overline{CS}$≥Vcc-0.2	-	-	2.4	mA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ms

Notes (1) Figures are measured over the comercial Temp range.

AC OPERATING CONDITIONS

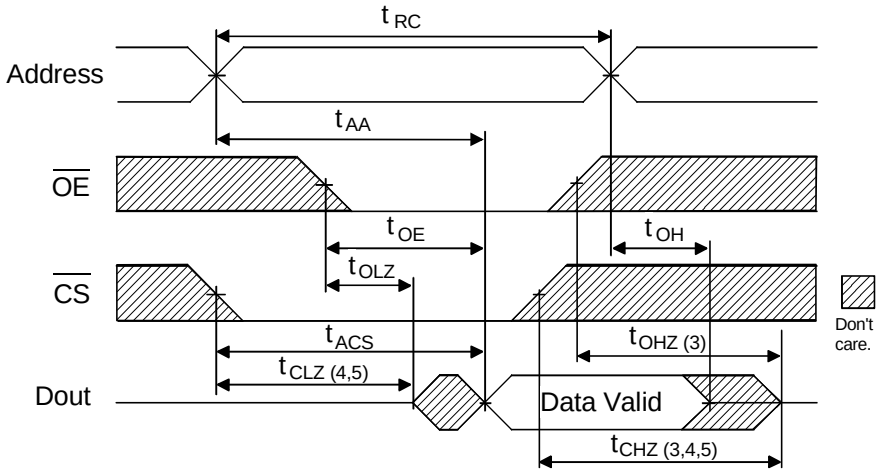
Read Cycle

		-020		-025		-035		
Parameter	Symbol	min	max	min	max	min	max	Unit
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	35	ns
Output Enable to Output Valid	t_{OE}	-	10	-	12	-	14	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	0	-	0	-	0	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	9	0	10	0	12	ns
Output Disable to Output in High Z	t_{OHZ}	0	9	0	10	0	12	ns

Write Cycle

		-20		-25		-35		
Parameter	Symbol	min	max	min	max	min	max	Unit
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns
Chip Selection to End of Write	t_{CW}	15	-	17	-	20	-	ns
Address Valid to End of Write	t_{AW}	15	-	17	-	20	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	15	-	17	-	20	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	3	-	ns
Write to Output in High Z	t_{WHZ}	0	9	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	10	-	12	-	20	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output active from End of Write	t_{OW}	3	-	5	-	5	-	ns

Read Cycle Timing Waveform (1,2)



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

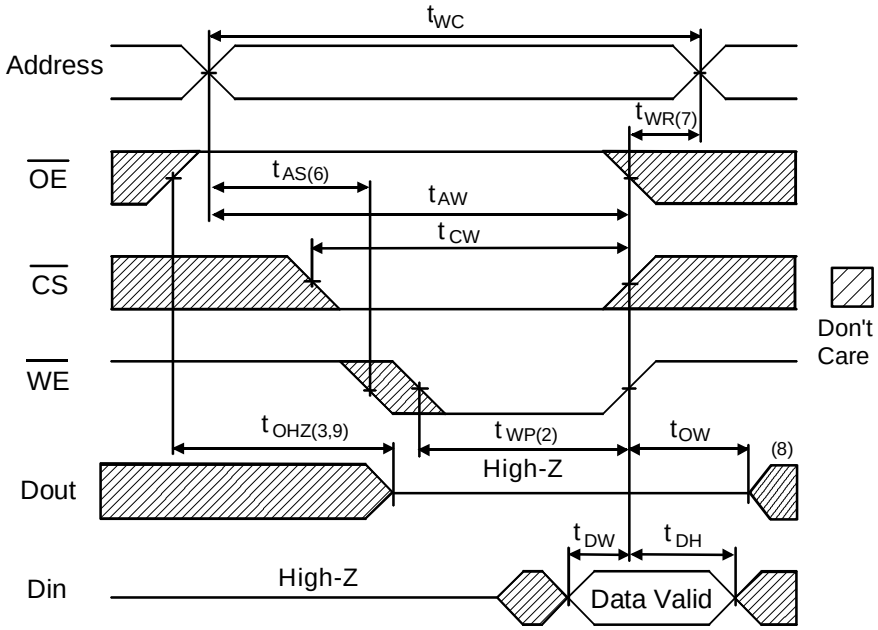
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

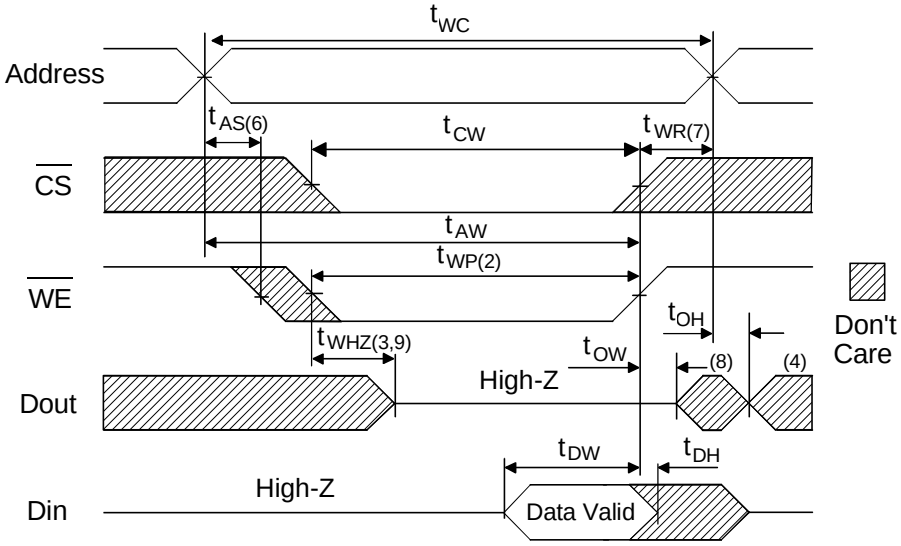
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



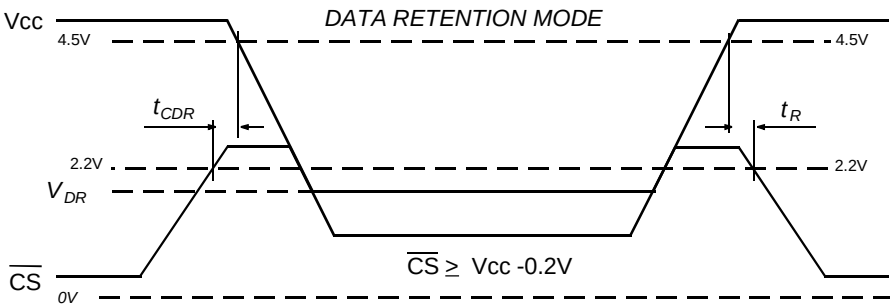
Write Cycle No.2 Timing Waveform (1,5)



AC Write Characteristics Notes

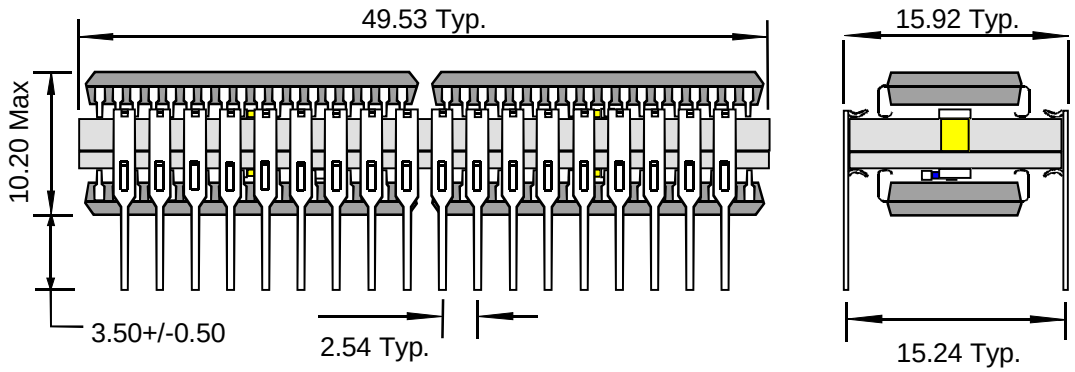
(1) All write cycle timing is referenced from the last valid address to the first transition address.
(2) All writes occur during the overlap of $\overline{CS}$ and $\overline{WE}$ low.
(3) If $\overline{OE}$, $\overline{CS}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
(4) Dout is the Read data of the new address.
(5) $\overline{OE}$ is continuously low.
(6) Address is valid prior to or coincident with $\overline{CS}$ and $\overline{WE}$ low, too avoid inadvertant writes.
(7) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
(8) When $\overline{CS}$ is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Data Retention Waveform



Package Information Dimensions in mm

Plastic 36 Pin 0.6" Dual-in-Line (DIP)



Ordering Information

SYS82000FKLI - 35

Speed	020	=	20 ns
	025	=	25 ns
	35	=	35 ns
Temperature Range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Consumption	Blank	=	Standard Part
	L	=	Low Power Part
Package	FK	=	Plastic 36 Pin 0.6" DIP
Organization	82000	=	2M x 8
Memory Type	SYS	=	Static RAM