Integrated Circuit Systems, Inc.

ICSSSTV16857C

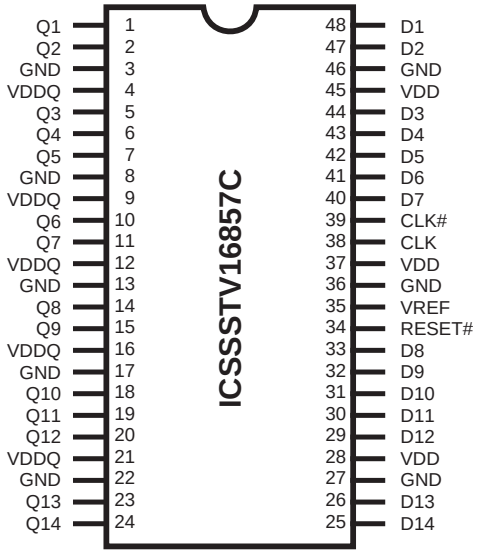
DDR 14-Bit Registered Buffer

Recommended Application:
DDR Memory Modules

Product Features:

- Differential clock signal
- Meets SSTL_2 signal data
- Supports SSTL_2 class I & II specifications
- Low-voltage operation
  VDD = 2.3V to 2.7V
- 48 pin TSSOP package

Pin Configuration



48-Pin TSSOP & TVSOP

6.10 mm. Body, 0.50 mm. pitch = TSSOP
4.40 mm. Body, 0.40 mm. pitch = TSSOP (TVSOP)

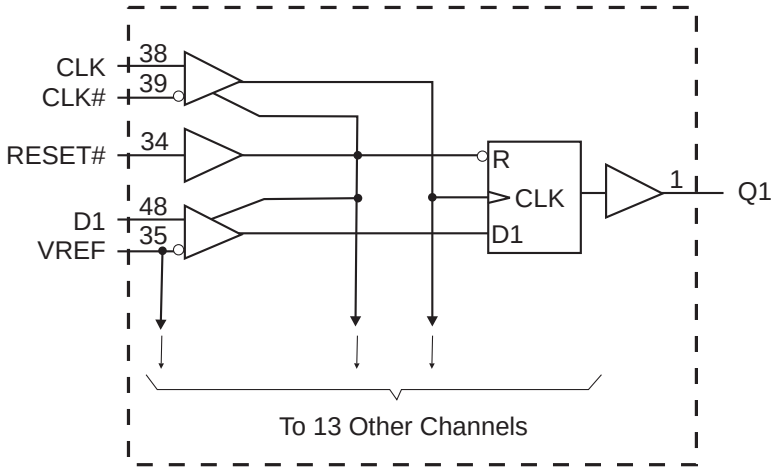
Truth Table[1]

Inputs				Q Outputs
RESET#	**CLK**	**CLK#**	**D**	**Q**
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0[(2)]

Notes:

1. H = High Signal Level
   L = Low Signal Level
   ↑ = Transition LOW-to-HIGH
   ↓ = Transition HIGH -to LOW
   X = Irrelevant
2. Output level before the indicated steady state input conditions were established.

Block Diagram



General Description

The 14-bit ICSSTV16857 is a universal bus driver designed for 2.3V to 2.7V VDD operation and SSTL_2 I/O Levels except for the RESET# input which is LVCMOS.

Data flow from D to Q is controlled by the differential clock, CLK, CLK# and RESET#. Data is triggered on the positive edge of CLK. CLK# must be used to maintain noise margins. RESET# must be supported with LVCMOS levels as VREF may not be stable during power-up. RESET# is asynchronous and is intended for power-up only and when low assures that all of the registers reset to the Low State, Q outputs are low, and all input receivers, data and clock are switched off.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
24, 23, 20, 19, 18, 15, 14, 11, 10, 7, 6, 5, 2, 1	Q (14:1)	OUTPUT	Data output
3, 8, 13, 22, 27, 36, 46	GND	PWR	Ground
4, 9, 12, 16, 21	VDDQ	PWR	Output supply voltage
25, 26, 29, 30, 31, 32, 33, 40, 41, 42, 43, 44, 47, 48	D (14:1)	INPUT	Data input
38	CLK	INPUT	Positive clock input
39	CLK#	INPUT	Negative clock input
28, 37, 45	VDD	PWR	Core supply voltage
34	RESET#	INPUT	Reset (active low)
35	VREF	INPUT	Input reference voltage

Absolute Maximum Ratings

Storage Temperature ..... –65°C to +150°C
Supply Voltage ..... -0.5 to 3.6V
Input Voltage[1] ..... -0.5 to VDD +0.5
Output Voltage[1,2] ..... -0.5 to VDDQ +0.5
Input Clamp Current ..... ±50 mA
Output Clamp Current ..... ±50mA
Continuous Output Current ..... ±50mA
VDD, VDDQ or GND Current/Pin ..... ±100mA
Package Thermal Impedance[3] ..... 55°C/W

Notes:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only whtn the output is in the high state level $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O Supply Voltage		2.3	2.5	2.7	
V_{REF}	Reference Voltage V_{REF} = 0.5X V_{DDQ}		1.15	1.25	1.35	
V_{TT}	Termination Voltage		V_{REF} -0.04	V_{REF}	V_{REF} -0.04	
V_I	Input Voltage		0		V_{DD}	
V_{IH}	DC Input High Voltage	Data Inputs	V_{REF} +0.15			
V_{IH}	AC Input High Voltage		V_{REF} +0.31			
V_{IL}	DC Input Low Voltage				V_{REF} -0.15	
V_{IL}	AC Input Low Voltage				V_{REF} -0.31	
V_{IH}	Input High Voltage Level	RESET#	1.7			
V_{IL}	Input Low Voltage Level				0.7	
V_{ICR}	Common mode Input Range	CLK, CLK#	0.97		1.53	
V_{ID}	Differential Input Voltage		0.36			
V_{IX}	Cross Point Voltage of Differential Clock Pair		(V_{DDQ}/2) -0.2		(V_{DDQ}/2) +0.2	
I_{OH}	High-Level Output Current				-20	mA
I_{OL}	Low-Level Output Current				20	
T_A	Operating Free-Air Temperature		0		70	°C

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - DC

T_A = 0 - 70º C; V_{DD} = 2.5 V +/-200mV, V_{DDQ}=2.5V 200mV; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS		VDD	MIN	TYP	MAX	UNITS
V_{IK}		I_I = -18mA		2.3V			-1.2	
V_{OH}		I_{OH} = -100µA		2.3V-2.7	VDD -0.2			
		I_{OH}= -16mA		2.3V	1.95			
V_{OL}		I_{OL} = 100µA		2.3-2.7V			0.2	V
		I_{OL} = 16mA		2.3V			0.35	
I_I	All Inputs	$V_I = V_{DD}$ or GND		2.7V			±5	µA
I_{DD}	Standby (Static)	RESET# = GND	IO = 0	2.7V			0.01	µA
	Operating (Static)	$V_I = V_{IH\ (AC\#)}$ or $V_{IL\ (AC)}$, RESET# = V_{DD}					55	mA
I_{DDD}	Dynamic operating clock only	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL\ (AC)}$, CK and CK# switching 50% duty cycle.					75	µA/clock MHz
	Dynamic Operating per each data input	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL\ (AC)}$, CK and CK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle					15	µA/ clock MHz/data
r_{OH}	Output High	I_{OH} = -20mA		2.3-2.7V	7		20	W
r_{OL}	Output Low	I_{OL} = 20mA		2.3-2.7V	7		20	W
$r_{O(D)}$	[r_{OH} - r_{OL}] each separate bit	I_O = 20mA, T_A = 25° C		2.5V			4	W
	Data Inputs	$V_I = V_{REF}$ ±310mV			2.5		3.5	
C_i	CK and CK#	V_{ICR} = 1.25V, $V_{I(PP)}$ = 360mV		2.5V	2.5		3.5	pF

Notes:

1 - Guaranteed by design, not 100% tested in production.

Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS		VDD=2.5±0.2V			UNITS
			MIN	TYP	MAX	
f_{clock}	Clock frequency			133	200	MHz
t_{PD}	Clock to output time		1.6	2	2.6	ns
t_{RST}	Reset to output time		2.5	2.7	3.3	ns
t_{SL}	Output slew rate		1	1.5	4	V/ns
t_{SU}	Setup time, fast slew rate [2, 4]	Data before CK↑ , CK#↓	0.75	0.018		ns
	Setup time, slow slew rate [3, 4]		0.9			ns
T_h	Hold time, fast slew rate [2,4]	Data after CK↑ , CK#↓	0.75	0.145		ns
	Hold time, slow slew rate [3, 4]		0.9			ns

Notes: 1 - Guaranteed by design, not 100% tested in production.

2 - For data signal input slew rate ?1V/ns.

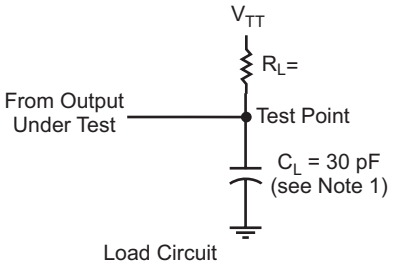
4 - CLK, CLK# signals input slew rates are ?1V/ns.

3 - For data signal input slew rate ?0.5V/ns and < 1V/ns.

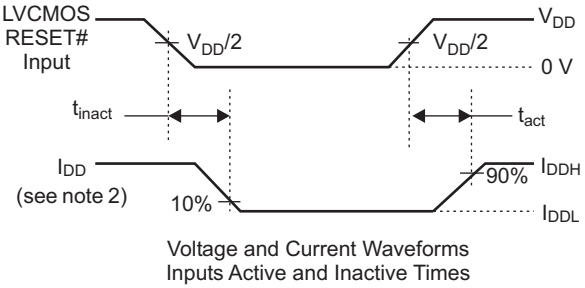
Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

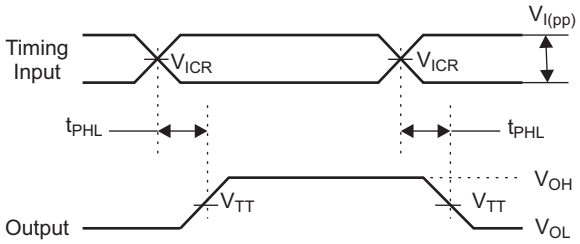
SYMBOL	From (Input)	To (Output)	VDD=2.5±0.2V			UNITS
			MIN	TYP	MAX	
f_{clock}				133	200	MHz
t_{PD}	CLK, CLK#	Q	1.6	2	2.6	ns
t_{ph1}	RESET	Q	2.5	2.7	3.3	ns



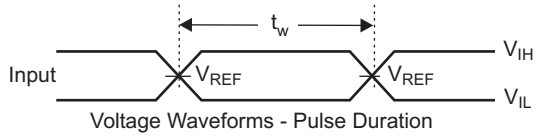
Load Circuit



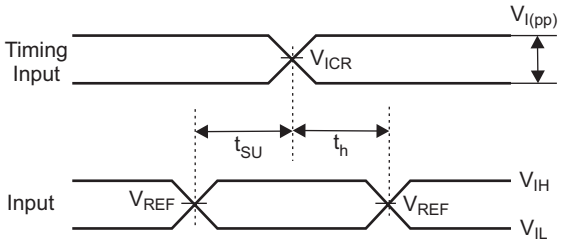
Voltage and Current Waveforms
Inputs Active and Inactive Times



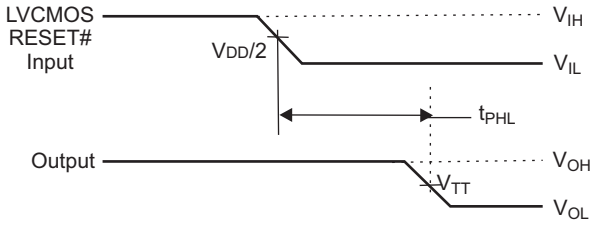
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



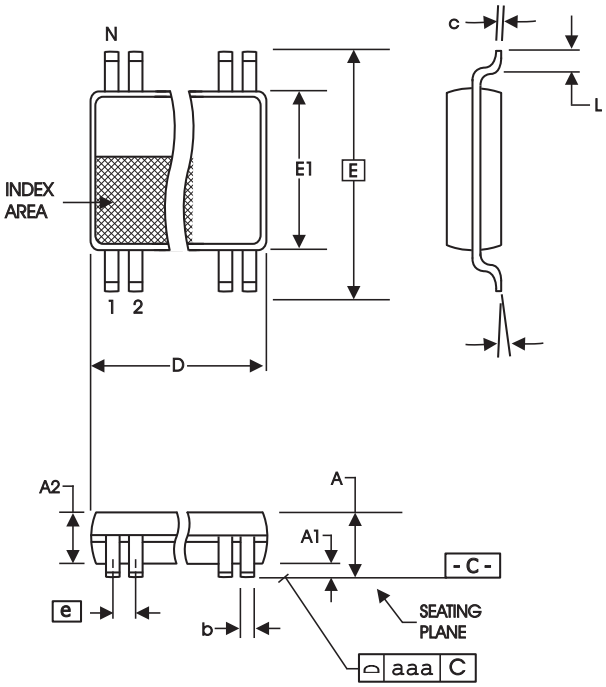
Voltage Waveforms - Setup and Hold Times



Voltage Waveforms - Propagation Delay Times

Parameter Measurement Information (V_{DD} = 2.5V ±0.2V)

Notes: 1. CL incluces probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA.
3. All input pulses are supplied by generators having the following chareacteristics: PRR ≤10 MHz, Zo=50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. V_{TT} = V_{REF} = V_{DDQ}/2
6. V_{IH} = V_{REF} + 310mV (ac voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.
7. V_{IL} = V_{REF} -310mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. t_{PLH} and t_{PHL} are the same as t_{pd}



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

'ARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

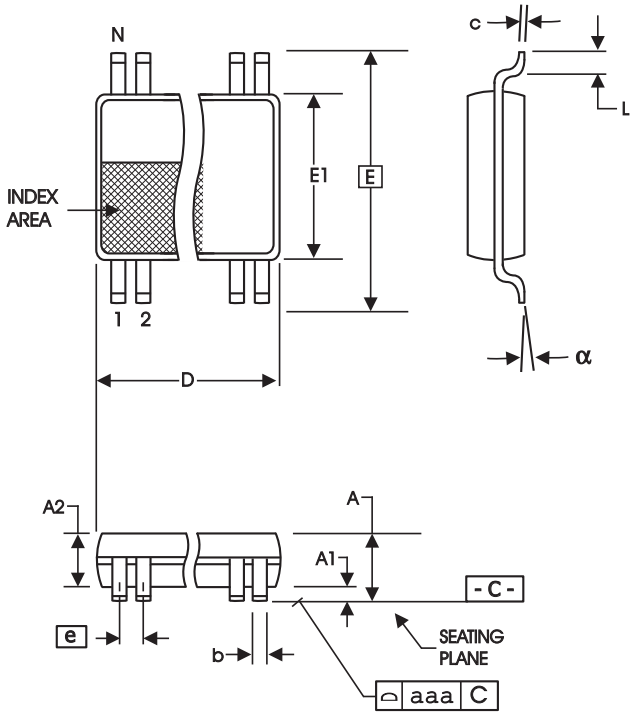
Ordering Information

ICSSSTV16857CyG-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.13	0.23	.005	.009
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.40 BASIC		0.016 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.08	--	.003

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0037

4.40 mm. Body, 0.40 mm. pitch TSSOP

(173 mil) (16 mil)

Ordering Information

ICSSSTV16857CyL-T

Example:

ICS XXXX y L - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  L=TSSOP (TVSOP)
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device