CAT34C02

2-Kb I²C EEPROM for DDR2 DIMM Serial Presence Detect

FEATURES

- **Supports Standard and Fast I²C Protocol**
- **1.7 V to 5.5 V Supply Voltage Range**
- **16-Byte Page Write Buffer**
- **Hardware Write Protection for entire memory**
- **Software Write Protection for lower 128 Bytes**
- **Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA).**
- **Low power CMOS technology**
- **1,000,000 program/erase cycles**
- **100 year data retention**
- **RoHS-compliant packages**
- **Industrial temperature range**

For Ordering Information details, see page 14.

DEVICE DESCRIPTION

The CAT34C02 is a 2-Kb Serial CMOS EEPROM, internally organized as 16 pages of 16 bytes each, for a total of 256 bytes of 8 bits each.

It features a 16-byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

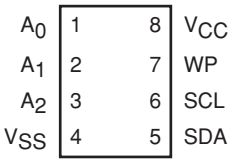
Write operations can be inhibited by taking the WP pin High (this protects the entire memory) or by setting an internal Write Protect flag via Software command (this protects the lower half of the memory).

In addition to Permanent Software Write Protection, the CAT34C02 also features JEDEC compatible Reversible Software Write Protection for DDR2 Serial Presence Detect (SPD) applications operating over the 1.7 V to 3.6 V supply voltage range.

The CAT34C02 is fully backwards compatible with earlier DDR1 SPD applications operating over the 1.7 V to 5.5 V supply voltage range.

PIN CONFIGURATION

TSSOP (Y)
TDFN (VP2)

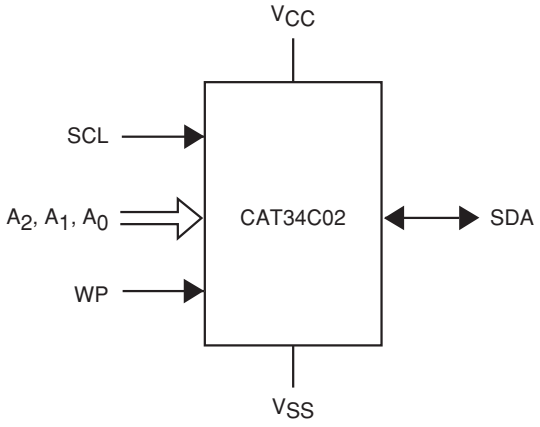


For the location of Pin 1, please consult the corresponding package drawing.

PIN FUNCTIONS

A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground

FUNCTIONAL SYMBOL



* Catalyst carries the I²C protocol under a license from the Philips Corporation.

Doc. No. 1095, Rev. I

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground(1)	-0.5 V to +6.5 V

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS(2)

Symbol	Parameter	Min	Units
N_{END}(*)	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

(*) Page Mode, V_{CC} = 5 V, 25°C

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.7 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Supply Current	Read or Write at 400 kHz		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		2	µA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		2	µA
V_{IL}	Input Low Voltage		-0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} > 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} > 1.7 V, I_{OL} = 1.0 mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

T_A = 25°C, f = 400 kHz, V_{CC} = 5 V

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN}(2)	SDA I/O Pin Capacitance	V_{IN} = 0 V		8	pF
C_{IN}(2)	Input Capacitance (other pins)	V_{IN} = 0 V		6	pF
Z_{WPL}	WP Input Low Impedance	V_{IN} < 0.5 V	5	70	kΩ
I_{LWPH}	WP Input High Leakage	V_{IN} > V_{CC} x 0.7		2	µA

Note:

(1) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

A.C. CHARACTERISTICS(1)

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C.

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		µs
$t_{HD:DAT}$	Data Hold Time	0		0		µs
$t_{SU:DAT}$	Data Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F(2)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		µs
t_{AA}	SCL Low to SDA Data Out		3.5		0.9	µs
t_{DH}	Data Out Hold Time	100		100		ns
T_i(2)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		µs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		µs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU}(2, 3)	Power-up to Ready Mode		1		1	ms

Note:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this paramete.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

A.C. TEST CONDITIONS

Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Times	< = 50 ns
Input Reference Levels	$0.3V_{CC}$, $0.7V_{CC}$
Output Reference Levels	$0.5V_{CC}$
Output Load	Current Source: I_{OL} = 3mA; C_L = 100pF

POWER-ON RESET (POR)

The CAT34C02 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The CAT34C02 will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address pins accept the device address. These pins have on-chip pull-down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on-chip pull-down resistor.

FUNCTIONAL DESCRIPTION

The CAT34C02 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT34C02 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

I^2C BUS PROTOCOL

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 1).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 2). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 3). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 4.

Figure 1. Start/Stop Timing

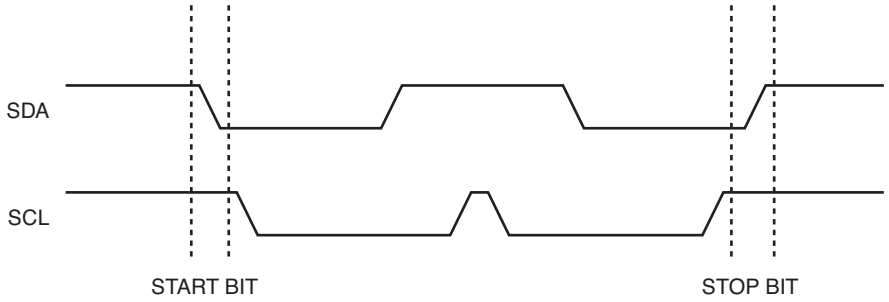


Figure 2. Slave Address Bits

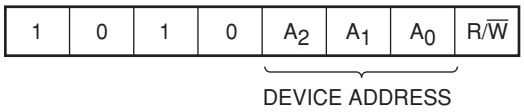


Figure 3. Acknowledge Timing

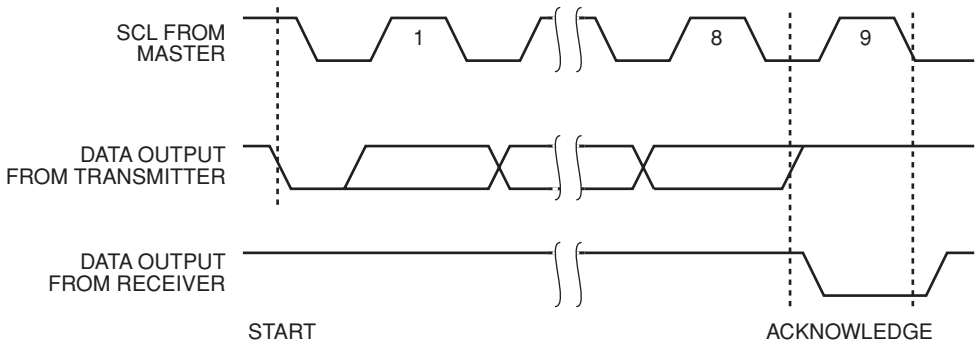
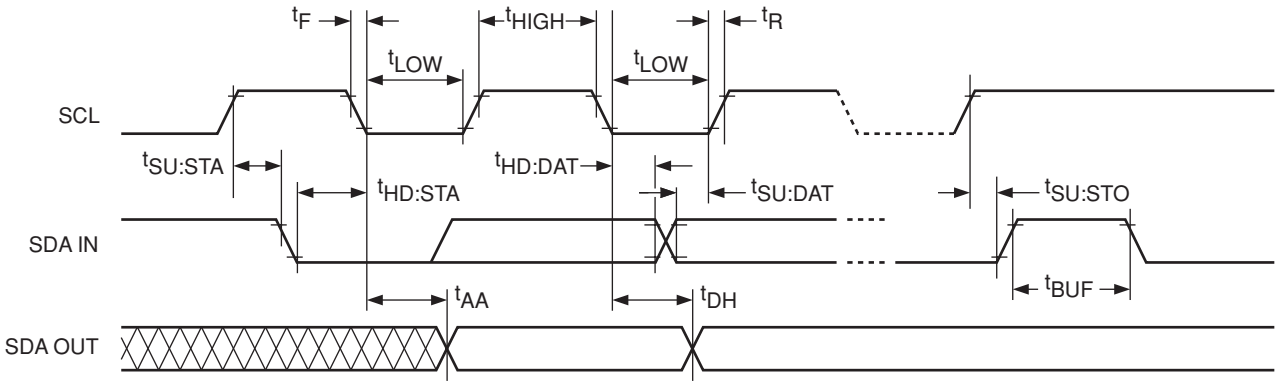


Figure 4. Bus Timing



WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, byte address and data to be written (Figure 5). The Slave acknowledges all 3 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 6). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT34C02 contains 256 bytes of data, arranged in 16 pages of 16 bytes each. A page is selected by the 4 most significant bits of the address byte following the Slave address, while the 4 least significant bits point to the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 7).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap-around' fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34C02 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a 'Selective Read' command (see READ OPERATIONS).

The CAT34C02 will not acknowledge the Slave address, as long as internal Write is in progress.

DELIVERY STATE

The CAT34C02 is shipped 'unprotected', i.e. neither SWP flag is set. The entire 2-Kb memory is erased, i.e. all bytes are FFh.

Figure 5. Byte Write Timing

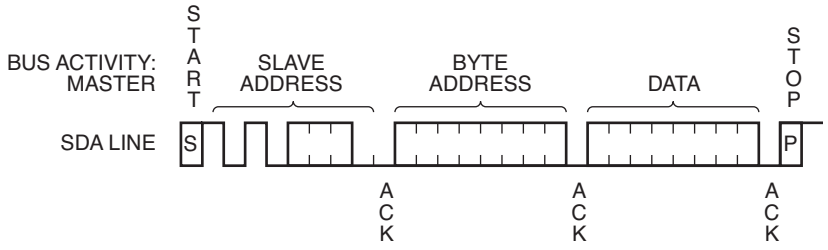


Figure 6. Write Cycle Timing

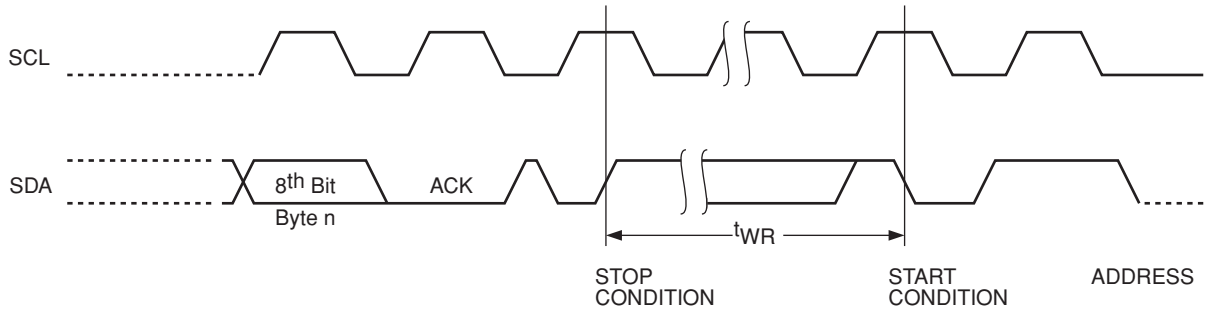
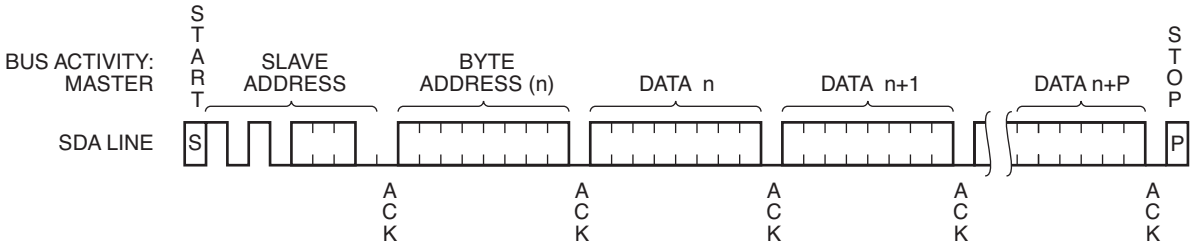
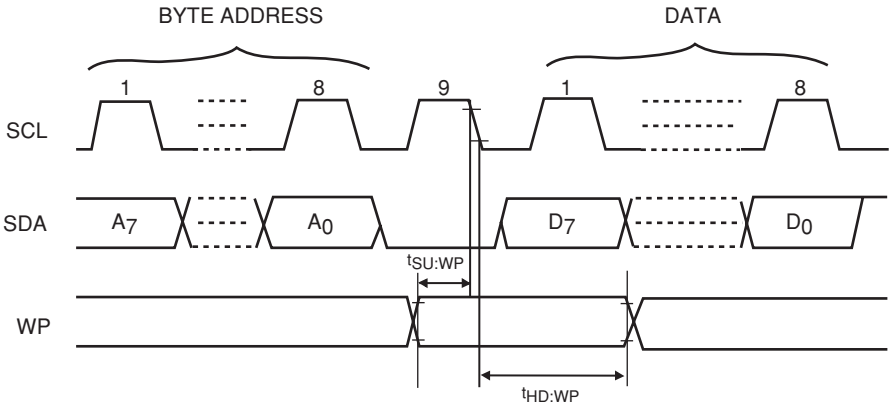


Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

Figure 8. WP Timing



READ OPERATIONS

Immediate Address Read

In standby mode, the CAT34C02 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that 'previous' byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT34C02 is presented with a Slave address containing a '1' in the R/$\overline{W}$ bit position (Figure 9), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a 'dummy' Write operation (Figure 10). Here the START is followed by the Slave address (with the R/$\overline{W}$ bit set to '0') and the desired byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT34C02, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 11). If the end of memory is reached during sequential Read, then the address counter will 'wrap-around' to the beginning of memory, etc. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

Figure 9. Immediate Address Read Timing

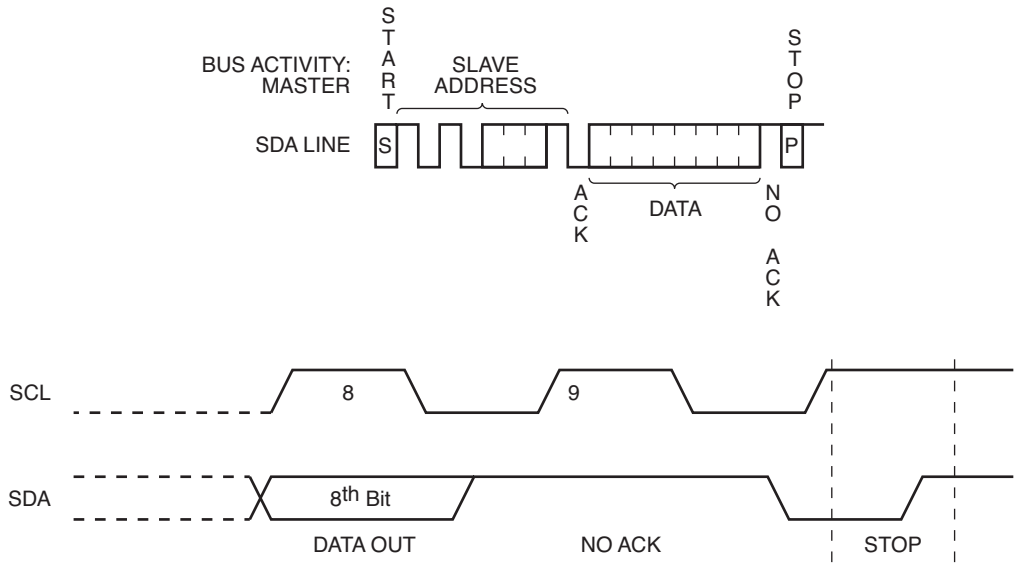


Figure 10. Selective Read Timing

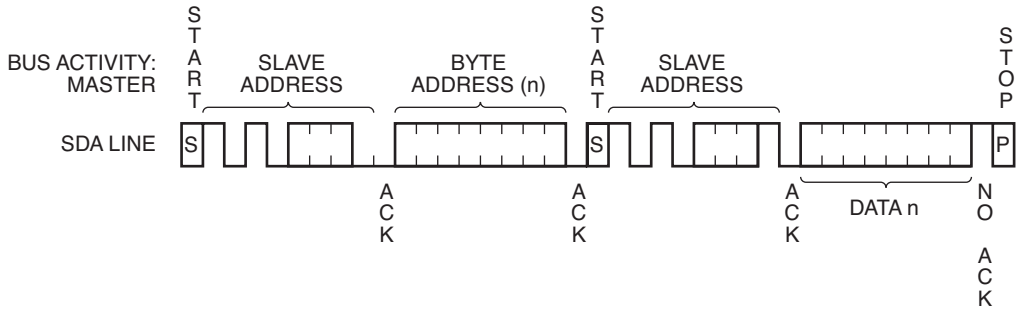
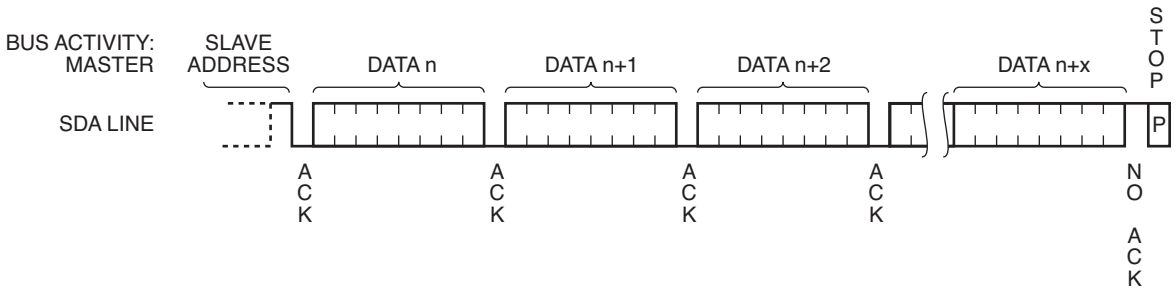


Figure 11. Sequential Read Timing



SOFTWARE WRITE PROTECTION

The lower half of memory (first 128 bytes) can be protected against Write requests by setting one of two Software Write Protection (SWP) flags.

The Permanent Software Write Protection (PSWP) flag can be set or read while all address pins are at regular CMOS levels (GND or V_{CC}), whereas the very high voltage V_{HV} must be present on address pin A_0 to set, clear or read the Reversible Software Write Protection (**RSWP**) flag. The D.C. OPERATING CONDITIONS for RSWP operations are shown in Table 1.

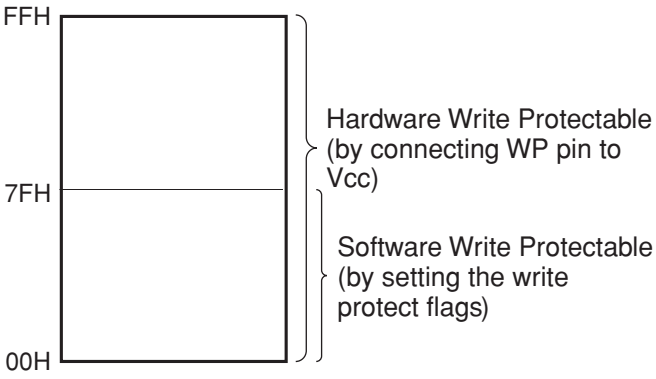
The SWP commands are listed in Table 2. All commands are preceded by a START and terminated with a STOP, following the ACK or NoACK from the CAT34C02. All SWP related Slave addresses use the pre-amble: 0110 (6h), instead of the regular 1010 (Ah) used for memory access. For **PSWP** commands, the three address pins can be at any logic level, whereas for **RSWP** commands the address pins must be at pre-assigned logic levels. V_{HV} is interpreted as logic '1'. The V_{HV} condition must be established on pin A_0 before the START and maintained just beyond the STOP. Otherwise an RSWP request could be interpreted by the CAT34C02 as a PSWP request.

The SWP Slave addresses follow the standard I^2C convention, i.e. to read the state of the SWP flag, the LSB of the Slave address must be '1', and to set or clear a flag, it must be '0'. For Write commands a dummy byte address and dummy data byte must be provided (Figure 12). In contrast to a regular memory Read, a SWP Read does not return Data. Instead the CAT34C02 will respond with NoACK if the flag is set and with ACK if the flag is not set. Therefore, the Master can immediately follow up with a STOP, as there is no meaningful data following the ACK interval (Figure 13).

HARDWARE WRITE PROTECTION

With the WP pin held HIGH, the entire memory, as well as the SWP flags are protected against Write operations, see Memory Protection Map below. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT34C02.

The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 8). If the WP pin is HIGH during the strobe interval, the CAT34C02 will not acknowledge the data byte and the Write request will be rejected.



Memory Protection Map

TABLE 1: RSWP D.C. OPERATING CONDITIONS(1)

Symbol	Parameter	Test Conditions	Min	Max	Units
ΔV_{HV}	A_0 Overdrive (V_{HV} - V_{CC})	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V
I_{HV}	A_0 Input Current @ V_{HV}			1	mA

(1) To prevent damaging the CAT34C02 while applying V_{HV}, it is strongly recommended to limit the power delivered to pin A_0, by inserting a series resistor (> 1.5 kΩ) between the supply and the input pin. The resistance is only limited by the combination of V_{HV} and maximum I_{HVD}. While the resistor can be omitted if V_{HV} is clamped well below 10 V, it nevertheless provides simple protection against EOS events. As an example: V_{CC} = 1.7 V, V_{HV} = 8 V, 1.5 kΩ < R_S < 15 kΩ.

Table 2. SWP Commands

Action	Control Pin Levels (1)				Flag State (2)		Slave Address					ACK ?	Address Byte	ACK ?	Data Byte	ACK ?	Write Cycle
	WP	A_2	A_1	A_0	PSWP	RSWP	b_7 to b_4	b_3	b_2	b_1	b_0						
Set PSWP	X	A_2	A_1	A_0	1	X	0110	A_2	A_1	A_0	X	No					
	GND	A_2	A_1	A_0	0	X		A_2	A_1	A_0	0	Yes	X	Yes	X	Yes	Yes
	V_{CC}	A_2	A_1	A_0	0	X		A_2	A_1	A_0	0	Yes	X	Yes	X	No	No
	X	A_2	A_1	A_0	0	X		A_2	A_1	A_0	1	Yes					
Set RSWP	X	GND	GND	V_{HV}	1	X		0	0	1	X	No					
	X	GND	GND	V_{HV}	0	1		0	0	1	X	No					
	GND	GND	GND	V_{HV}	0	0		0	0	1	0	Yes	X	Yes	X	Yes	Yes
	V_{CC}	GND	GND	V_{HV}	0	0		0	0	1	0	Yes	X	Yes	X	No	No
	X	GND	GND	V_{HV}	0	0		0	0	1	1	Yes					
Clear RSWP	X	GND	V_{CC}	V_{HV}	1	X		0	1	1	X	No					
	GND	GND	V_{CC}	V_{HV}	0	X		0	1	1	0	Yes	X	Yes	X	Yes	Yes
	V_{CC}	GND	V_{CC}	V_{HV}	0	X		0	1	1	0	Yes	X	Yes	X	No	No
	X	GND	V_{CC}	V_{HV}	0	X		0	1	1	1	Yes					

Note:
(1) Here A_2, A_1 and A_0 are either at V_{CC} or GND.
(2) 1 stands for 'Set', 0 stands for 'Not Set', X stands for 'don't care'.

Figure 12. Software Write Protect (Write)

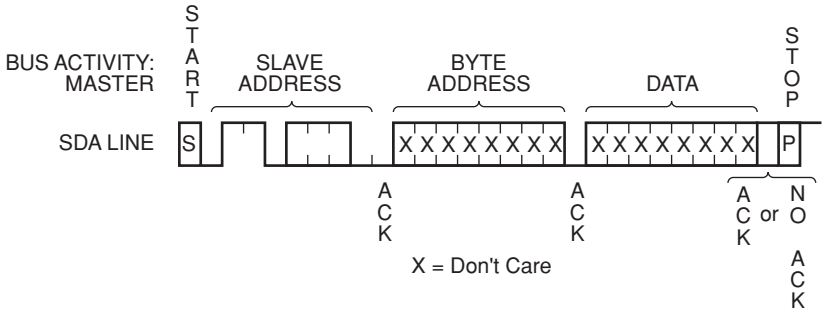
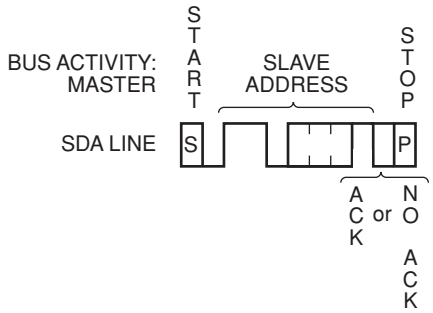
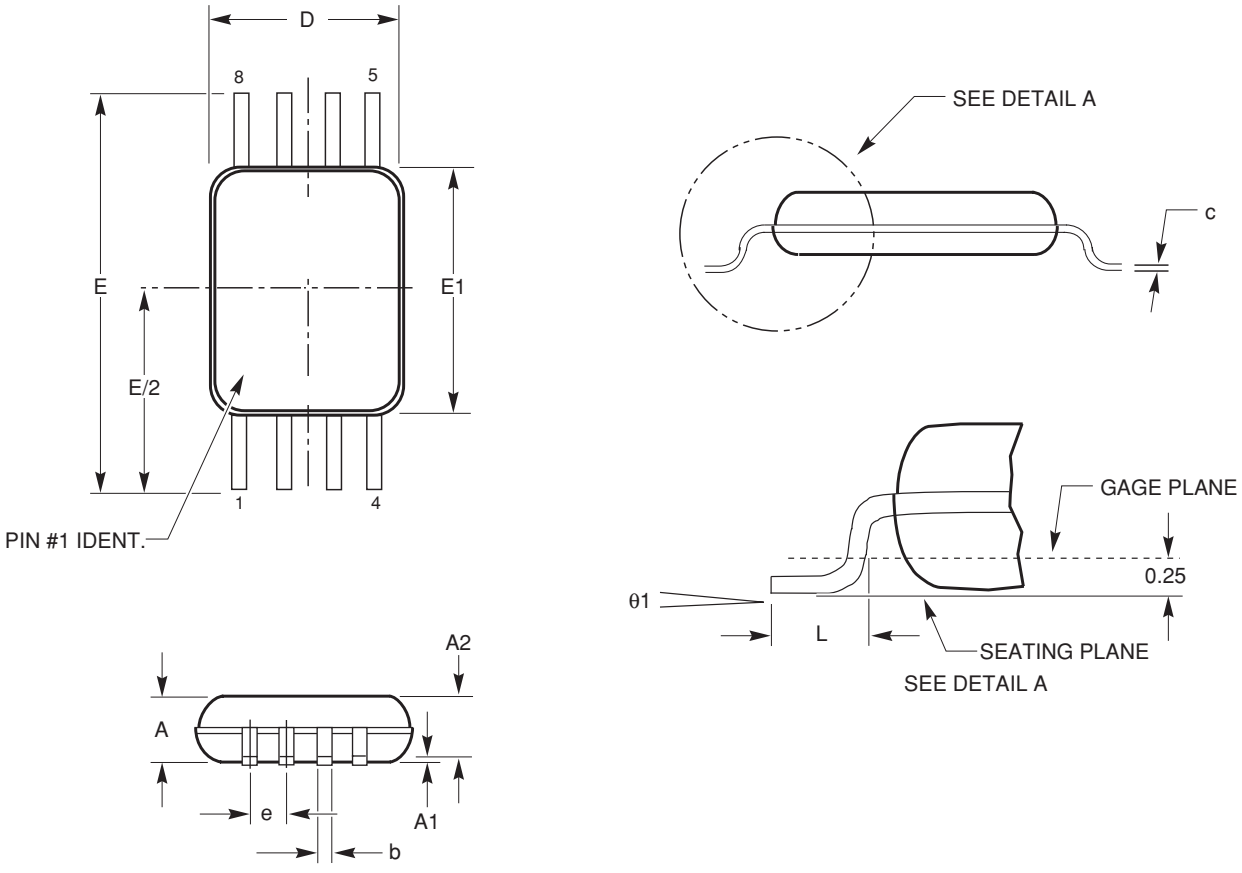


Figure 13. Software Write Protect (Read)



PACKAGE DIMENSIONS

8-LEAD TSSOP (Y)



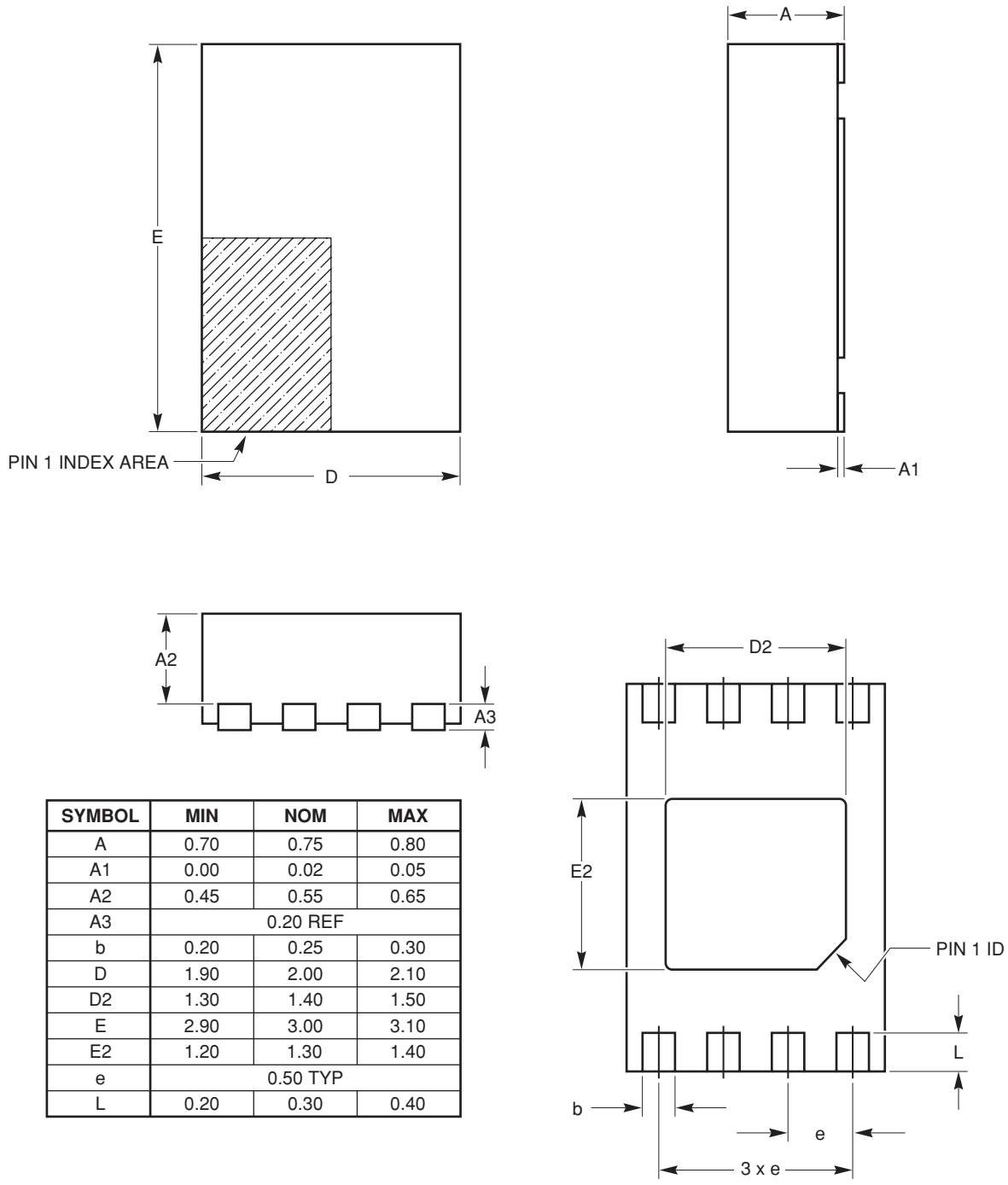
SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.4	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.75
θ1	0.00		8.00

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-153.

8-PAD TDFN 2X3 PACKAGE (VP2)



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40

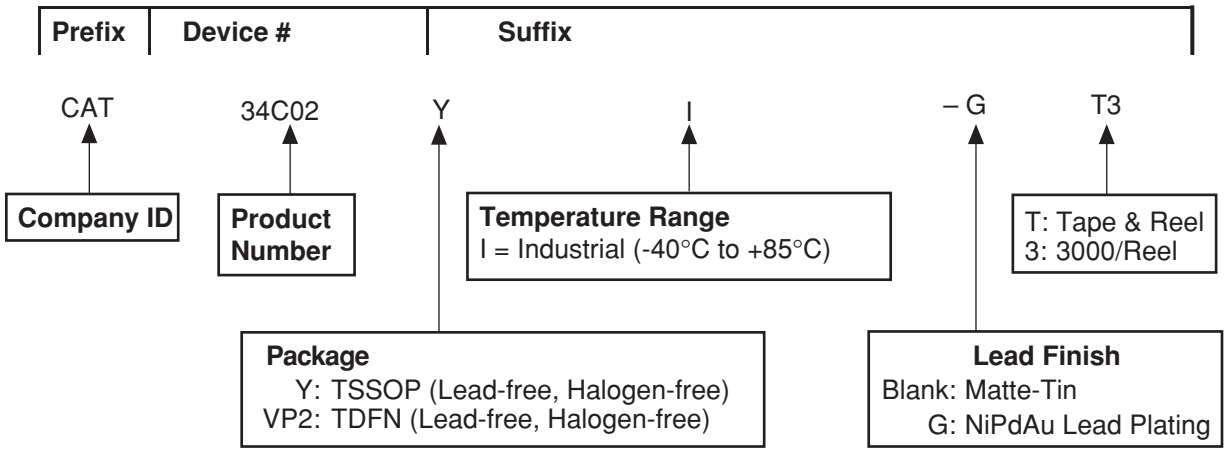
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

TDFN2X3 (03).eps

Notes:

1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-229.

ORDERING INFORMATION



Notes:

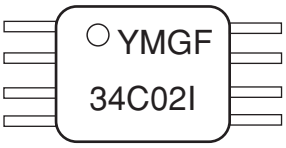
((1) All packages are RoHS-compliant (Lead-free, Halogen-free)

(2) The device used in the above example is a CAT34C02YI-GT3 (TSSOP, Industrial Temperature, NiPdAu, Tape & Reel)

(3) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

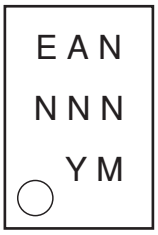
PACKAGE MARKING

8-Lead TSSOP



Y = Production Year
M = Production Month
G = Die Revision
34C02 = Device Code
I = Temperature Range
F = Lead Finish
4 = NiPdAu
3 = Matte-Tin

8-Lead TDFN



E A = Device Code (NiPdAu)
E V = Device Code (Matte-Tin)
N = Traceability Code
Y = Production Year
M = Production Month

Notes:

(1) The circle on the package marking indicates the location of Pin 1.

REVISION HISTORY

Date	Revision	Comments
09/27/05	A	Initial Issue
09/28/05	B	Update Features Update Absolute Maximum Ratings Update D.C. Operating Characteristics Update Pin Impedance Characteristics Update A.C. Characteristics Update I^2C Bus Protocol - Power-On Reset (POR)
10/03/05	C	Update Power-On Reset (POR)
11/05/05	D	Update Ordering Information Add Tape and Reel Specifications
12/07/05	E	Update D.C. Operating Characteristics Update Pin Impedance Characteristics
12/21/05	F	Update D.C. Operating Characteristics
05/18/06	G	Update Ordering Information
05/22/06	H	Update Pin Functions Update D.C. Operating Characteristics Update A.C. Characteristics Add A.C. Test Conditions Update Figure 3 and 4 Update Software Write Protection Update Delivery State Add Table 1: RSWP D.C. Operating Conditions Update Package Marking
07/19/06	I	Add link to Tape and Reel Update Package Dimensions Update Package Marking

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Publication #: 1095
Revison: I
Issue date: 07/19/06