Z~Communications, Inc.
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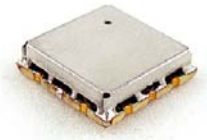
TEL: (858) 621-2700 | FAX: (858) 486-1927

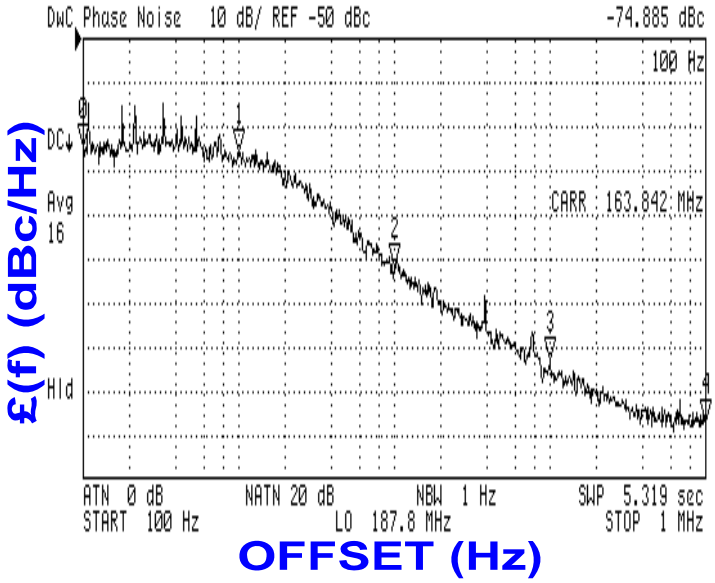
PCA0163A-LF

PHASE LOCKED LOOP

Rev A1



PHASE NOISE (1 Hz BW, typical)



FEATURES

- Frequency Range: 163.84 - 163.84 MHz
- Step Size: 80 KHz
- CPLL - Style Package

APPLICATIONS

- Telecommunications
- Satellite
- Telemetry

PERFORMANCE SPECIFICATIONS	VALUE	UNITS
Frequency Range	163.84 - 163.84	MHz
Phase Noise @ 10 kHz offset (1 Hz BW, typ.)	-102	dBc/Hz
Harmonic Suppression (2nd, typ.)	-10	dBc
Sideband Spurs (typ.)	-70	dBc
Power Output	0±3	dBm
Load Impedance	50	Ω
Step Size	80	kHz
Charge Pump Output Current	1250	µA
Switching Speed (typ., adjacent channel)	3	mSec
Startup Lock Time (typ.)	5	mSec
Operating Temperature Range	-40 to 85	°C
Package Style	CPLL	
POWER SUPPLY REQUIREMENTS		
Supply Voltage (Vcc, nom.)	3	Vdc
Supply Current (Icc, typ.)	21	mA

All specifications are typical unless otherwise noted and subject to change without notice.

APPLICATION NOTES

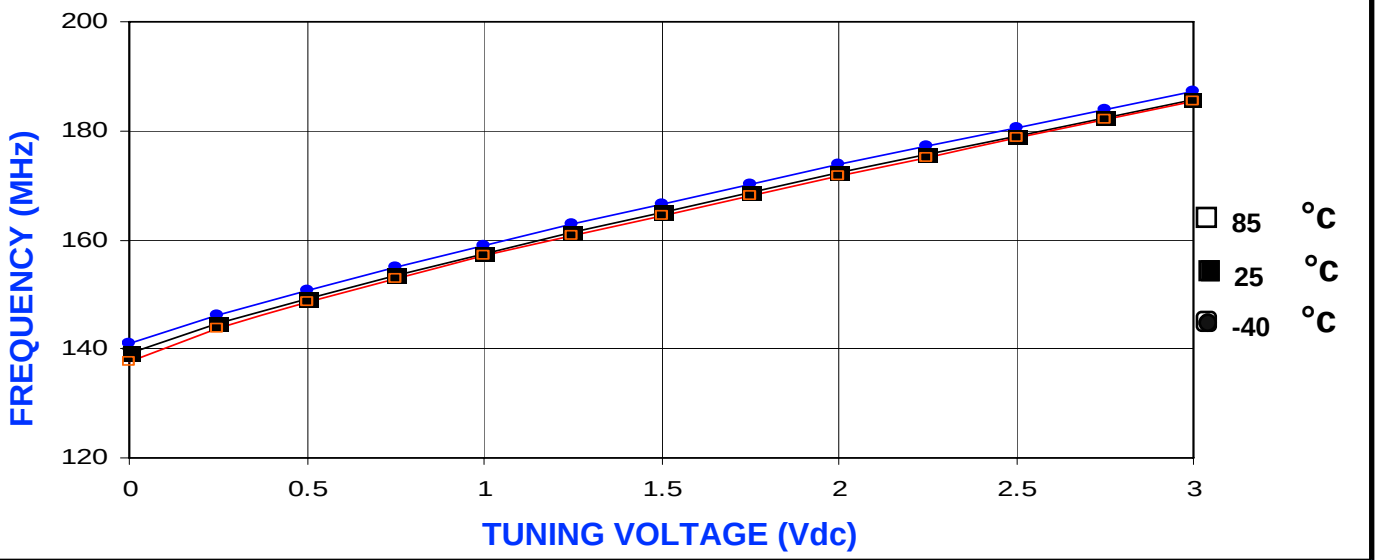
- AN-107 : How to Solder Z-COMM VCOs / PLLs
- AN-202 : PLL Functional Description

NOTES:

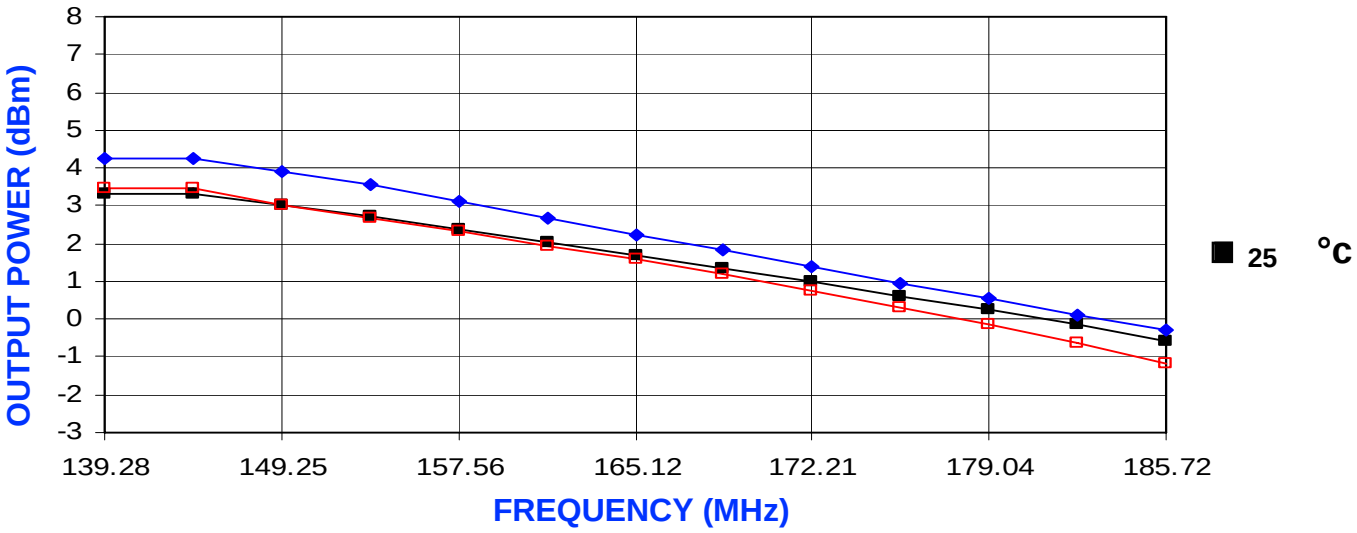
Reference Oscillator Signal: 5 MHz<f_{osc}<100 MHz

Frequency Synthesizer: Analog Devices - ADF4001

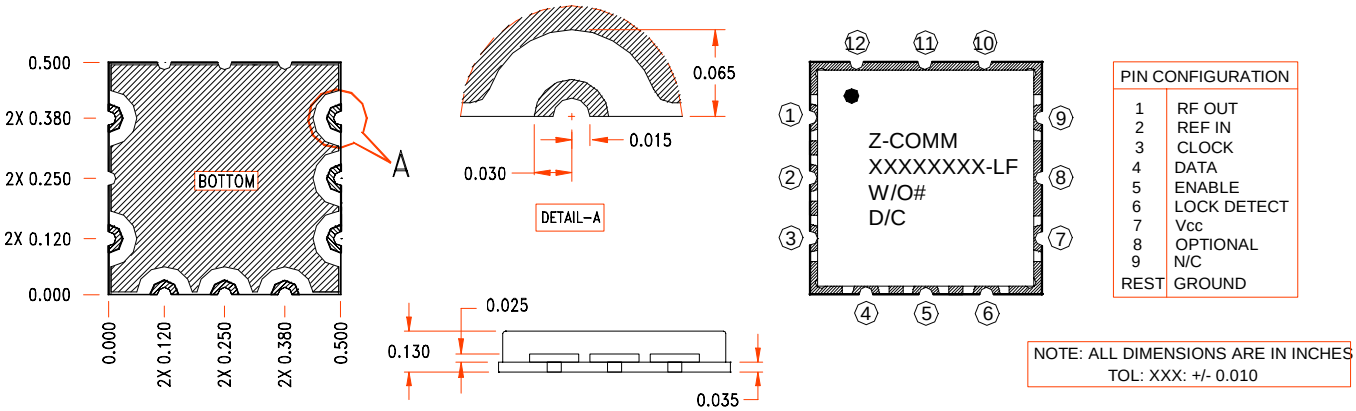
VCO TUNING CURVE, typ.



VCO POWER CURVE, typ.



PHYSICAL DIMENSIONS



PIN CONFIGURATION	
1	RF OUT
2	REF IN
3	CLOCK
4	DATA
5	ENABLE
6	LOCK DETECT
7	Vcc
8	OPTIONAL
9	N/C
REST	GROUND

NOTE: ALL DIMENSIONS ARE IN INCHES
TOL: XXX: +/- 0.010