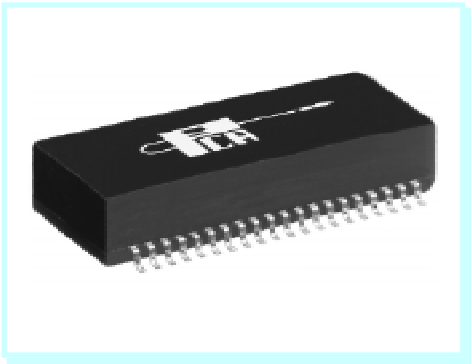
10/100 Base-X Module for QSI 6611/6612 Multi-Port Applications

EPF8050S



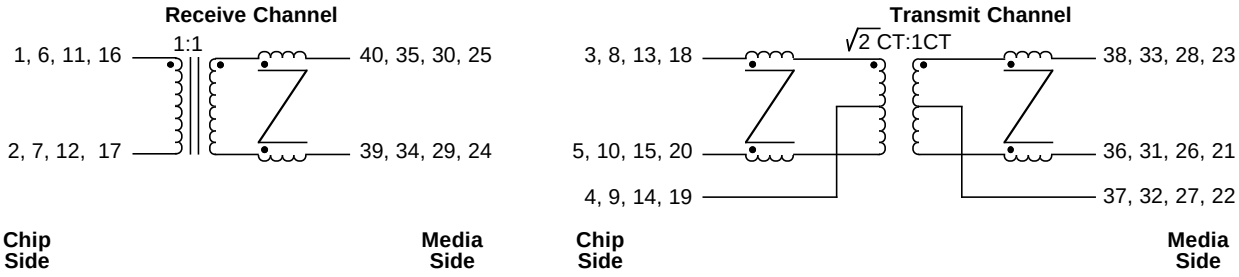
- Also recommended for Broadcom BCM5208 10/100 Solution
- Significantly improved common mode attenuation
- Guaranteed to operate with 8 mA DC bias at 70°C
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards

Electrical Parameters @ 25° C

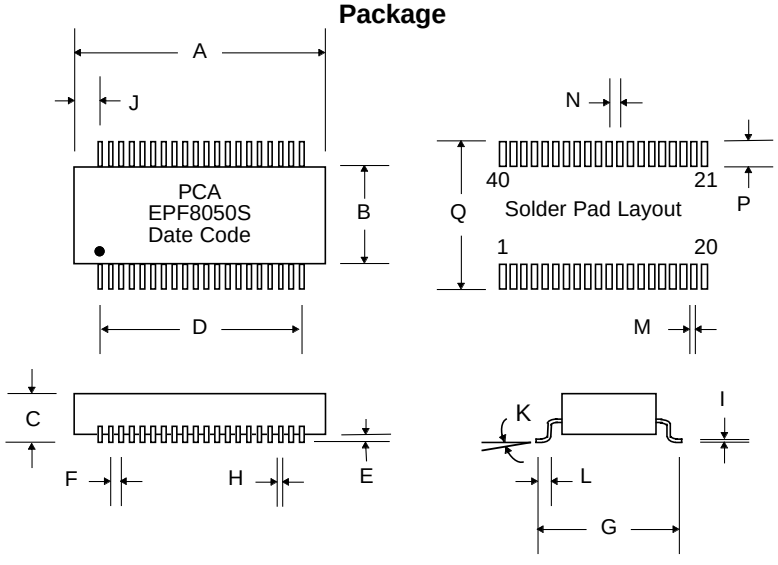
OCL @ 70°C	Insertion Loss (dB Max.)						Return Loss (dB Min.)								Common Mode Rejection (dB Min.)								Crosstalk (dB Min.)
100 KHz, 0.1 Vrms 8 mA DC Bias	0.1-80 MHz		80-100 MHz		150 MHz		1-10 MHz		20-30 MHz		40-60 MHz		70-100 MHz		30-100 MHz		200 MHz		300 MHz		500 MHz		0.1-100 MHz
Media Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	
350µH	-1	-1	-1	-1	-3	-3	-18	-18	-14	-18	-10	-18	-8	-10	-30	-25	-25	-20	-20	-10	-15	---	-30

- **Isolation** : 1500 Vrms • **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max.

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	1.110	1.130		28.19	28.70	
B	.470	.490		11.94	12.45	
C	.235	.255		5.97	6.48	
D	.950	Typ.		24.13	Typ.	
E	.008	.012		.203	.305	
F	.050	Typ.		1.27	Typ.	
G	.620	.630		15.75..	16.00	
H	.016	.022		406	.559	
I	.008	.012		.203	.305	
J	.085	Typ.		2.16	Typ.	
K	0°	8°		0°	8°	
L	.045	Typ.		1.14	Typ.	
M			.030			.762
N			.050			1.27
P			.090			2.29
Q			.670			17.02

PCA ELECTRONICS, INC.
16799 SCHOENBORN ST.
NORTH HILLS, CA 91343

CSF8050Sa Rev. Orig. 3/6/97

TEL: (818) 892-0761
FAX: (818) 894-5791
http://www.pca.com

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EPF8050S

The circuit below is a guideline for interconnecting PCA's EPF8050S with QSI6611 and QSI6612 chip set for 10.100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the chips supporting resistor to get at least 2.12V pk-pk across the transmit pins.

It is recommended that system designers do not use the receiver side center tap to ground, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

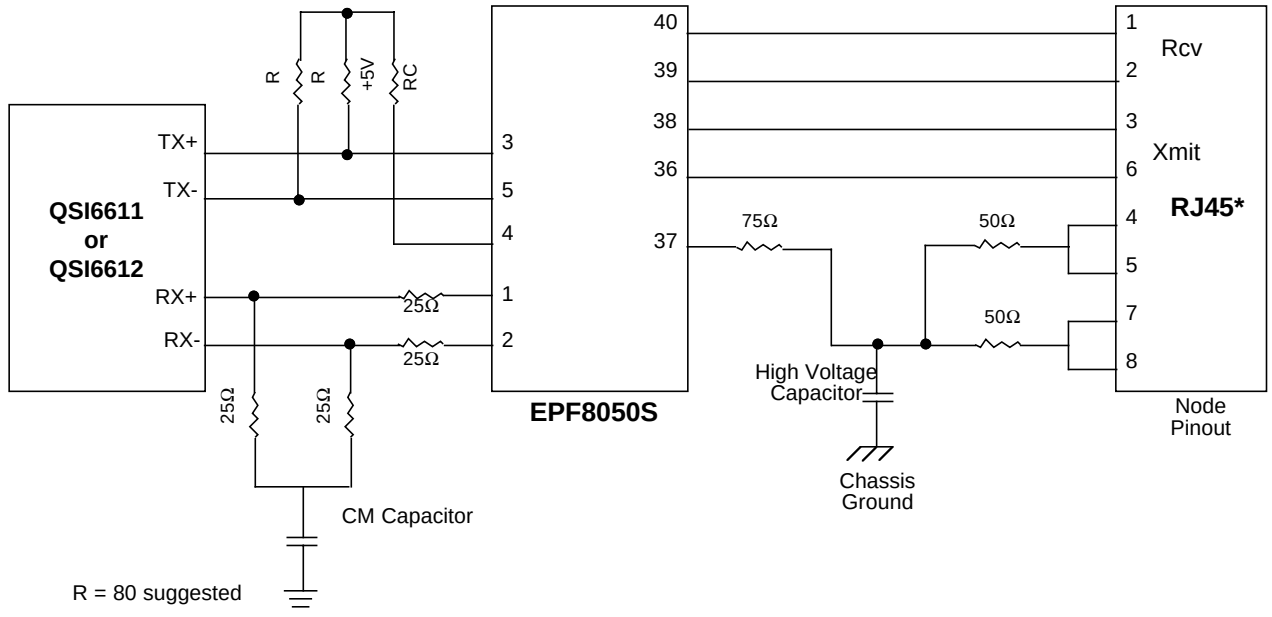
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8050S. There need not be any ground plane beyond this plane.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP



Notes : R = 80Ω suggested; RC typical 39Ω. Consult QSI for update.
* NIC Side is shown. Hub side connection will have crossover swapping pins 3-6 &

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