PCF85176

Universal LCD driver for low multiplex rates

Rev. 01 — 14 April 2010 Product data sheet

1. General description

The PCF85176 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCF85176 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

2. Features and benefits

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to twenty 7-segment alphanumeric characters
  - Up to ten 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components required
- Manufactured in silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 16.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF85176H	TQFP64	plastic thin quad flat package, 64 leads; body 10 × 10 × 1.0 mm	SOT357-1
PCF85176T	TSSOP56	plastic thin shrink small outline package, 56 leads; body width 6.1 mm	SOT364-1

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF85176H	PCF85176H
PCF85176T	PCF85176T

5. Block diagram

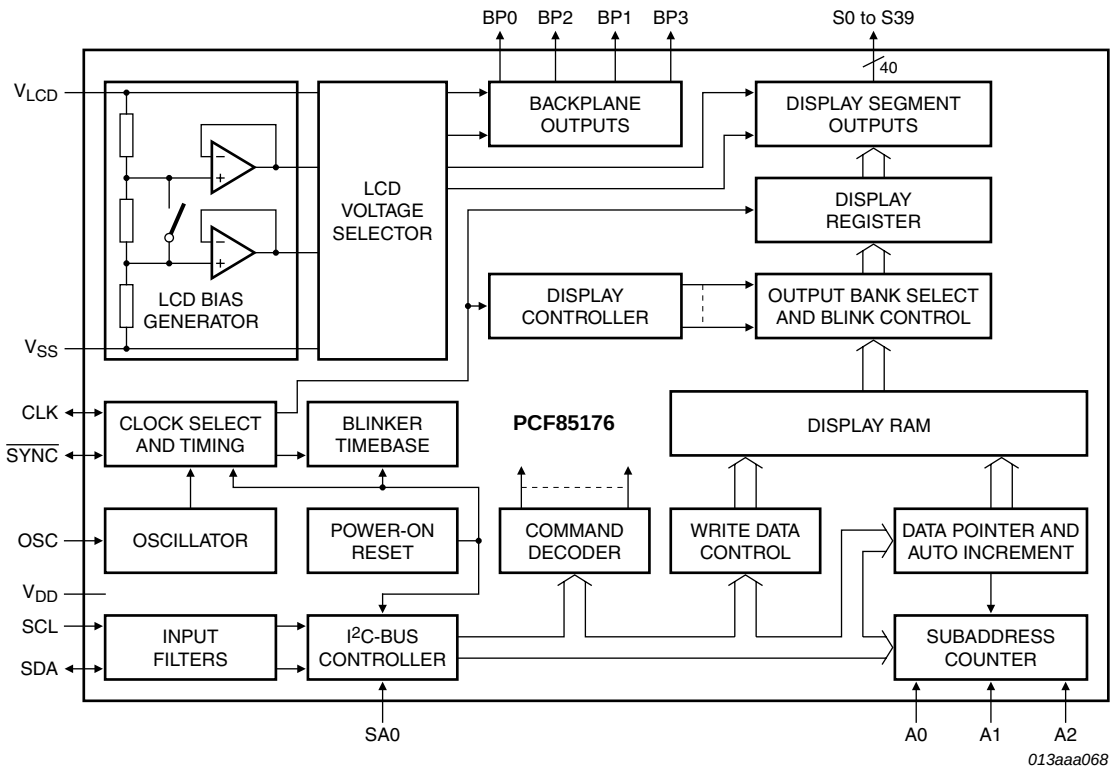
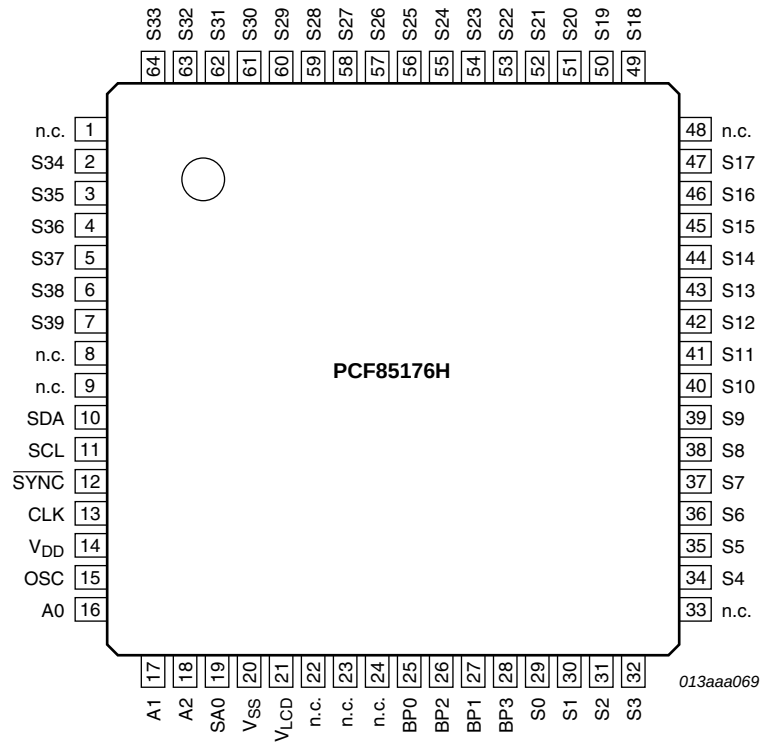


Fig 1. Block diagram of PCF85176

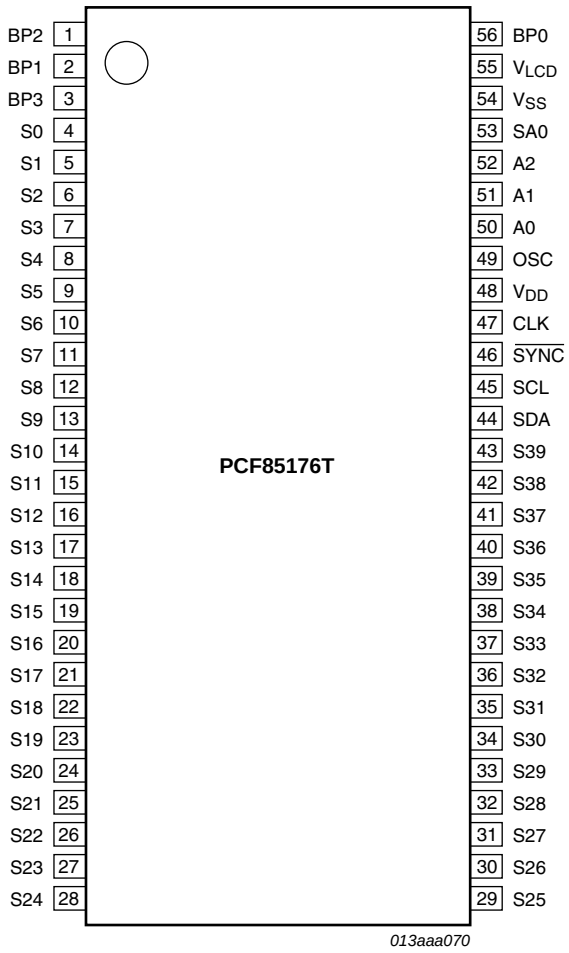
6. Pinning information

6.1 Pinning



Top view. For mechanical details, see Figure 25.

Fig 2. Pinning diagram for TQFP64 (PCF85176H)



Top view. For mechanical details, see Figure 26.

Fig 3. Pinning diagram for TSSOP56 (PCF85176T)

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	TQFP64 (PCF85176H)	TSSOP56 (PCF85176T)	Type	
SDA	10	44	input/output	I^2C-bus serial data line
SCL	11	45	input	I^2C-bus serial clock
CLK	13	47	input/output	clock line
V_{DD}	14	48	supply	supply voltage
$\overline{SYNC}$	12	46	input/output	cascade synchronization
OSC	15	49	input	internal oscillator enable
A0 to A2	16 to 18	50 to 52	input	subaddress inputs
SA0	19	53	input	I^2C-bus address input
V_{SS}	20	54	supply	ground supply voltage
V_{LCD}	21	55	supply	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	56, 1, 2, 3	output	LCD backplane outputs
S0 to S39	29 to 32, 34 to 47, 49 to 64, 2 to 7	4 to 43	output	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	not connected; do not connect and do not use as feed through

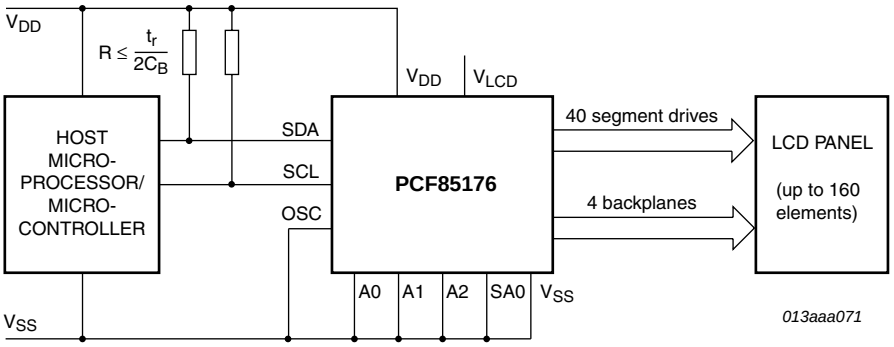
7. Functional description

The PCF85176 is a versatile peripheral device designed to interface any microprocessor or microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

The possible display configurations of the PCF85176 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 4. All of these configurations can be implemented in the typical system shown in Figure 4.

Table 4. Display configurations

Number of:		7-segment alphanumeric		14-segment alphanumeric		Dot matrix
Backplanes	Elements	Digits	Indicator symbols	Characters	Indicator symbols	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)



The resistance of the power lines must be kept to a minimum.

Fig 4. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I^2C-bus communication channel with the PCF85176. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

7.1 Power-On Reset (POR)

At power-on the PCF85176 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)

- Display is disabled

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{LCD} and V_{SS}. The center resistor is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex configuration is selected.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 5.

Table 5. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

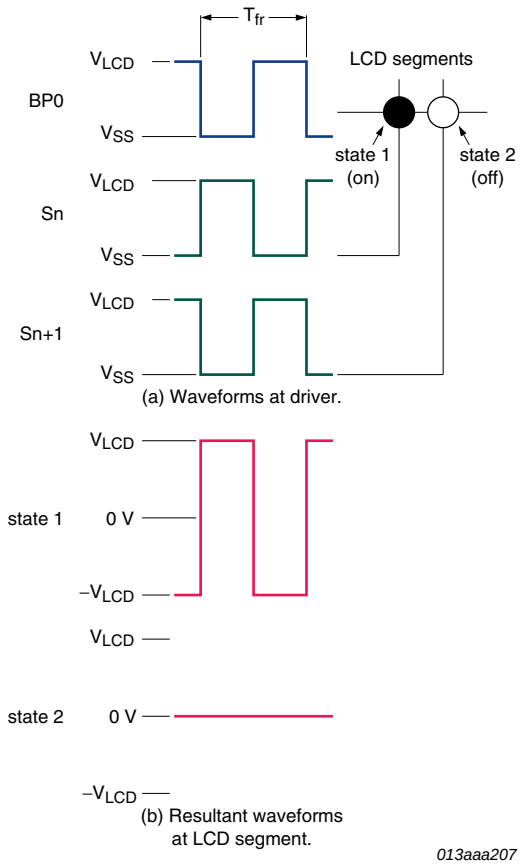
These compare with $V_{LCD} = 3 V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment (Sn) drive waveforms for this mode are shown in Figure 5.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

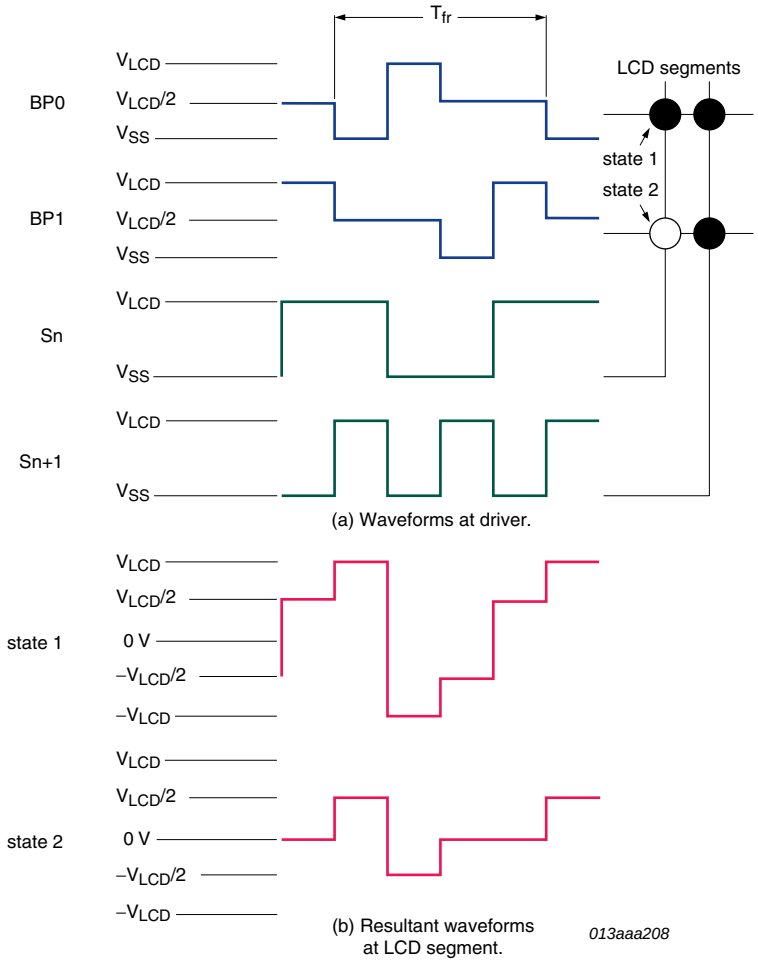
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 5. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF85176 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 6 and Figure 7.



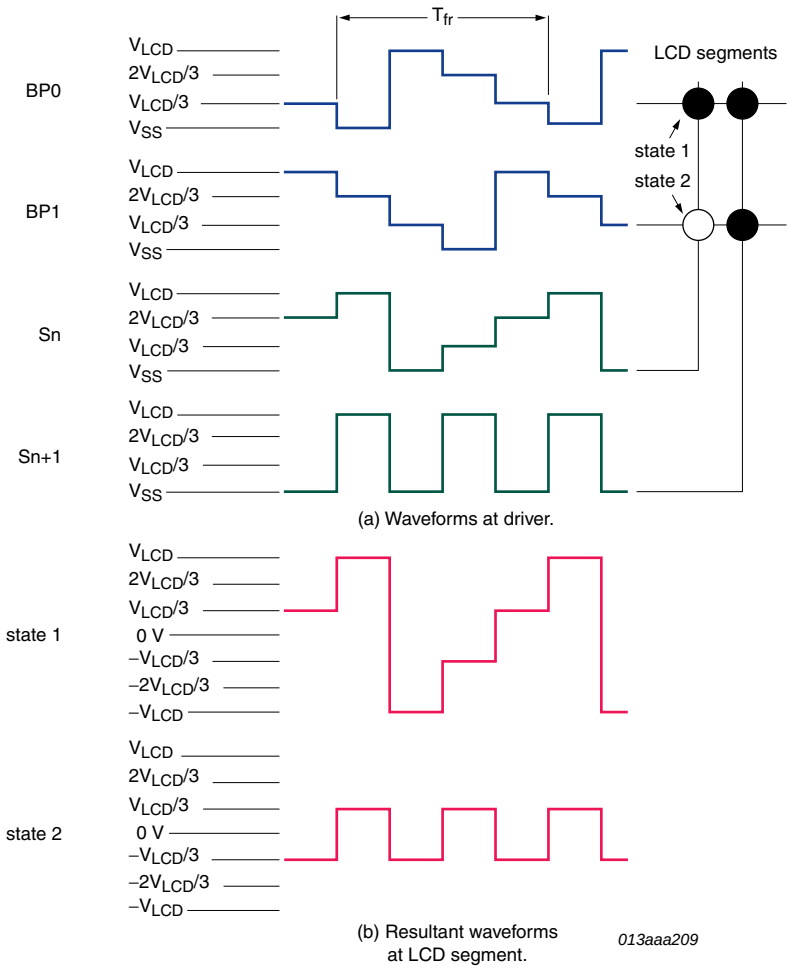
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 6. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

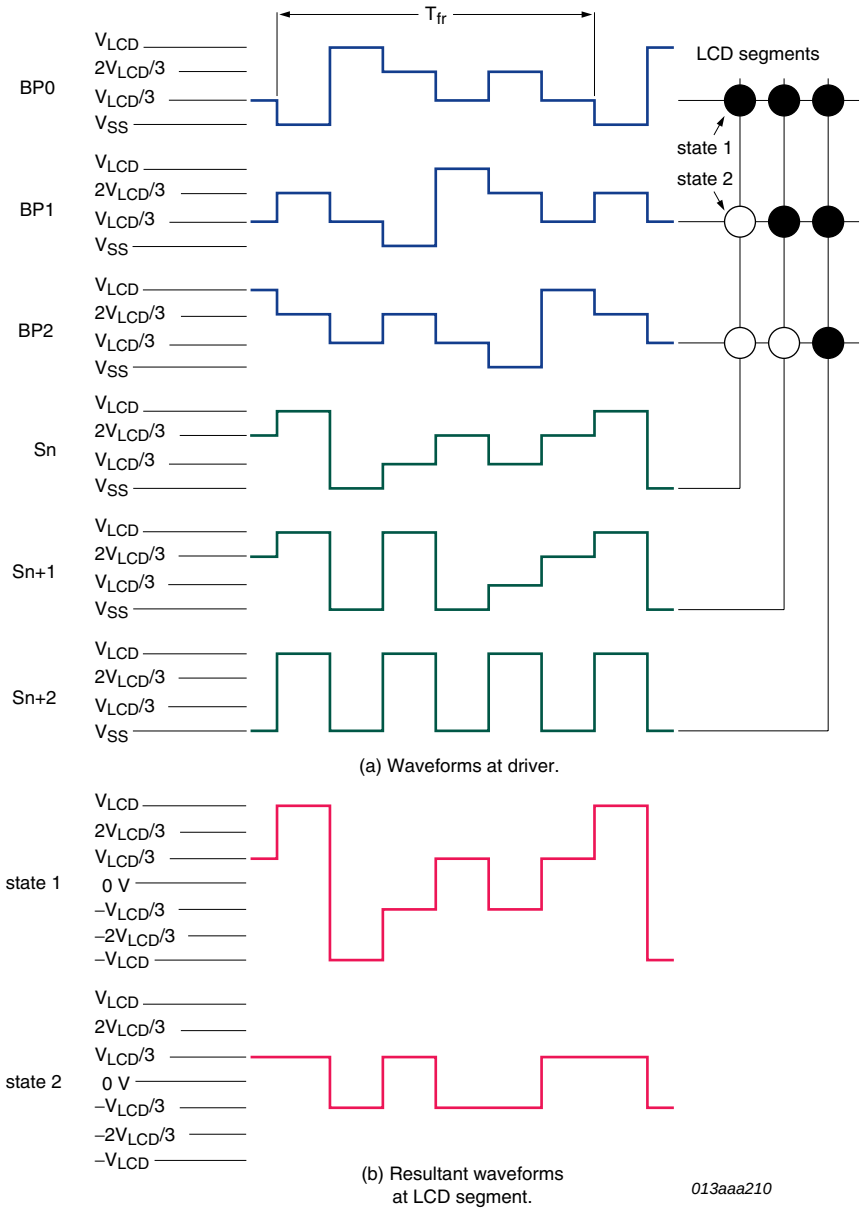
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with $^1/_3$ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 8.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

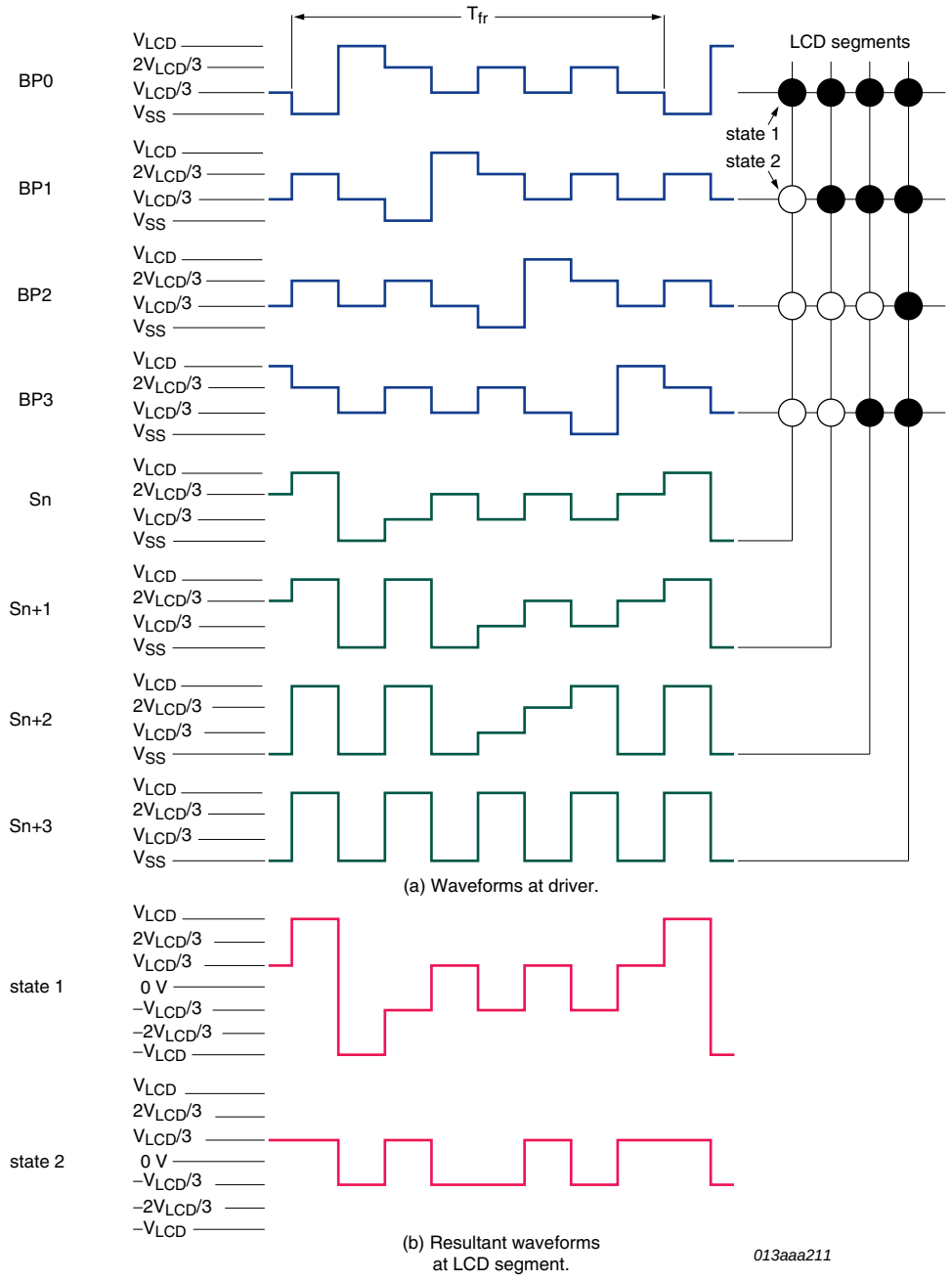
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:3 multiplex drive mode with $^1/_3$ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:4 multiplex drive mode with $^1/_3$ bias

7.5 Oscillator

7.5.1 Internal clock

The internal logic of the PCF85176 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF85176 in the system that are connected in cascade.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}. The LCD frame signal frequency is determined by the clock frequency (f_{clk}).

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing

The PCF85176 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF85176 in the system is maintained by the synchronization signal at pin $\overline{\text{SYNC}}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.8 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.

- In static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

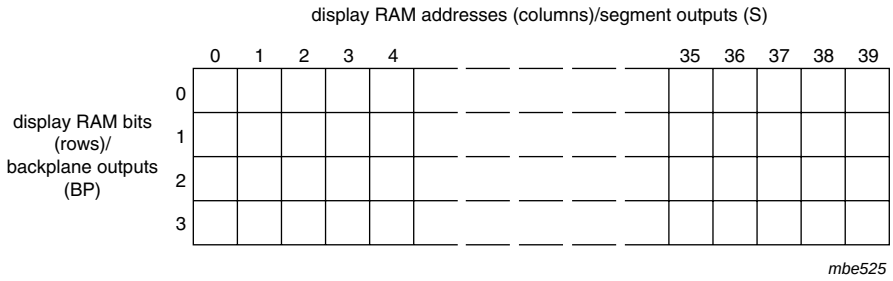
The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

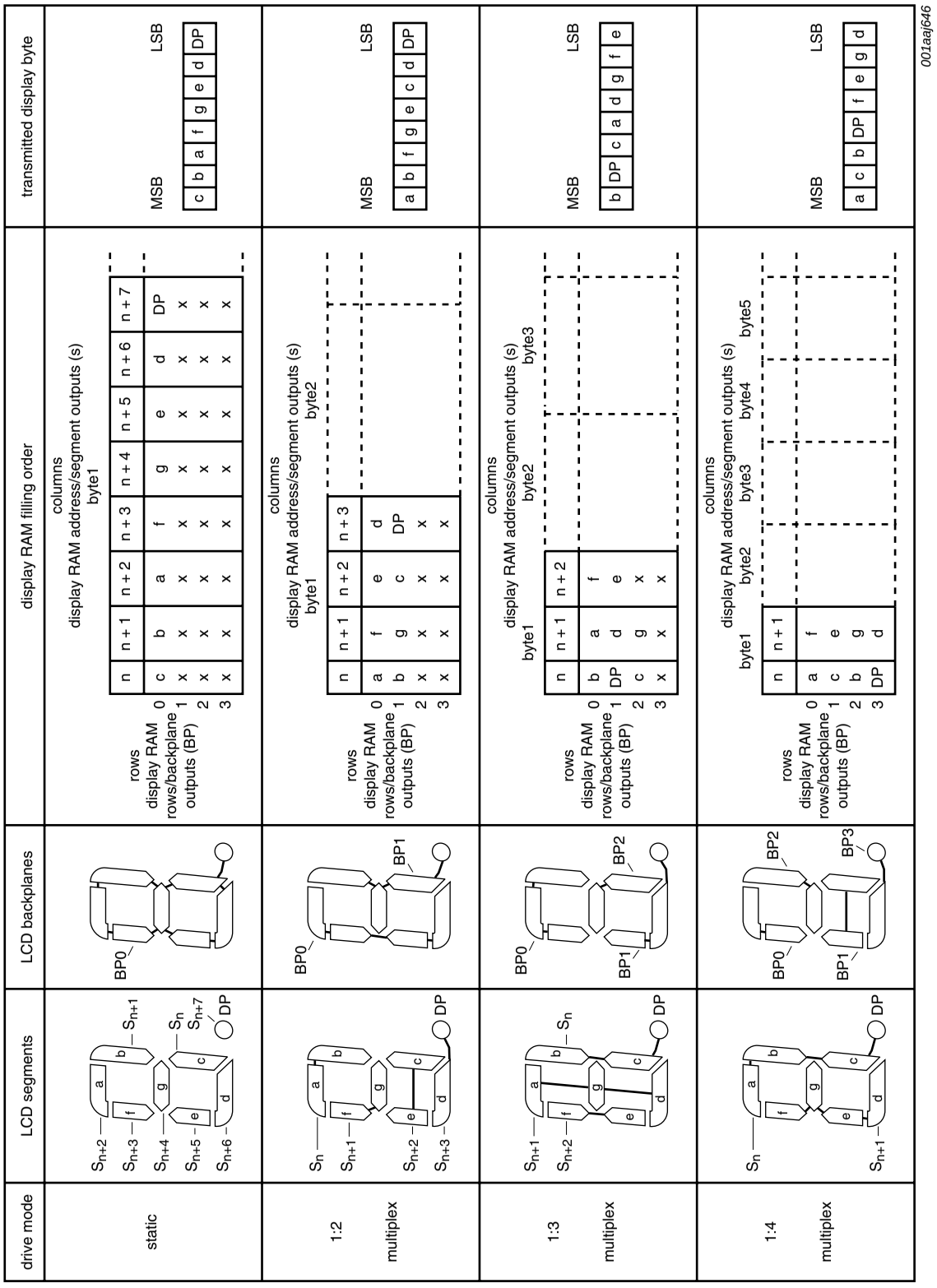
The display RAM bit map, Figure 10, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

Fig 10. Display RAM bit map

When display data is transmitted to the PCF85176 the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 11; the RAM filling organization depicted applies equally to other LCD types.



x = data bit unchanged.

Fig 11. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

The following applies to Figure 11:

- In static drive mode the eight transmitted data bits are placed in row 0 of eight successive 4-bit RAM words.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 to three successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of two successive 4-bit RAM words.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 11). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 11.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^2C-bus data access is terminated early then the state of the data pointer is unknown. The data pointer should be re-written prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed only when the content of the subaddress counter match with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 12). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF85176 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

7.13 Output bank selector

The output bank selector (see Table 13) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, row 2, and then row 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCF85176 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 13). The input bank selector functions independently to the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCF85176 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 14). The blink frequencies are fractions of the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected (see Table 6).

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

Table 6. Blink frequencies[1]

Blink mode	Blink frequency equation
off	-
1	$f_{blink} = \frac{f_{clk}}{768}$
2	$f_{blink} = \frac{f_{clk}}{1536}$
3	$f_{blink} = \frac{f_{clk}}{3072}$

[1] The blink frequency is proportional to the clock frequency (f_{clk}). For the range of the clock frequency see Table 17.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 10).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta Line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 12).

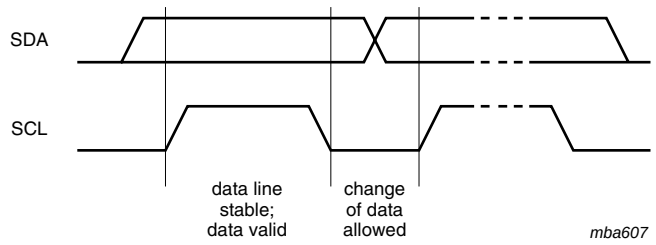


Fig 12. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 13).

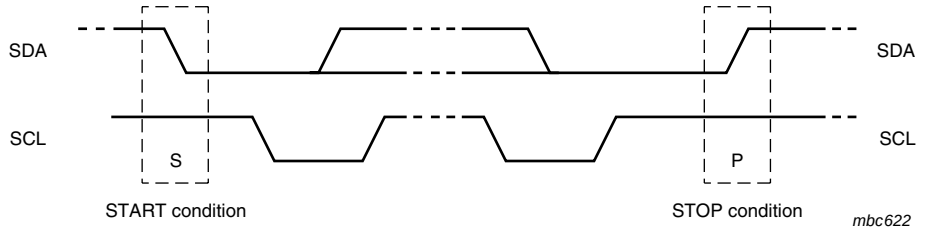


Fig 13. Definition of START and STOP conditions

7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 14).

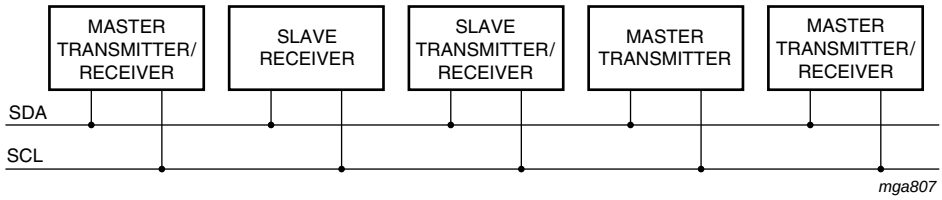


Fig 14. System configuration

7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is illustrated in Figure 15.

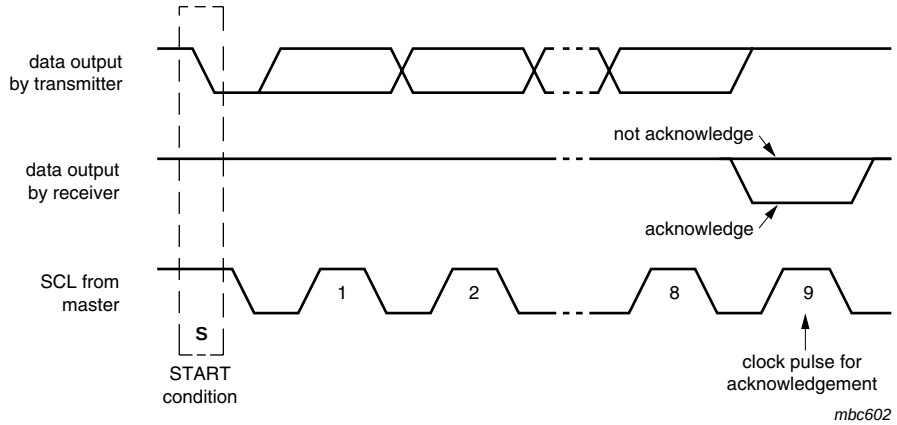


Fig 15. Acknowledgement of the I²C-bus

7.16.5 I²C-bus controller

The PCF85176 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF85176 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme, so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the PCF85176. The entire I²C-bus slave address byte is shown in Table 7.

Table 7. I²C slave address byte

Bit	Slave address							
	7	6	5	4	3	2	1	0
	MSB							LSB
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The PCF85176 is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte that a PCF85176 will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCF85176 for very large LCD applications
- The use of two types of LCD multiplex drive

The I²C-bus protocol is shown in Figure 16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCF85176 slave addresses available. All PCF85176 whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF85176 whose SA0 inputs are set to the alternative level.

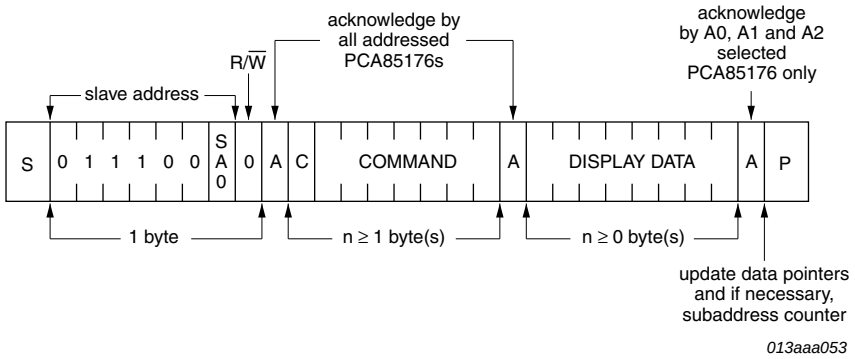


Fig 16. I²C-bus protocol

After an acknowledgement, one or more command bytes follow that define the status of each addressed PCF85176.

The last command byte sent is identified by resetting its most significant bit, continuation bit C (see Figure 17). The command bytes are also acknowledged by all addressed PCF85176 on the bus.

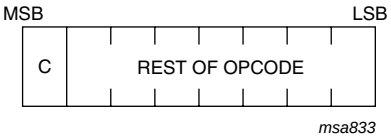


Fig 17. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCF85176 device.

An acknowledgement after each byte is asserted only by the PCF85176 that are addressed via address lines A0, A1, and A2. After the last display byte, the I²C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I²C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus.

The commands available to the PCF85176 are defined in Table 8.

Table 8. Definition of PCF85176 commands

Bit position labelled as - is not used.

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	-	E	B	M[1:0]		Table 10
load-data-pointer	C	0	P[5:0]						Table 11
device-select	C	1	1	0	0	A[2:0]			Table 12
bank-select	C	1	1	1	1	0	I	O	Table 13
blink-select	C	1	1	1	0	A	BF[1:0]		Table 14

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 17. When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see Table 9).

Table 9. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

Table 10. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 5	-	10	fixed value
4	-	-	unused
3	E		**display status**
		0	disabled[1]
		1	enabled
2	B		**LCD bias configuration**
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

Table 11. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6	-	0	fixed value
5 to 0	P[5:0]	000000 to 100111	6 bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses

Table 12. Device-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 3	-	1100	fixed value
2 to 0	A[2:0]	000 to 111	3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

Table 13. Bank-select command bit description

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7	C	0, 1	see Table 9	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

Table 14. Blink-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 3	-	1110	fixed value
2	A		**blink mode selection**
		0	normal blinking[1]
		1	alternate RAM bank blinking[2]
1 to 0	BF[1:0]		**blink frequency selection**
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

8. Internal circuitry

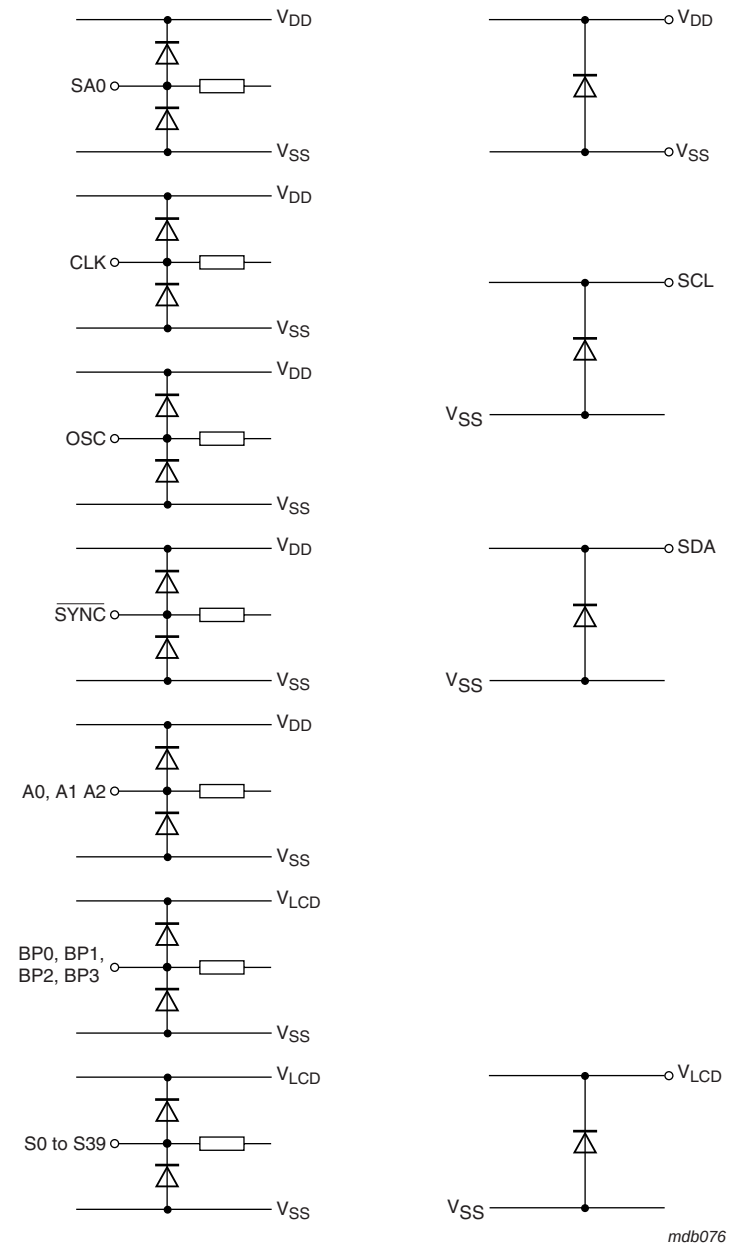


Fig 18. Device protection circuits

9. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
V_{LCD}	LCD supply voltage			−0.5	+7.5	V
V_I	input voltage	on each of the pins CLK, SDA, SCL, $\overline{SYNC}$, SA0, OSC, A0 to A2		−0.5	+6.5	V
V_O	output voltage	on each of the pins S0 to S39, BP0 to BP3		−0.5	+7.5	V
I_I	input current			−10	+10	mA
I_O	output current			−10	+10	mA
I_{DD}	supply current			−50	+50	mA
$I_{DD(LCD)}$	LCD supply current			−50	+50	mA
I_{SS}	ground supply current			−50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P_o	output power			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		MM	[2]	-	±200	V
		CDM	[3]	-	±1000	V
I_{lu}	latch-up current		[4]	-	200	mA
T_{stg}	storage temperature		[5]	−55	+150	°C
T_{oper}	operating temperature			−40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 5 “JESD22-A114”

[2] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”

[3] Pass level; Charged-Device Model (CDM), according to Ref. 7 “JESD22-C101”

[4] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[5] According to the NXP store and transport requirements (see Ref. 10 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

10. Static characteristics

Table 16. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage		[1]	2.5	-	6.5	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz	[2][3]	-	-	20	μA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz	[2][4]	-	-	60	μA
Logic							
$V_{P(POR)}$	power-on reset supply voltage			1.0	1.3	1.6	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, SCL, SDA		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, SCL, SDA	[5][6]	$0.7V_{DD}$	-	V_{DD}	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V					
		on pins CLK and $\overline{SYNC}$		1	-	-	mA
		on pin SDA		3	-	-	mA
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V		1	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}; on pins CLK, SCL, SDA, A0 to A2 and SA0		−1	-	+1	μA
$I_{L(OSC)}$	leakage current on pin OSC	$V_I = V_{DD}$		−1	-	+1	μA
C_I	input capacitance		[7]	-	-	7	pF
LCD outputs							
ΔV_O	output voltage variation	on pins BP0 to BP3 and S0 to S39		−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V	[8]				
		on pins BP0 to BP3		-	1.5	-	kΩ
		on pins S0 to S39		-	6.0	-	kΩ

[1] $V_{LCD} > 3$ V for $\frac{1}{3}$ bias.

[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[3] For typical values, see Figure 19.

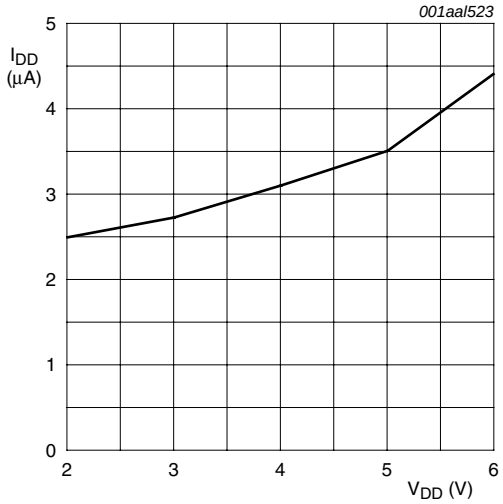
[4] For typical values, see Figure 20.

[5] When tested, I^2C pins SCL and SDA have no diode to V_{DD} and may be driven to the V_I limiting values given in Table 15 (see Figure 18 as well).

[6] Propagation delay of driver between clock (CLK) and LCD driving signals.

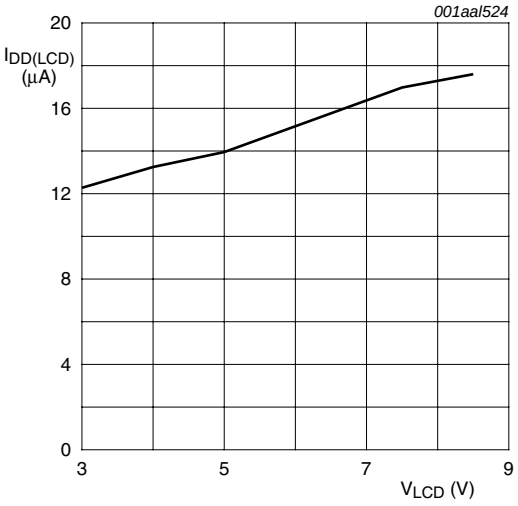
[7] Periodically sampled, not 100 % tested.

[8] Outputs measured one at a time.



T_{amb} = 30 °C; 1:4 multiplex; V_{LCD} = 6.5 V; $f_{clk(ext)}$ = 1.536 kHz; all RAM written with logic 1; no display connected; I^2C-bus inactive.

Fig 19. Typical I_{DD} with respect to V_{DD}



T_{amb} = 30 °C; 1:4 multiplex; $f_{clk(ext)}$ = 1.536 kHz; all RAM written with logic 1; no display connected.

Fig 20. Typical $I_{DD(LCD)}$ with respect to V_{LCD}

11. Dynamic characteristics

Table 17. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
$f_{clk(int)}$	internal clock frequency		[1]	1440	1970	2640	Hz
$f_{clk(ext)}$	external clock frequency			960	-	2640	Hz
f_{fr}	frame frequency	internal clock		60	82	110	Hz
		external clock		40	-	110	Hz
$t_{clk(H)}$	HIGH-level clock time			60	-	-	µs
$t_{clk(L)}$	LOW-level clock time			60	-	-	µs
Synchronization							
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time			1	-	-	µs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V	[2]	-	-	30	µs
I^2C-bus[3]							
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz		-	-	0.3	µs
		f_{SCL} < 125 kHz		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width	on the I^2C-bus		-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

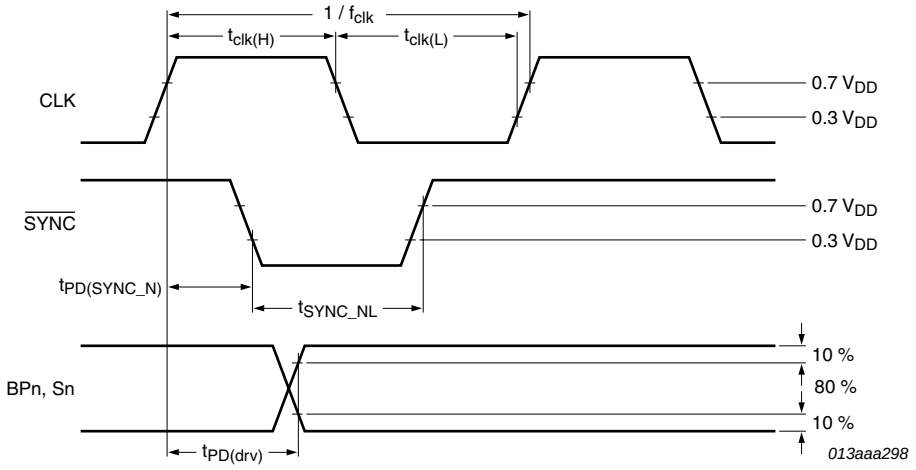


Fig 21. Driver timing waveforms

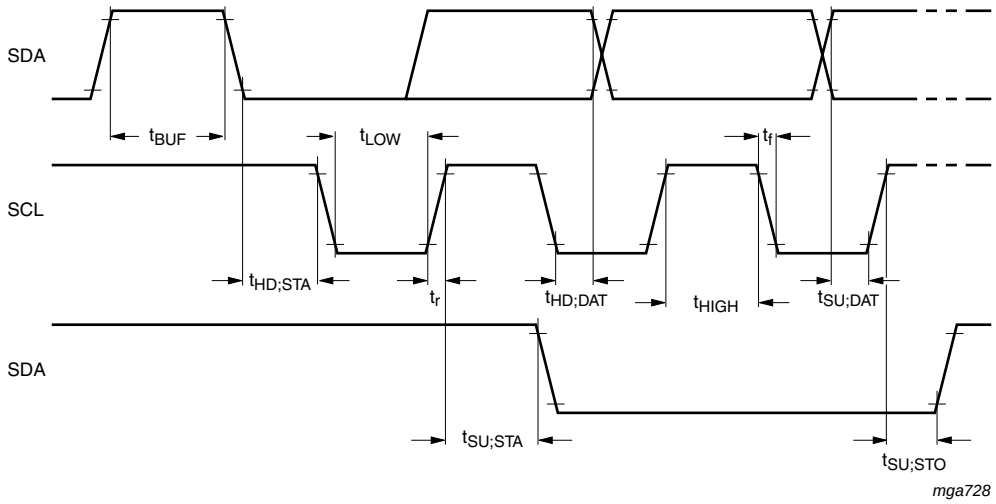


Fig 22. I²C-bus timing waveforms

12. Application information

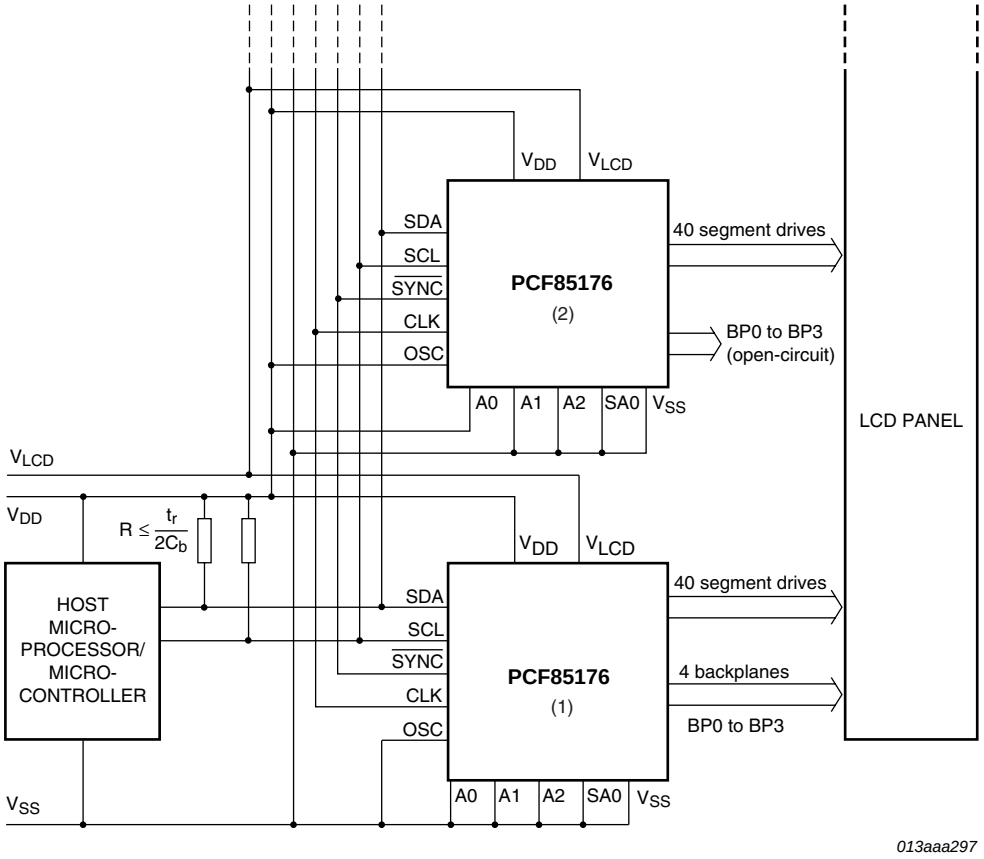
12.1 Cascaded operation

Large display configurations of up to 16 PCF85176 can be recognized on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1, and A2) and the programmable I^2C-bus slave address (SA0).

Table 18. Addressing cascaded PCF85176

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

When cascaded PCF85176 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF85176 of the cascade contribute additional segment outputs, but their backplane outputs are left open-circuit (see Figure 23).



(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 23. Cascaded PCF85176 configuration

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF85176. Synchronization is guaranteed after a power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by defining a multiplex drive mode when PCF85176 with different SA0 levels are cascaded).

$\overline{SYNC}$ is organized as an input/output pin. The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCF85176 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF85176 to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF85176 are shown in Figure 24.

The contact resistance between the $\overline{SYNC}$ on each cascaded device must be controlled. If the resistance is too high, the device is not able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum $\overline{SYNC}$ contact resistance allowed for the number of devices in cascade is given in Table 19.

Table 19. $\overline{SYNC}$ contact resistance

Number of devices	Maximum contact resistance
2	6 kΩ
3 to 5	2.2 kΩ
6 to 10	1.2 kΩ
10 to 16	700 Ω

The PCF85176 can always be cascaded with other devices of the same type or conditionally with other devices of the same family. This allows optimal drive selection for a given number of pixels to display. Figure 21 and Figure 24 show the timing of the synchronization signals.

In a cascaded configuration only one PCF85176 master must be used as clock source. All other PCF85176 in the cascade must be configured as slave such that they receive the clock from the master.

If an external clock source is used, all PCF85176 in the cascade must be configured such as to receive the clock from that external source (pin OSC connected to V_{DD}). Thereby it must be ensured that the clock tree is designed such that on all PCF85176 the clock propagation delay from the clock source to all PCF85176 in the cascade is as equal as possible since otherwise synchronization artefacts may occur.

In mixed cascading configurations, care has to be taken that the specifications of the individual cascaded devices are met at all times.

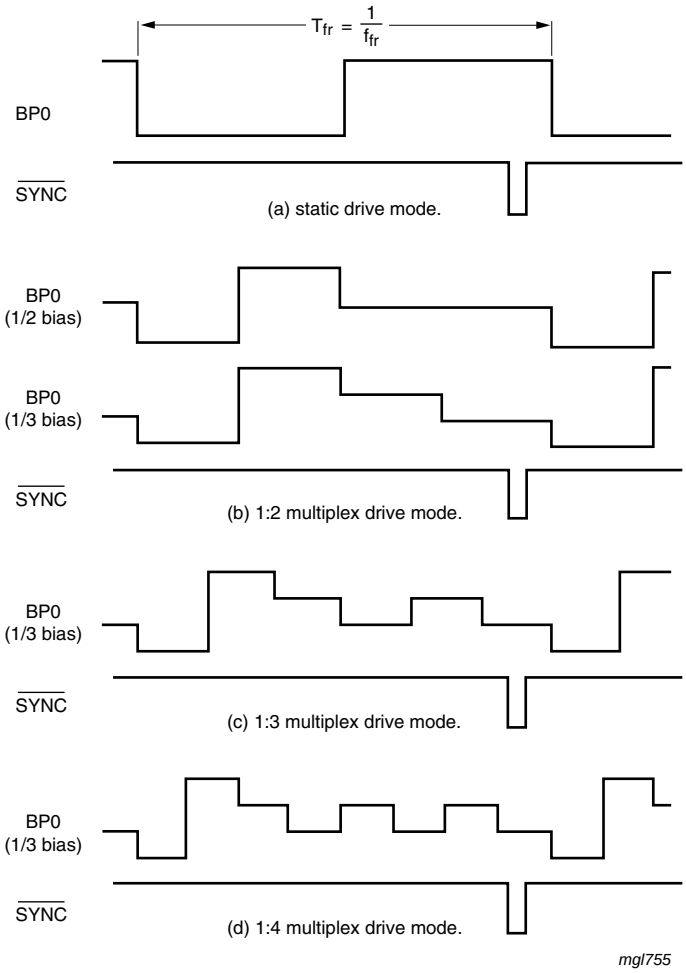
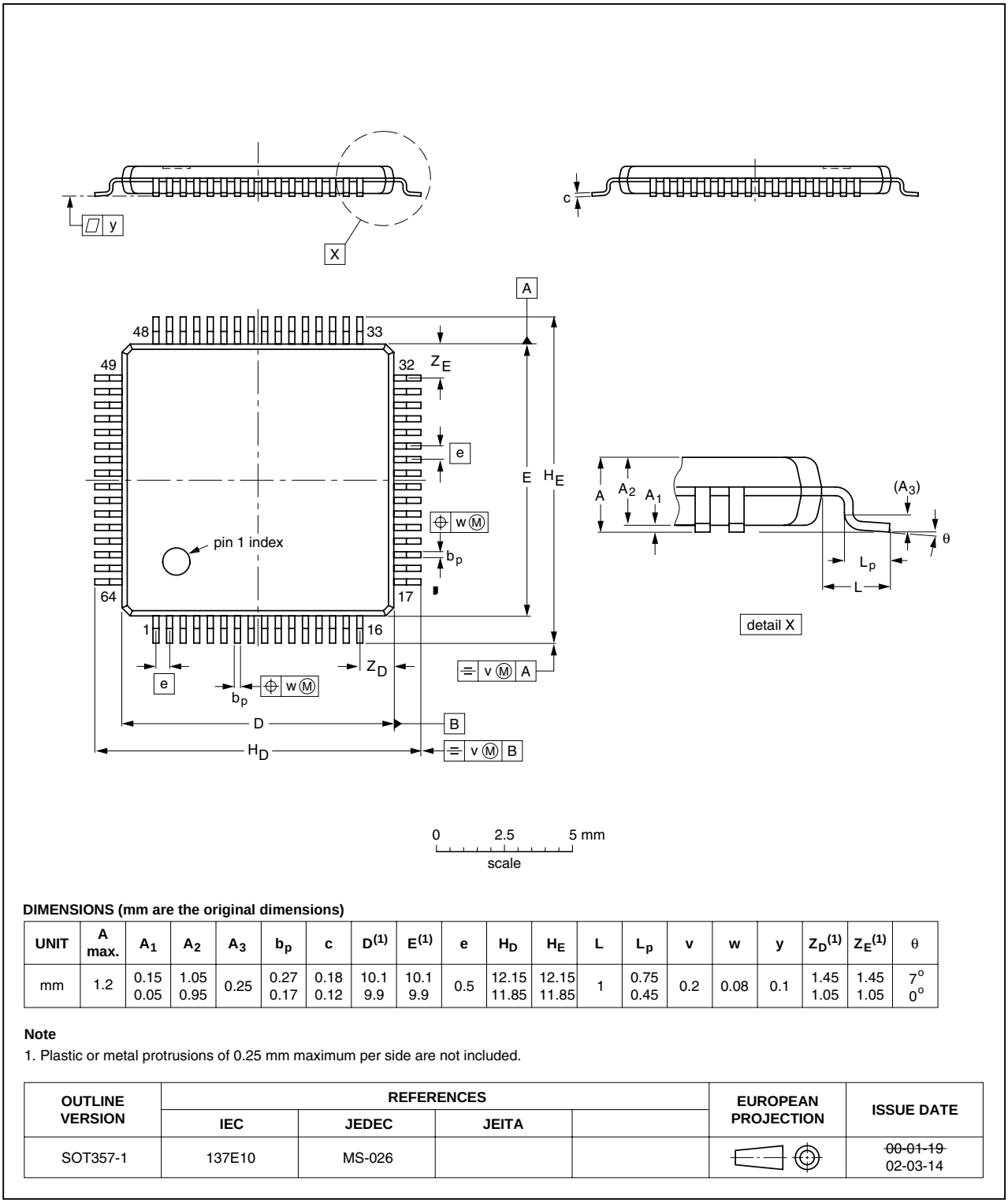


Fig 24. Synchronization of the cascade for the various PCF85176 drive modes

13. Package outline

TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm **SOT357-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7^o 0^o

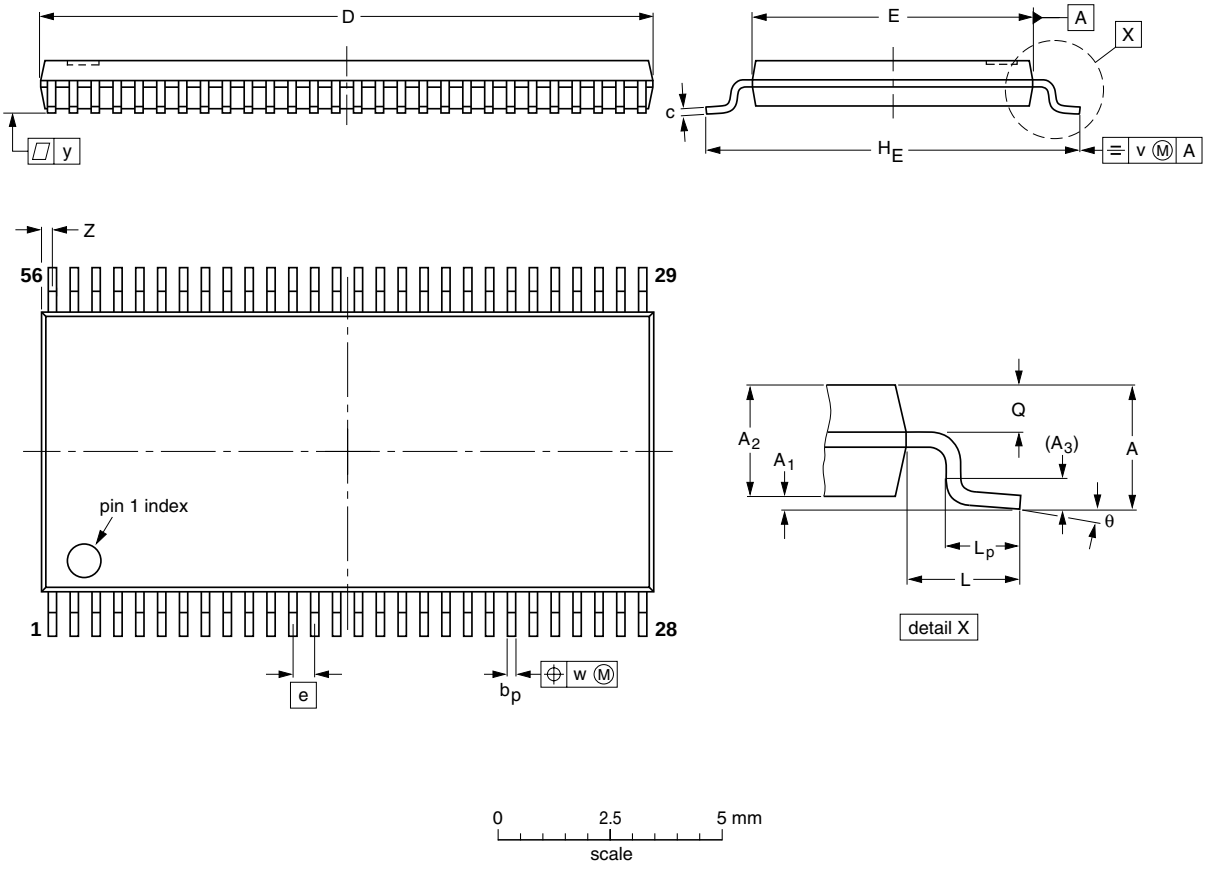
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT357-1	137E10	MS-026				~~00-01-19~~ 02-03-14

Fig 25. Package outline SOT357-1 (TQFP64) of PCF85176H

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 26. Package outline SOT364-1 (TSSOP56) of PCF85176T

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 27) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 20 and 21

Table 20. SnPb eutectic process (from J-STD-020C)

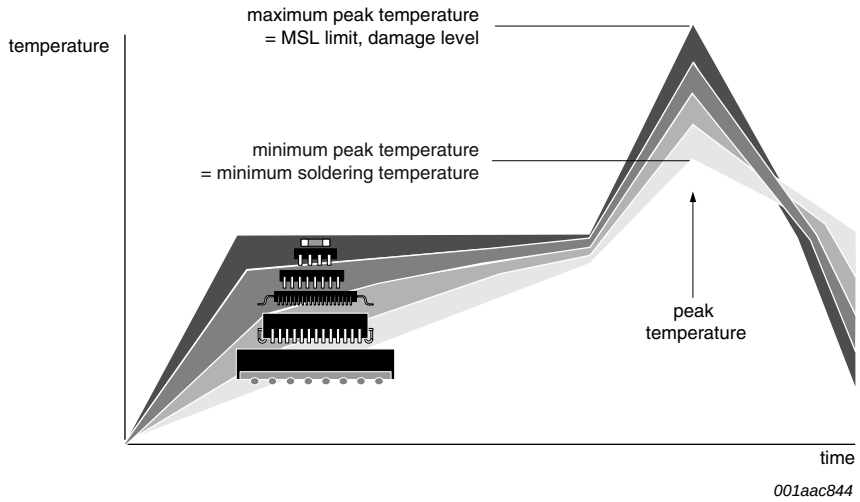
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 21. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 27.



MSL: Moisture Sensitivity Level

Fig 27. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 22. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
CDM	Charged Device Model
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RAM	Random Access Memory
RC	Resistance and Capacitance
RMS	Root Mean Square
SCL	Serial Clock Line
SDA	Serial DAta Line
SMD	Surface-Mount Device

17. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **NX3-00092 —** NXP store and transport requirements

[11] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[12] **UM10204 —** I^2C-bus specification and user manual

18. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF85176_1	20100414	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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