CAT6612

Single-Link HDMI Transmitter

CHIP ADVANCED TECHNOLOGY
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General Description

The CAT6612 is a high-performance and low-cost single channel HDMI transmitter, fully compliant with HDMI 1.2, HDCP 1.1 and backward compatible to DVI 1.0 specifications. The CAT6612 serves to provide the most cost-effective HDMI solution for DTV-ready consumer electronics such as settop boxes, DVD players and A/V receivers, as well as DTV-enriched PC products such as notebooks and desktops, without compromising the performance. Its backward compatibility to DVI standard allows connectivity to myriad video displays such as LCD and CRT monitors, in addition to the ever-so-flourishing flat panel TVs.

Aside from the various video output formats supported, the CAT6612 also supports 2 channels of I^2S digital audio, with sampling rate up to 192kHz and sample size up to 24 bits. CAT6612 also support S/PDIF input of up to 192kHz sampling rate.

By default the CAT6612 comes with integrated HDCP ROMs which are pre-programmed with HDCP keys that ensures secure digital content transmission. Users need not worry about the procurement and maintainence of the HDCP keys.

Features

- Single channel HDMI transmitter
- Compliant with HDMI 1.2, HDCP 1.1 and DVI 1.0 specifications
- Supporting pixel rates from 25MHz to 165MHz
  - DTV resolutions: 480i, 576i, 480p, 576p, 720p, 1080i up to 1080p
  - PC resolutions: VGA, SVGA, XGA, SXGA up to UXGA
- Various video input interface supporting digital video standards such as:
  - 24-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (CCIR-656)
  - 12-bit double data rate interface
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
- Dithering for conversion from 12-bit component and 8-bit
- Digital audio input interface supporting
  - audio sample rate: 32~192 kHz
  - sample size: 16~24 bits
  - one I2S interface supporting 2-channel audio

  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio transmission at up to 192kHz
  - Compatible with IEC 60958 and IEC 61937
- Software programmable HDMI output current, enabling user to optimize the performance for fixed-cable systems or those with pre-defined cable length
- MCLK input is optional for audio operation. Users could opt to implement audio input interface with or without MCLK.
- Integrated pre-programmed HDCP keys
- Purely hardware HDCP engine increasing the robustness and security of HDCP operation
- Monitor detection through Hot Plug Detection and Receiver Termination Detection
- Intelligent, programmable power management
- 80-pin LQFP package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
CAT6612CQ	0~70	80-pin LQFP	Green

Pin Diagram

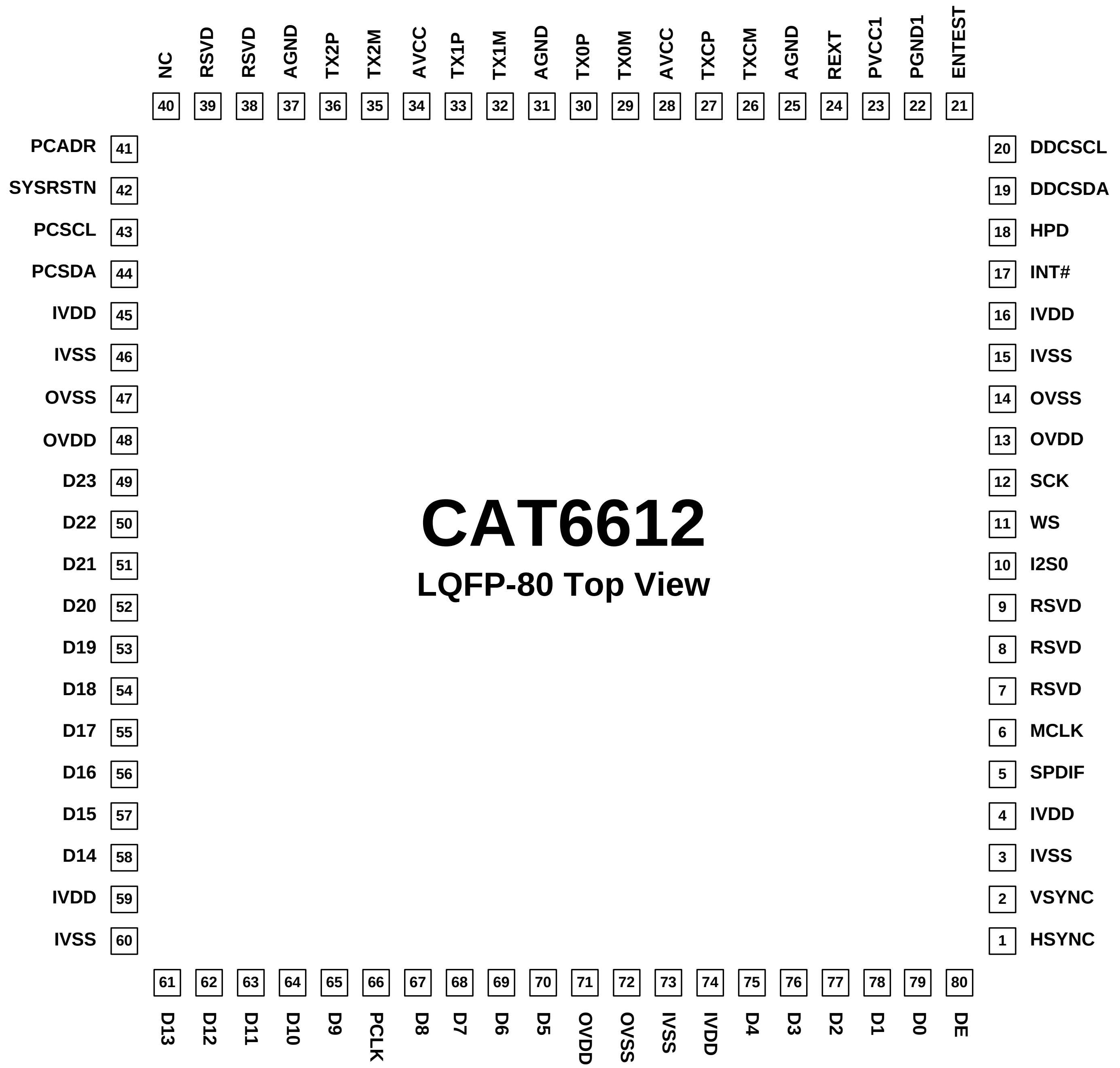


Figure 1. CAT6612 pin diagram

Pin Description

Digital Video Input Pins

Pin Name	Direction	Description	Type	Pin No.
D[23:0]	Input	Digital video input pins. D[23:12] are only used in 24-bit single-edged mode. In 12-bit, dual-edged mode D[23:12] should be tied to ground.	LVTTL	49-58, 61-65, 67-70, 75-79
DE	Input	Data enable	LVTTL	80
HSYNC	Input	Horizontal sync. signal	LVTTL	1
VSYNC	Input	Vertical sync. signal	LVTTL	2
PCLK	Input	Input data clock	LVTTL	66

Digital Audio Input Pins

Pin Name	Direction	Description	Type	Pin No.
MCLK	Input	Audio master clock input	LVTTL	6
SCK	Input	I2S serial clock input	LVTTL	12
WS	Input	I2S word select input	LVTTL	11
I2S0	Input	I2S serial data input	LVTTL	10
SPDIF	Input	S/PDIF audio input	LVTTL	5

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
INT#	Output	Interrupt output. Default active-low (5V-tolerant)	LVTTL	17
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	Schmitt	42
DDCSCL	I/O	I^2C Clock for DDC (5V-tolerant)	Schmitt	20
DDCSDA	I/O	I^2C Data for DDC (5V-tolerant)	Schmitt	19
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	43
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	44
PCADR	Input	Serial programming device address select	LVTTL	41
HPD	Input	Hot Plug Detection (5V-tolerant)	LVTTL	18
ENTEST	Input	Must be tied low via a resistor.	LVTTL	21
NC		Must be left unconnected		41
RSVD		Could be tied to either low or high, **or** just left connected in the way of CAT6611		7, 8, 9, 38, 39

HDMI front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Analog	HDMI Channel 2 positive output	TMDS	36
TX2M	Analog	HDMI Channel 2 negative output	TMDS	35
TX1P	Analog	HDMI Channel 1 positive output	TMDS	33
TX1M	Analog	HDMI Channel 1 negative output	TMDS	32
TX0P	Analog	HDMI Channel 0 positive output	TMDS	30
TX0M	Analog	HDMI Channel 0 negative output	TMDS	29
TXCP	Analog	HDMI Clock Channel positive output	TMDS	27
TXCM	Analog	HDMI Clock Channel negative output	TMDS	26
REXT	Analog	External resistor for setting TMDS output level. Default tied to AVCC via a 475-Ohm SMD resistor.	Analog	24

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	4, 16, 45, 59, 74
IVSS	Digital logic ground	Ground	3, 15, 46, 60, 73
OVDD	I/O Pin power (3.3V)	Power	13, 48, 71
OVSS	I/O Pin ground	Ground	14, 47, 72
AVCC	HDMI analog frontend power (3.3V)	Power	28, 34
AGND	HDMI analog frontend ground	Ground	25, 31, 37
PVCC1	HDMI core PLL power (3.3V)	Power	23
PGND1	HDMI core PLL ground	Ground	22

Functional Description

CAT6612 provides complete solutions for HDMI Source systems by implementing all the required HDMI functions. In addition, advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion and up/down sampling. The following picture is the functional block digram of CAT6612, which describes clearly the data flow.

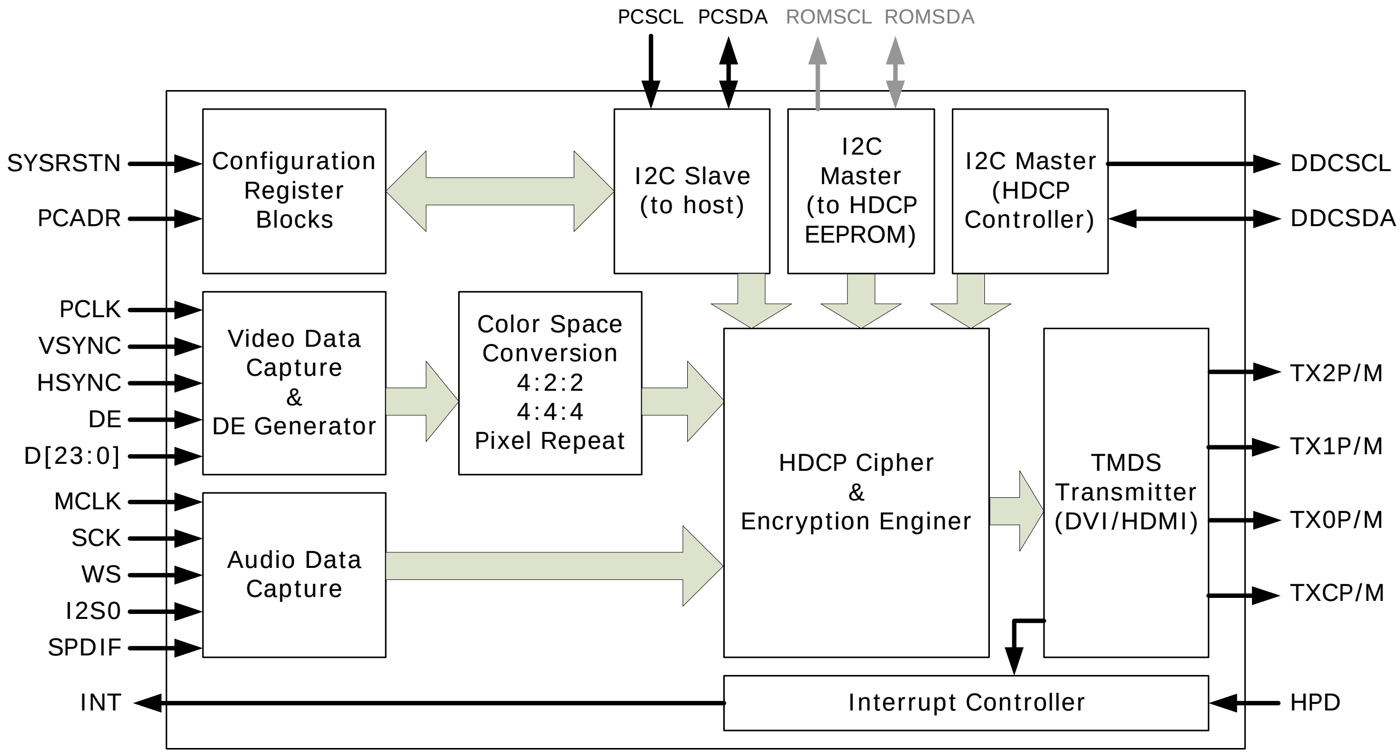


Figure 2. Functional block diagram of CAT6612

Video Data Processing Flow

Figure 3 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enablings and path bypassings are controlled through register programming. Please refer to CAT6612 Programming Guide for detailed and precise descriptions.

As can be seen from Figure 3, the first step of video data processing is to prepare the video data (Data), data enable signal (DE), video clock (Clock), horizontal sync and vertical sync signals (H/VSYNC). While the video data and video clock are always readily available from input pins, the preparation of the data enable and sync signals require special extraction process (Embedded Ctrl. Signals Extraction & DE Generator) depending on the format of input video data.

All the data then undergo a series of video processing including YCbCr up/down-sampling, color-space conversion and dithering. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected input-output format combination and the corresponding video processing block selection. Please refer to the CAT6612 Programming Guide for suggested register setting.

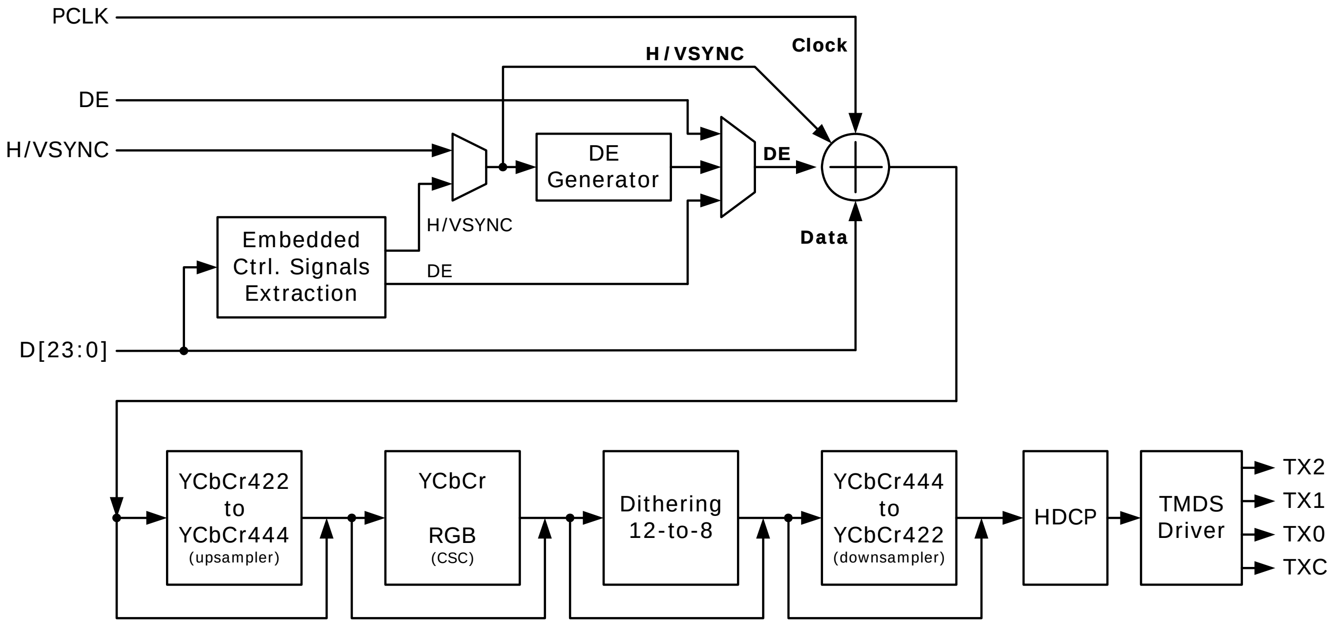


Figure 3. Video data processing flow of CAT6612

Designated as D[23:0], the input video data could take on bus width of 8 bits to 24 bits. This input interface could be configured through register setting to provide various data formats as listed in Table 1.

Although not explicitly depicted in Figure 3, input video clock (PCLK) can be configured to be multiplied by 0.5, 2 or 4, so as to support special formats such as CCIR-656 and pixel-repeating. This is also enabled by software programming.

General description of block functions is as follows:

Extraction of embedded control signals (Embedded Ctrl. Signals Extraction)

Input video formats with only embedded sync signals rely on this block to derive the proper Hsync, Vsync and DE signals. Specifically, CCIR-656 video streams includes Start of Active Video (SAV) and End of Active Video (EAV) that this block uses to extract the required control signals.

Generation of data enable signal (DE Generator)

DE signal defines the region of active video data. In cases where the video decoders supply no such DE signals to CAT6612, this block is used to generate appropriate DE signal from Hsync, Vsync and Clock.

Upsampling (YCbCr422 to YCbCr444)

In cases where input signals are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr ↔ RGB)

Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB ↔ YCbCr color space conversion (CSC). To provide maximum flexibility, the maxtrix coefficients of the CSC engine in CAT6612 are fully programmable. Users of CAT6612 could elect to employ their preferred conversion formula.

Dithering (Dithering 12-to-8)

All the video processings in CAT6612 are done in 12 bits per channel in order to minimize rounding errors and other computational residuals that occur during processing. For outputing to the 8-bits-per-channel formats, decimation from 12 bits to 8 bits is required. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

Downsampling (YCbCr444 to YCbCr422)

In cases where input signals are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

HDCP engine (HDCP)

The HDCP engine in CAT6612 handles all the processing requried by HDCP mechanism in hardware. Software intervention is not necessary except checking for revocation. Preprogrammed HDCP keys are also embedded in CAT6612. Users need not worry about the purchasing and management of the HDCP keys as Chip Advanced Technology will take care of them.

TMDS driver (TMDS Driver)

The final stop of the data processing flow is TMDS serializer. The TMDS driver serializes the input parallel data and drive out the proper electrical signals to the HDMI cable. The output current level is controlled through connecting a precision resistor of proper value to Pin 24 (REXT).

Supported Input Video Formats

Table 1 lists the input video formats supported by CAT6612.

					Input Pixel clock frequency (MHz)							
Color Space	Video Format	Input Chs	Bus Width	Hsync/ Vsync	480i	480p	XGA	720p	1080i	SXGA	1080p	UXGA
RGB	4:4:4	3	24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
RGB	4:4:4	1	12	Separate	13.5	27	65	74.25	74.25	108	148.5	
YCbCr	4:4:4	3	24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
YCbCr	4:4:4	1	12	Separate	13.5	27	65	74.25	74.25	108	148.5	
YCbCr	4:2:2	2	16/20/24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
YCbCr	4:2:2	2	16/20/24	Embedded	13.5	27	65	74.25	74.25	108	148.5	162
YCbCr	4:2:2	1	8/10/12	Separate	27	54	130	148.5	148.5			
YCbCr	4:2:2	1	8/10/12	Embedded	27	54	130	148.5	148.5			

Table 1. Input video formats supported by CAT6612

Notes:
1. Table cells that are left blanks are those format combinations that are not supported by CAT6612.
2. Input channel number is defined by the way the three color components (either R, G & B or Y, Cb & Cr) are arranged. Refer to Video Data Bus Mappings starting page 17 for better understanding.
3. Embedded sync signals are defined by CCIR-656 standard, using SAV/EAV sequences of FF, 00, 00, XY.
4. The original pixel clock of 480i is 13.5MHz. HDMI standard mandates that a 27MHz pixel clock be used and pixel repeating is employed to keep the frequency range of the HDMI link within control.

Audio Data Capture and Processing

CAT6612 takes in one I^2S inputs as well as one S/PDIF input of audio data. The I^2S input allows transmission of 2-channel uncompressed audio data at up to 192kHz sample rate. The S/PDIF input allows transmission of uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz.

Note that MCLK input is optional for CAT6612. By default CAT6612 generates the MCLK internally to process the audio. Neither I^2S nor S/PDIF inputs requires MCLK input, coherent or not. However, if the user prefers inputing MCLK from external audio source, such configuration could be enabled through register setting. Refer to CAT6612 Programming Guide for such setting.

Interrupt Generation

The system micro-controller should take in the interrupt signal output by CAT6612 at PIN 17 (INT). CAT6612 generates an interrupt signal with events involving the following signals or situations:

1. Hot-plug detection (Pin 18, HPD) experiences state changes.

2. Receiver detection circuit reports the presence or absence of an active termination at the TMDS Clock Channel (Register 0Eh[5], RxSENDetect)
3. DDC bus is hanged for any reasons
4. Audio FIFO overflows
5. HDCP authentication fails
6. Video data is stable or not

A typical initialization of HDMI link should be based on interrupt signal and appropriate register probing. Recommended flow is detailed in CAT6612 Programming Guide. Simply put, the microcontroller should monitor the HPD status first. Upon valid HPD event, move on to check RxSENDetect register to see if the receiver chip is ready for further handshaking. When RxSENDetect is asserted, start reading EDID data through DDC channels and carry on the rest of the handshaking subsequently.

If the micro-controller makes no use of the interrupt signal as well as the above-mentioned status registers, the link establishment might fail. Please do follow the suggested initialization flow recommended in CAT6612 Programming Guide.

Configuration and Function Control

CAT6612 includes two serial programming ports by default (i.e. with embedded HDCP keys): one for interfacing with micro-controller, the other for accessing the DDC channels of HDMI link. If the customer elects to use CAT6612 with external HDCP keys, there's an additional serial programming port for interfacing with the HDCP ROM.

The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 43) and PCSDA (Pin 44). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 41). If PCADR is pulled high by the user, the device address is **0x9A**. If pulled low, **0x98**.

The I^2C interface for accessing the DDC channels of the HDMI link is a master interface, comprising DDCSCL (Pin 20) and DDCSDA (Pin 19). CAT6612 uses this interface to read the EDID data and perform HDCP authentication protocol with the sink device over the HDMI cable.

For temporarily storing the acquired EDID data, CAT6612 includes a 32 bytes dedicated FIFO. The micro-controller may command CAT6612 to acquire 32 bytes of EDID information, read it back and then continue to read the next 32 bytes until getting all neccessary EDID informations.

The HDCP protocol of CAT6612 is completely implemented in hardware. No software intervention is needed except for revocation list checking. Various HDCP-related statuses are stored in HDCP registers for the reference of micro-controller. Refer to CAT6612 Programming Guide for detailed register descriptions. The HDCP Standard also specifies a special message read protocol other than the standard I^2C protocol. See Figure 4 for checking HDCP port link integrity.

S	Slave Addr (7)	R	A	Read Data (8)	A	Read Data (8)	A	Read Data (8)	NA	P

S=Start; R=Read; A=Ack; NA=No Ack; P=Stop

Figure 4. HDCP port link integrity message read

Shall the user opt to purchase CAT6612 with external HDCP ROM, Pin 72 (ROMSCL) and Pin 71 (ROMSDA) form the third serial programming port and interface with the external HDCP ROM. This interface is a master one.

All serial programming interfaces conform to standard I^2C transactions and operate at up to 100kHz.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	-0.3		2.5	V
OVDD	I/O pins supply voltage	-0.3		4.0	V
AVCC	HDMI analog frontend supply voltage	-0.3		4.0	V
PVCC1	HDMI core PLL supply voltage	-0.3		4.0	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	1.71	1.8	1.89	V
OVDD	I/O pins supply voltage	2.97	3.3	3.63	V
AVCC	HDMI analog frontend supply voltage	3.135	3.3	3.465	V
PVCC1	HDMI core PLL supply voltage	3.135	3.3	3.465	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance			40	°C/W

Notes:
1. AVCC and PVCC1 should be regulated.
2. See System Design Consideration at page 24 for supply decoupling and regulation.

Operation Supply Current Specification

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{IVDD_OP}	IVDD current under normal operation	HDMI-1	21.0	22.5	mA
		HDMI-2	46.1	48.6	mA
		HDMI-3	80.9	86.0	mA
I_{OVDD_OP}	OVDD current under normal operation	HDMI-1	0.16	0.45	mA
		HDMI-2	0.10	0.47	mA
		HDMI-3	0.06	0.49	mA
I_{AVCC_OP}	AVCC current under normal operation	HDMI-1	8.6	9.5	mA
		HDMI-2	15.0	17.0	mA
		HDMI-3	26.0	29.0	mA
I_{PVCC1_OP}	PVCC1 current under normal operation	HDMI-1	1.7	1.9	mA
		HDMI-2	4.3	4.6	mA
		HDMI-3	8.8	9.4	mA
PW_{TOTAL_OP}	Total power consumption under normal operation[3]	HDMI-1	72	87	mW
		HDMI-2	147	176	mW
		HDMI-3	261	310	mW

Notes:

1. Typ: OVDD=AVCC=PVCC1= 3.3V, IVDD=1.8V
   Max: OVDD=AVCC=PVCC1= 3.6V, IVDD=1.98V
2. HDMI-1: 480p with 2-channel audio, PCLK=27MHz
   HDMI-2: 720p/1080i with 2-channel audio, PCLK=74.25MHz
   HDMI-3: 1080p with 2-channel audio, PCLK=148.5MHz
3. PW_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Conditions	Min.	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL		2.0			V
V_{IL}	Input low voltage[1]	LVTTL				0.8	V
V_T	Switching threshold[1]	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt			1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL	I_{OL}=2~16mA			0.4	
V_{OH}	Output high voltage[1]	LVTTL	I_{OH}=-2~-16mA	2.4			
I_{IN}	Input leakage current[1]	all	V_{IN}=5.5V or 0		±5		μA
I_{OZ}	Tri-state output leakage current[1]	all	V_{IN}=5.5V or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	Schmitt	V_{OUT}=0.2V	4		16	mA
V_{swing}	TMDS output single-ended swing[3]	TMDS	R_{LOAD}=50Ω V_{LOAD}=3.3V R_{EXT}=475Ω	400		600	mA
V_{OHTMDS}	TMDS output high voltage[3]	TMDS		V_{LOAD} -10mV		V_{LOAD}+ 10mV	V
I_{OFF}	Single-ended standby output current[3]	TMDS	V_{OUT}=0			10	μA

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of CAT6612 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to CAT6612 Programming Guide for proper register setting.
3. Limits defined by HDMI 1.2 standard

Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 2 channels	32		192	kHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	kHz

Video AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
T_{pixel}	PCLK pixel clock period[1]	Single-edged clocking	6.06		40	ns
F_{pixel}	PCLK pixel clock frequency[1]		25		165	MHz
T_{CDE}	PCLK dual-edged clock period[2]	Dual-edged clocking	13.47		40	ns
F_{CDE}	PCLK dual-edged clock frequency[2]		25		74.25	MHz
T_{PDUTY}	PCLK clock duty cycle		40%		60%	
T_{PJ}	PCLK worst-case jitter				2.0	ns
T_S	Video data setup time[3]	Single-edged clocking	1.5			ns
T_H	Video data hold time[3]		0.7			ns
T_{SDE}	Video data setup time[3]	Dual-edged clocking	1.5			ns
T_{HDE}	Video data hold time[3]		0.7			ns

Notes:

1. Fpixel is the inverse of Tpixel. Operating frequency range is given here while the actual video clock frequency should comply with all video timing standards. Refer to Table 1 for supported video timings and corresponding pixel frequencies.
2. 12-bit dual-edged clocking is supported up to 74.5MHz of PCLK frequency, which covers 720p/1080i.
3. All setup time and hold time specifications are with respect to the latching edge of PCLK selected by the user through register programming.

Video Data Bus Mappings

CAT6612 supports various input data mappings and formats, including those with embedded control signals only. Corresponding register setting is mandatory for any chosen input data mappings. Refer to CAT6612 Programming Guide for detailed instruction.

Color Space	Video Format	Input Channels	Bus Width	H/Vsync	Clocking	Table
RGB	4:4:4	3	24	Seperate	1X	3
		1	12	Seperate	Dual-edged	8
YCbCr	4:4:4	3	24	Seperate	1X	3
		1	12	Seperate	Dual-edged	8
	4:2:2	2	16/20/24	Seperate	1X	4
				Embedded	1X	5
		1	8/10/12	Seperate	2X	7
				Embedded	2X	6

Table 2. Input video format supported by CAT6612

With certain input formats, not all 24 data input pins are used. In that case, it is recommended to tie the unused input pins to ground.

RGB 4:4:4 and YCbCr 4:4:4, 24 Bits with Separate Syncs

These are the simpliest formats, with a complete definition of every pixel in each clock period. Timing diagram is depicted in Fig. 5 in the example of RGB. The timing of YCbCr 4:4:4 follow suits.

Pin Name	RGB	YCbCr
D0	B0	Cb0
D1	B1	Cb1
D2	B2	Cb2
D3	B3	Cb3
D4	B4	Cb4
D5	B5	Cb5
D6	B6	Cb6
D7	B7	Cb7
D8	G0	Y0
D9	G1	Y1
D10	G2	Y2
D11	G3	Y3
D12	G4	Y4
D13	G5	Y5
D14	G6	Y6
D15	G7	Y7
D16	R0	Cr0
D17	R1	Cr1
D18	R2	Cr2
D19	R3	Cr3
D20	R4	Cr4
D21	R5	Cr5
D22	R6	Cr6
D23	R7	Cr7
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

Table 3. RGB & YCbCr 4:4:4 Mappings

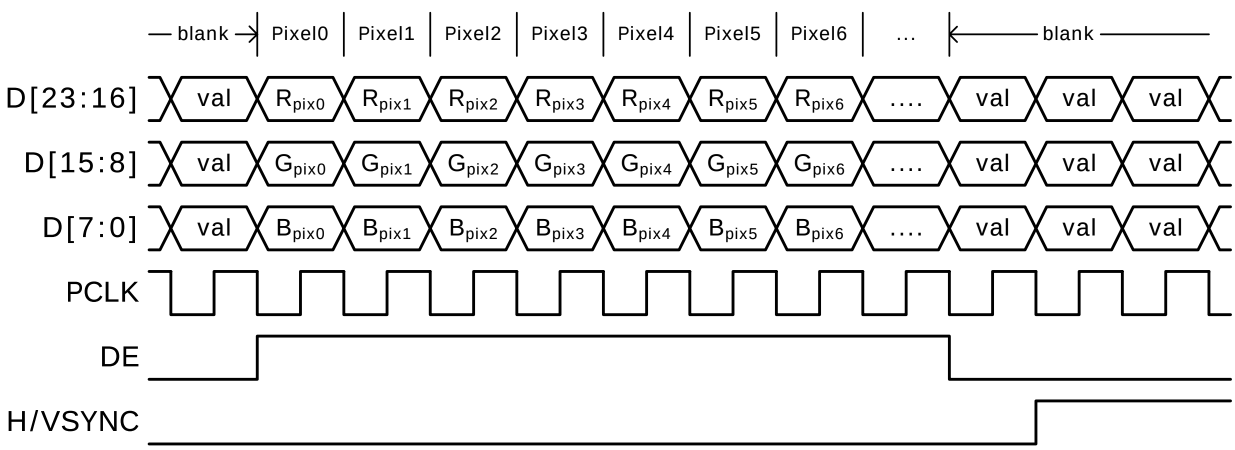


Figure 5. RGB 4:4:4 Timing Diagram

YCbCr 4:2:2 with Separate Syncs

YCbCr 4:2:2 format does not have one complete pixel for every clock period. Luminace channel (Y) is given for every pixel, while the two chroma channels are given alternatively on every other clock period. The average bit amount of Y is twice that of Cb or Cr. Depending on the bus width, each component could take on different lengths. The DE period should contain an even number of clock periods. Figure 6 gives a timing example of 16-bit YCbCr 4:2:2. The 20-bit and 24-bit versions are similar.

	YCbCr 4:2:2 16-bit		YCbCr 4:2:2 20-bit		YCbCr 4:2:2 24-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
D0	grounded	grounded	grounded	grounded	Y0	Y0
D1	grounded	grounded	grounded	grounded	Y1	Y1
D2	grounded	grounded	Y0	Y0	Y2	Y2
D3	grounded	grounded	Y1	Y1	Y3	Y3
D4	grounded	grounded	grounded	grounded	Cb0	Cr0
D5	grounded	grounded	grounded	grounded	Cb1	Cr1
D6	grounded	grounded	Cb0	Cr0	Cb2	Cr2
D7	grounded	grounded	Cb1	Cr1	Cb3	Cr3
D8	Y0	Y0	Y2	Y2	Y4	Y4
D9	Y1	Y1	Y3	Y3	Y5	Y5
D10	Y2	Y2	Y4	Y4	Y6	Y6
D11	Y3	Y3	Y5	Y5	Y7	Y7
D12	Y4	Y4	Y6	Y6	Y8	Y8
D13	Y5	Y5	Y7	Y7	Y9	Y9
D14	Y6	Y6	Y8	Y8	Y10	Y10
D15	Y7	Y7	Y9	Y9	Y11	Y11
D16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D22	Cb6	Cr6	Cb8	Cb8	Cb10	Cr10
D23	Cb7	Cr7	Cb9	Cb9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 4. Mappings of YCbCr 4:2:2 with separate syncs

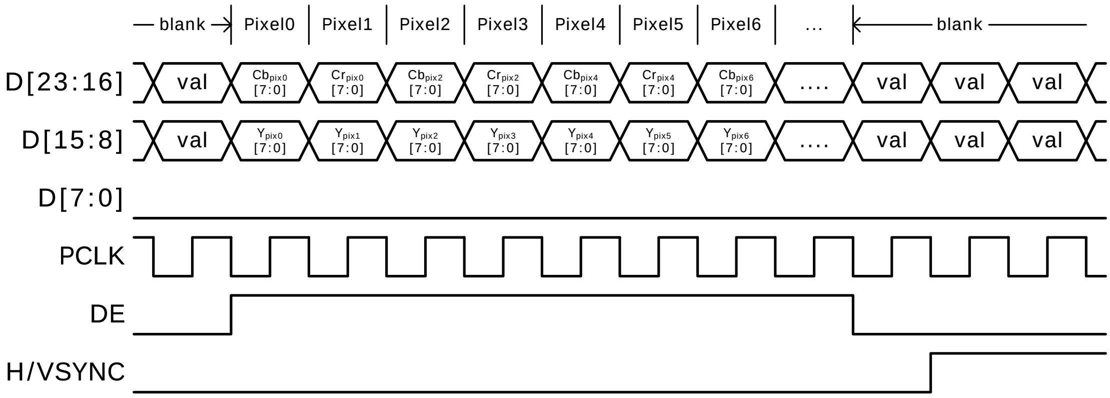


Figure 6. 16-bit YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 with Embedded Syncs

This is similar to the previous format. The only difference is that the syncs are embedded. Bus width could be 16-bit, 20-bit or 24-bit. Figure 7 gives a timing example of 16-bit YCbCr 4:2:2. The 20-bit and 24-bit versions are similar.

	YCbCr 4:2:2 16-bit		YCbCr 4:2:2 20-bit		YCbCr 4:2:2 24-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
D0	grounded	grounded	grounded	grounded	Y0	Y0
D1	grounded	grounded	grounded	grounded	Y1	Y1
D2	grounded	grounded	Y0	Y0	Y2	Y2
D3	grounded	grounded	Y1	Y1	Y3	Y3
D4	grounded	grounded	grounded	grounded	Cb0	Cr0
D5	grounded	grounded	grounded	grounded	Cb1	Cr1
D6	grounded	grounded	Cb0	Cr0	Cb2	Cr2
D7	grounded	grounded	Cb1	Cr1	Cb3	Cr3
D8	Y0	Y0	Y2	Y2	Y4	Y4
D9	Y1	Y1	Y3	Y3	Y5	Y5
D10	Y2	Y2	Y4	Y4	Y6	Y6
D11	Y3	Y3	Y5	Y5	Y7	Y7
D12	Y4	Y4	Y6	Y6	Y8	Y8
D13	Y5	Y5	Y7	Y7	Y9	Y9
D14	Y6	Y6	Y8	Y8	Y10	Y10
D15	Y7	Y7	Y9	Y9	Y11	Y11
D16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D22	Cb6	Cr6	Cb8	Cb8	Cb10	Cr10
D23	Cb7	Cr7	Cb9	Cb9	Cb11	Cr11
HSYNC	grounded	grounded	grounded	grounded	grounded	grounded
VSYNC	grounded	grounded	grounded	grounded	grounded	grounded
DE	grounded	grounded	grounded	grounded	grounded	grounded

Table 5. Mappings of YCbCr 4:2:2 with embedded syncs

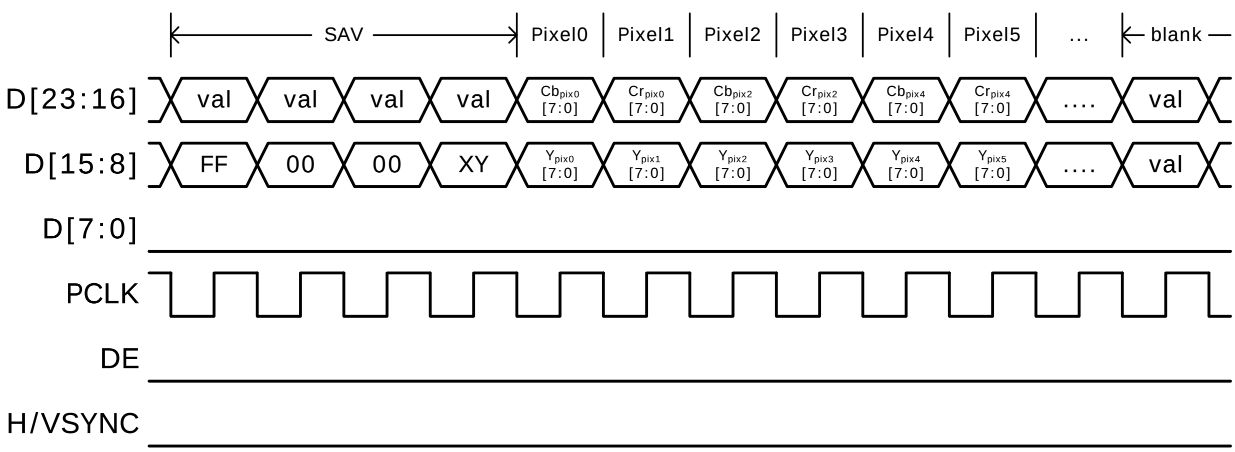


Figure 7. 16-bit YCbCr 4:2:2 with embedded syncs

CCIR-656 Format

The CCIR-656 format is yet another variation of the YCbCr formats. The bus width is further reduced by half compared from the previous YCbCr 4:2:2 formats, to either 8-bit, 10-bit or 12-bit. To compensate for the halving of data bus, PCLK is doubled. With the double-rate input clock, luminance channel (Y) and chroma channels (Cb or Cr) are alternated. CAT6612 supports CCIR-656 format of up to 720p or 1080i, with the doubled-rate clock running at 148.5MHz. CCIR-656 format supports embedded syncs only. Figure 8 gives an example of 8-bit CCIR-656. 10-bit and 12-bit versions are similar.

	CCIR-656 8-bit		CCIR-656 10-bit		CCIR-656 12-bit	
Pin Name	1st PCLK	2nd PCLK	1st PCLK	2nd PCLK	Pixel#2N	Pixel#2N+1
D0	grounded	grounded	grounded	grounded	C0	Y0
D1	grounded	grounded	grounded	grounded	C1	Y1
D2	grounded	grounded	C0	Y0	C2	Y2
D3	grounded	grounded	C1	Y1	C3	Y3
D4	grounded	grounded	grounded	grounded	grounded	grounded
D5	grounded	grounded	grounded	grounded	grounded	grounded
D6	grounded	grounded	grounded	grounded	grounded	grounded
D7	grounded	grounded	grounded	grounded	grounded	grounded
D8	C0	Y0	C2	Y2	C4	Y4
D9	C1	Y1	C3	Y3	C5	Y5
D10	C2	Y2	C4	Y4	C6	Y6
D11	C3	Y3	C5	Y5	C7	Y7
D12	C4	Y4	C6	Y6	C8	Y9
D13	C5	Y5	C7	Y7	C9	Y9
D14	C6	Y6	C8	Y8	C10	Y10
D15	C7	Y7	C9	Y9	C11	Y11
D16	grounded	grounded	grounded	grounded	grounded	grounded
D17	grounded	grounded	grounded	grounded	grounded	grounded
D18	grounded	grounded	grounded	grounded	grounded	grounded
D19	grounded	grounded	grounded	grounded	grounded	grounded
D20	grounded	grounded	grounded	grounded	grounded	grounded
D21	grounded	grounded	grounded	grounded	grounded	grounded
D22	grounded	grounded	grounded	grounded	grounded	grounded
D23	grounded	grounded	grounded	grounded	grounded	grounded
HSYNC	grounded	grounded	grounded	grounded	grounded	grounded
VSYNC	grounded	grounded	grounded	grounded	grounded	grounded
DE	grounded	grounded	grounded	grounded	grounded	grounded

Table 6. Mappings of CCIR-656

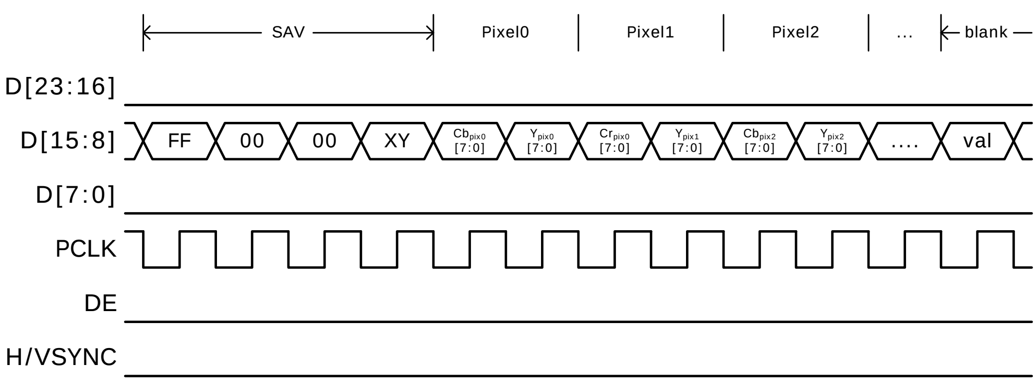


Figure 8. 8-bit CCIR-656

CCIR-656 + separate syncs

This format is not specified by CCIR-656. It's simply the previously mentioned CCIR-656 format plus separate syncs.

	CCIR-656 8-bit		CCIR-656 10-bit		CCIR-656 12-bit	
Pin Name	1st PCLK	2nd PCLK	1st PCLK	2nd PCLK	Pixel#2N	Pixel#2N+1
D0	grounded	grounded	grounded	grounded	C0	Y0
D1	grounded	grounded	grounded	grounded	C1	Y1
D2	grounded	grounded	C0	Y0	C2	Y2
D3	grounded	grounded	C1	Y1	C3	Y3
D4	grounded	grounded	grounded	grounded	grounded	grounded
D5	grounded	grounded	grounded	grounded	grounded	grounded
D6	grounded	grounded	grounded	grounded	grounded	grounded
D7	grounded	grounded	grounded	grounded	grounded	grounded
D8	C0	Y0	C2	Y2	C4	Y4
D9	C1	Y1	C3	Y3	C5	Y5
D10	C2	Y2	C4	Y4	C6	Y6
D11	C3	Y3	C5	Y5	C7	Y7
D12	C4	Y4	C6	Y6	C8	Y9
D13	C5	Y5	C7	Y7	C9	Y9
D14	C6	Y6	C8	Y8	C10	Y10
D15	C7	Y7	C9	Y9	C11	Y11
D16	grounded	grounded	grounded	grounded	grounded	grounded
D17	grounded	grounded	grounded	grounded	grounded	grounded
D18	grounded	grounded	grounded	grounded	grounded	grounded
D19	grounded	grounded	grounded	grounded	grounded	grounded
D20	grounded	grounded	grounded	grounded	grounded	grounded
D21	grounded	grounded	grounded	grounded	grounded	grounded
D22	grounded	grounded	grounded	grounded	grounded	grounded
D23	grounded	grounded	grounded	grounded	grounded	grounded
HSYNC	HSYNC		HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC		VSYNC	
DE	DE		DE		DE	

Table 7. Mappings of CCIR-656 + separate syncs

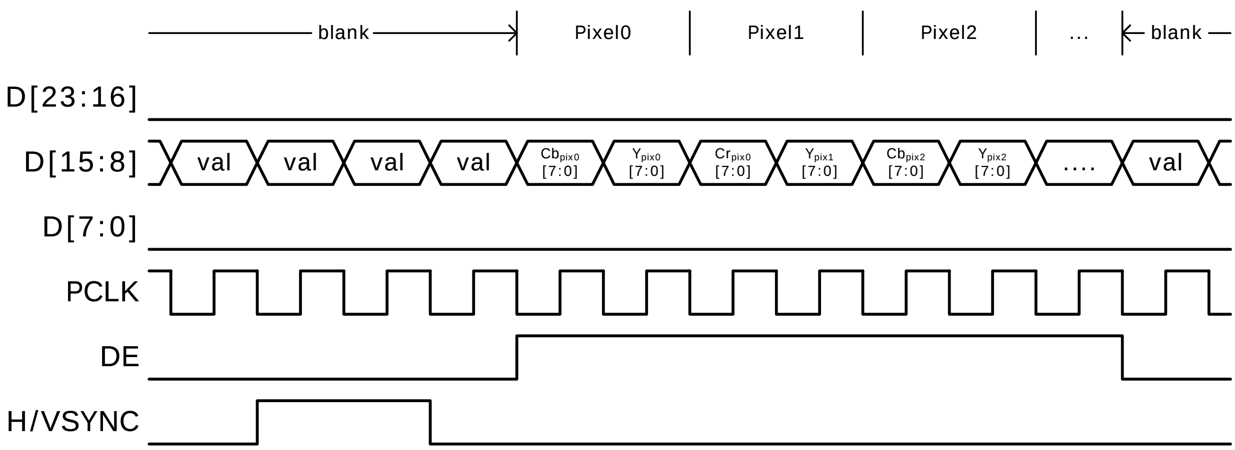


Figure 9. 8-bit CCIR-656 + separate syncs

12-bit RGB and YCbCr 4:4:4 Using Dual-Edge Triggering

This format is not specified by CCIR-656. It's simply the previously mentioned CCIR-656 format plus separate syncs.

	RGB		YCbCr	
Pin Name	1st edge	2nd edge	1st edge	2nd edge
D0	B0	G4	Cb0	Y4
D1	B1	G5	Cb1	Y5
D2	B2	G6	Cb2	Y6
D3	B3	G7	Cb3	Y7
D4	B4	R0	Cb4	Cr0
D5	B5	R1	Cb5	Cr1
D6	B6	R2	Cb6	Cr2
D7	B7	R3	Cb7	Cr3
D8	G0	R4	Y0	Cr4
D9	G1	R5	Y1	Cr5
D10	G2	R6	Y2	Cr6
D11	G3	R7	Y3	Cr7
D12	grounded	grounded	grounded	grounded
D13	grounded	grounded	grounded	grounded
D14	grounded	grounded	grounded	grounded
D15	grounded	grounded	grounded	grounded
D16	grounded	grounded	grounded	grounded
D17	grounded	grounded	grounded	grounded
D18	grounded	grounded	grounded	grounded
D19	grounded	grounded	grounded	grounded
D20	grounded	grounded	grounded	grounded
D21	grounded	grounded	grounded	grounded
D22	grounded	grounded	grounded	grounded
D23	grounded	grounded	grounded	grounded
HSYNC	HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC	
DE	DE		DE	

Table 8. Mappings of 12-bit 4:4:4 dual-edge triggered

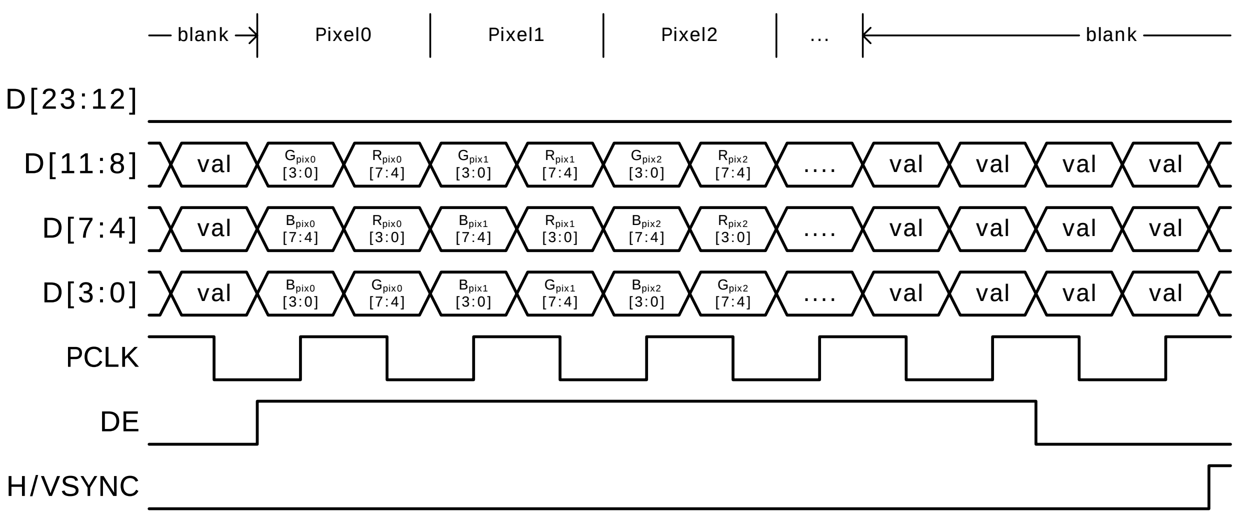


Figure 10. 12-bit RGB 4:4:4 dual-edge triggered

System Design Consideration

To get the optimum performance of CAT6612, the system designers should follow the guideline below when designing the application circuits and PCB layout.

1. Pin 23 (PVCC1) should be supplied with clean power: ferrite-decoupled and capacitively- bypassed, since this is the power for the transmitter PLL, which is crucial in determining the TMDS output signal quality . Excess power noise might degrade the system performance.

2. The characteristic impedance of all differential PCB traces (TX2P/M, TX1P/M, TX0P/M, TXCP/M) should be kept 100Ω all the way from the HDMI connector to CAT6612. This is very crucial to the system performance at high speeds. When layouting these 4 differential transmission lines (8 single-ended lines in total), the following guidelines should be followed:

A. The signals traces should be on the outside layers (e.g. TOP layer) while beneath it there should be a continuous ground plane in order to maintain the called micro-strip structure, giving stable and well-defined characteristic impedances.
B. Cornering, through holes, crossing and any irregular signal routing should be avoided so as to prevent from disrupting the EM field and creating discontinuity in characteristic impedance.
C. CAT6612 should be placed as close to the HDMI connector as possible. Since the TMDS signal pins of CAT6612 perfectly match the order of the connector pins, it is very convenient to route the signal directly into the chip, without through holes or angling.
D. Carefully choose the width and spacing of the differential transmission lines as their characteristic impedance depends on various parameters of the PCB: trace width, trace spacing, copper thickness, dielectric constant, dielectric thickness, etc. Careful 3D EM simulation is the best way to derive a correct dimension that enables a nominal 100Ω differential impedance. Please contact us directly for technical support of this issue.

3. Special care should be taken when adding discrete ESD devices to all differential PCB traces (TX2P/M, TX1P/M, TX0P/M, TXCP/M). CAT6612 is designed to provide ESD protection for up to 2kV at these pins. Adding discrete ESD diodes could enhance the ESD capability, but at the same time will inevitably add capacitive loads, therefore degrade the electrical performance at high speeds. If not chosen carefully, these diodes coupled with less-than-optimal layout could prevent the system from passing the SOURCE TMDS Data Eye Diagram test in the HDMI Compliance Test (Test ID 7-10). Besides, most general-purpose ESD diodes are relatively large in size, forcing the high-speed differential lines to corner several times and therefore introducing severe reflection. Carefully choosing an ESD diode that's designed for HDMI signalling could lead to a minimum loading as well as an optimized layout. Commercially available devices such as Semtech's RClamp0524p that take into consideration of all aspects are recommended.

(http://www.semtech.com/products/product-detail.jsp?navId=H0,C2,C222,P3028).

An layout example is shown in Fig. 11, with referenced FR4 PCB structure included. Note that the ESD diodes should be placed as close to the HDMI connectors as possible to yield the best ESD performances..

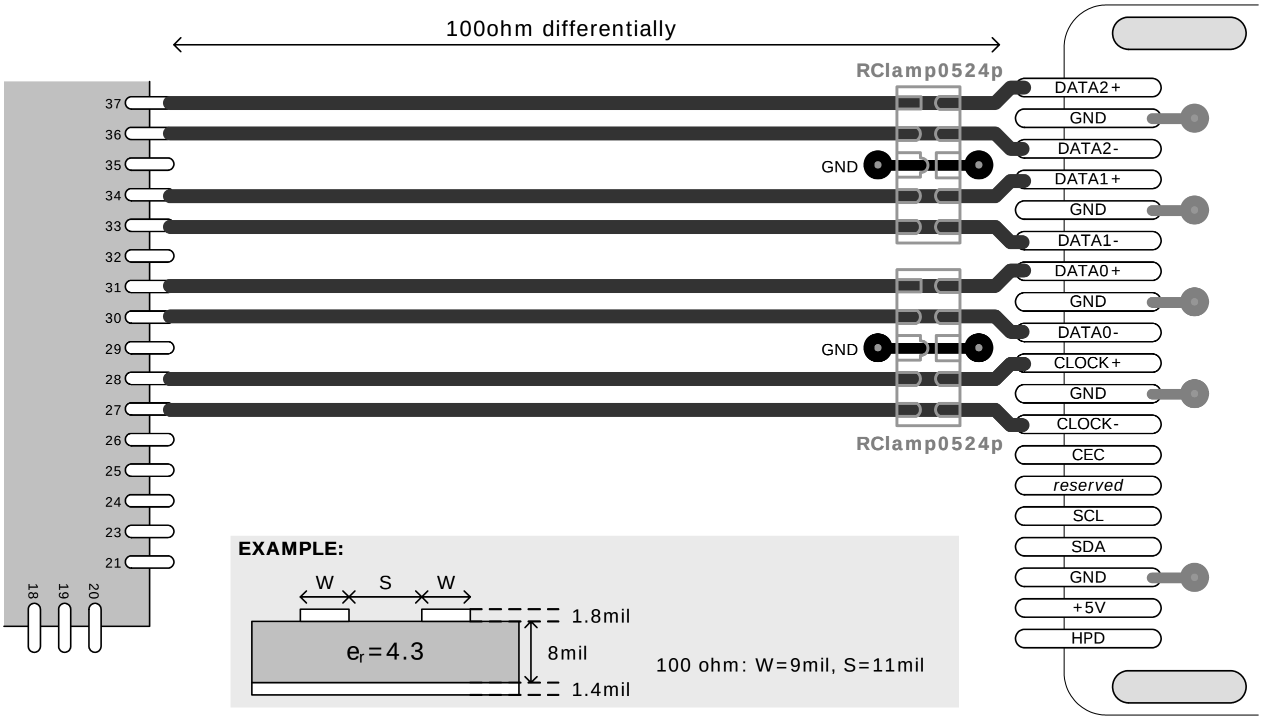
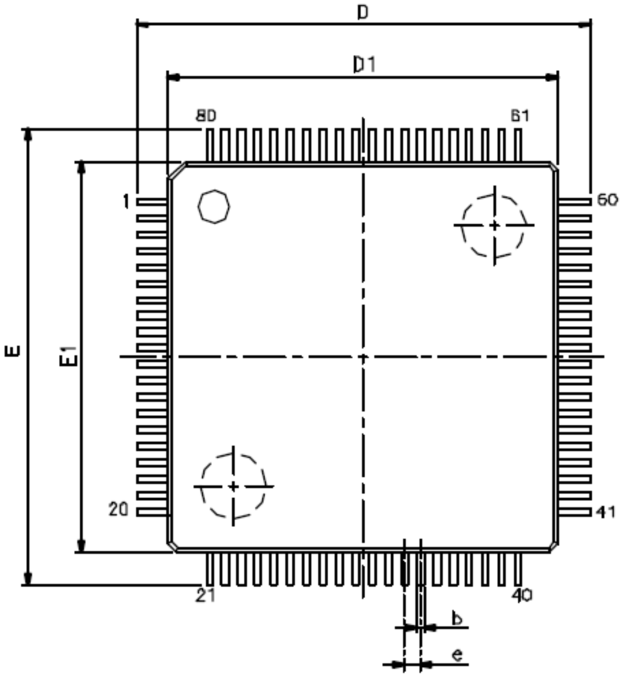
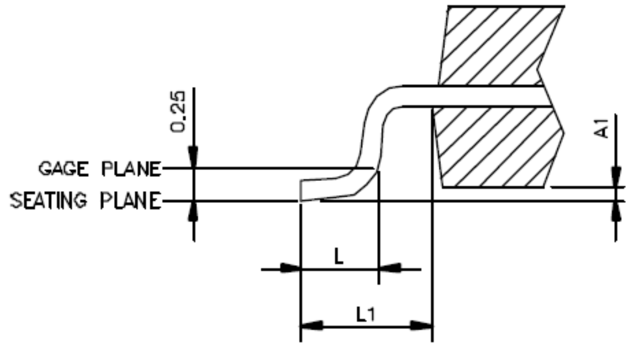


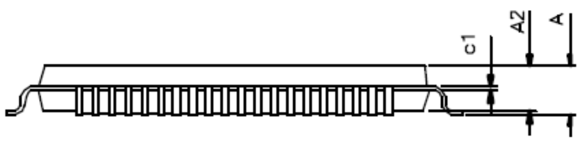
Figure 11. PCB layout example for high-speed transmission lines with RClamp0524p

4. <u>Pin 24 (REXT) should be connected to AVCC via a 476Ω/1% precision SMD resistor.</u> This resistor is used to calibrate the TMDS output current level to the nominal value of 10mA. The resistor should be placed as close to CAT6612 as possible.

Package Dimensions







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

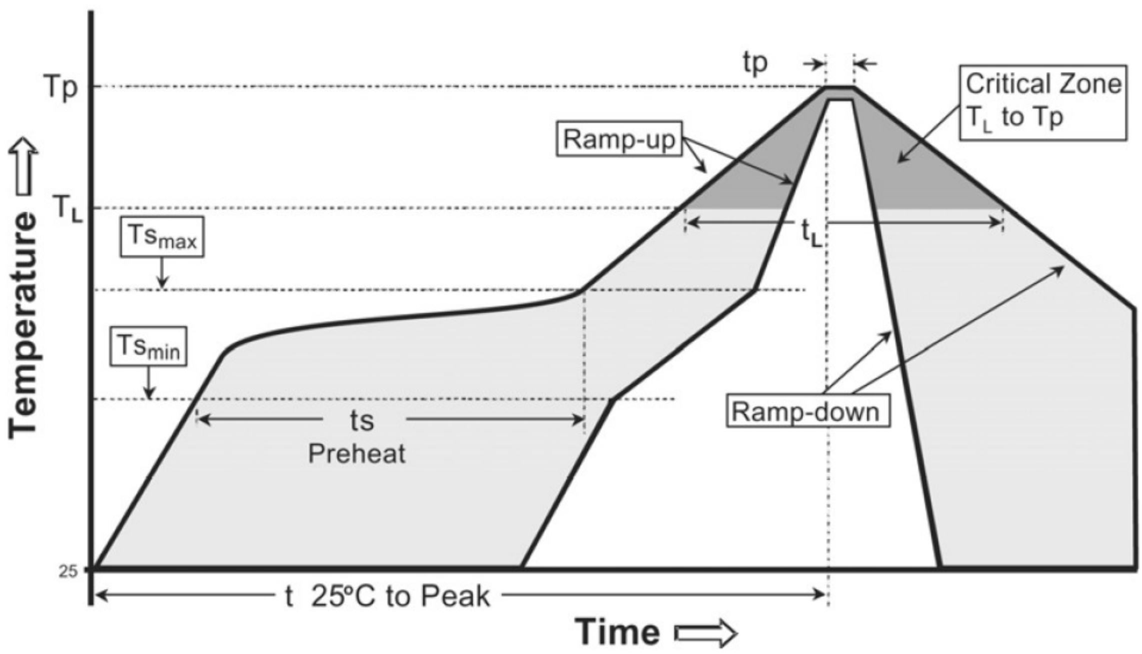
SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	14 BSC	
D1	12 BSC	
E	14 BSC	
E1	12 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

Figure 13. 80-pin LQFP Package Dimensions

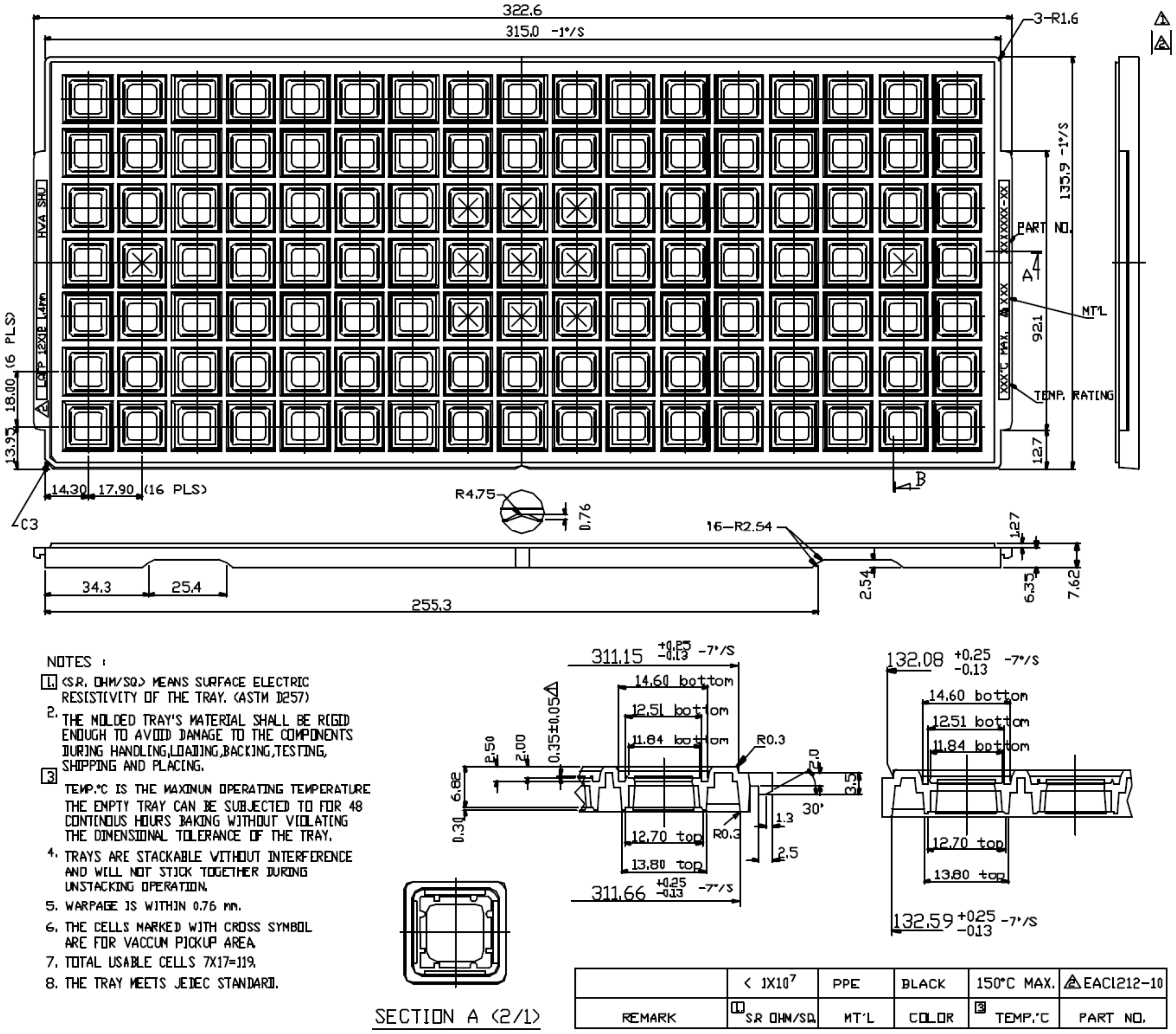
Classification Reflow Profiles

Reflow Profile	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0 /-5℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.



Carrier Tray Dimensions



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