

### VR5500™

## 64-/32-BIT MICROPROCESSOR

### DESCRIPTION

The  $\mu$ PD30550 (VR5500) is a member of the VR Series™ of RISC (Reduced Instruction Set Computer) microprocessors. It is a high-performance 64-/32-bit microprocessor that employs the RISC architecture developed by MIPS™.

The VR5500 allows selection of a 64-bit or 32-bit bus width for the system interface, and can operate using protocols compatible with the VR5000 Series™ and VR5432™.

**Detailed function descriptions are provided in the • VR5500 User's Manual (U16044E) user's manual. Be sure to read the manual before designing.**

### FEATURES

- MIPS 64-bit RISC architecture
- High-speed operation processing
  - Two-way superscaler super pipeline
  - 300 MHz product: 603 MIPS
  - 400 MHz product: 804 MIPS
- High-speed translation lookaside buffer (TLB) (48 entries)
- Address space
  - Physical: 36 bits (64-bit bus selected)  
32 bits (32-bit bus selected)
  - Virtual: 40 bits (in 64-bit mode)  
31 bits (in 32-bit mode)
- On-chip floating-point unit (FPU)
  - Supports sum-of-products instructions
- On-chip primary cache memory (instruction/data: 32 KB each)
  - 2-way set associative
  - Supports line lock feature
- 64-/32-bit address/data multiplexed bus
  - Bus width selectable during reset
  - Bus protocol compatibility with existing products retained
- Maximum operating frequency
  - 300 MHz product: Internal 300 MHz, external 133 MHz
  - 400 MHz product: Internal 400 MHz, external 133 MHz
- External/internal multiplication factor selectable from  $\times 2$  to  $\times 5.5$  by increments of .5
- Conforms to MIPS I, II, III, IV and MIPS64 instruction sets. Instruction set extensions supported include product-sum operation instruction, rotate instruction, register scan instruction, and instruction for low power mode.
- Hardware debug functions supported are N-Wire and JTAG.
- Supply voltage
 

Core block:	1.5 V $\pm 5\%$ (300 MHz product)
	1.6 to 1.7 V (400 MHz product)
I/O block:	3.3 V $\pm 5\%$ , 2.5 V $\pm 5\%$

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**APPLICATIONS**

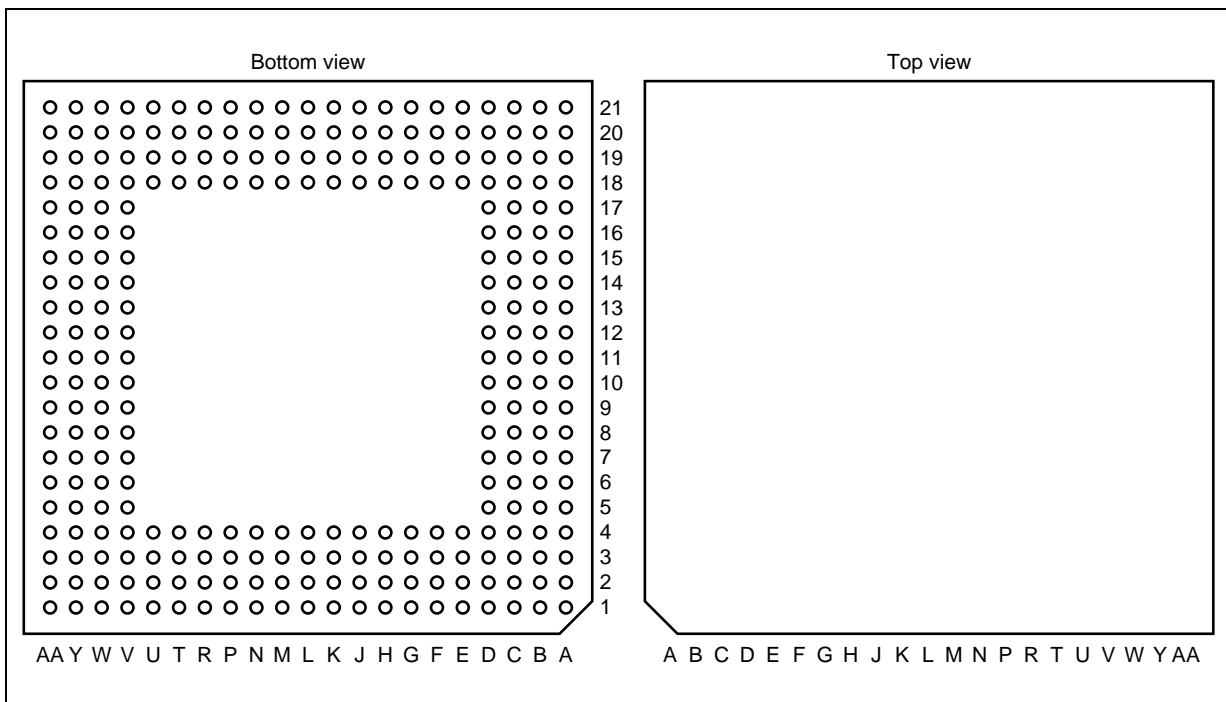
- Set-topboxes
- RAID
- High-end embedded devices, etc.

**ORDERING INFORMATION**

Part Number	Package	Maximum Operating Frequency (MHz)
μPD30550F2-300-NN1	272-pin plastic BGA (C/D advanced type) (29 × 29)	300
μPD30550F2-400-NN1	272-pin plastic BGA (C/D advanced type) (29 × 29)	400

**PIN CONFIGURATION**

- 272-pin plastic BGA (C/D advanced type) (29 × 29)  
 μPD30550F2-300-NN1  
 μPD30550F2-400-NN1



(1/2)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
A1	V <sub>SS</sub>	B17	SysAD27	D12	V <sub>SS</sub>	H4	V <sub>DD</sub>
A2	V <sub>SS</sub>	B18	V <sub>DD</sub> I/O	D13	SysAD31	H18	V <sub>SS</sub>
A3	V <sub>DD</sub> I/O	B19	V <sub>DD</sub> I/O	D14	V <sub>DD</sub>	H19	V <sub>SS</sub>
A4	V <sub>DD</sub> I/O	B20	V <sub>SS</sub>	D15	SysAD60	H20	V <sub>SS</sub>
A5	Reset#	B21	V <sub>SS</sub>	D16	V <sub>SS</sub>	H21	SysAD21
A6	PReq#	C1	V <sub>DD</sub> I/O	D17	SysAD26	J1	SysCmd7
A7	ValidIn#	C2	V <sub>DD</sub> I/O	D18	V <sub>SS</sub>	J2	SysCmd8
A8	ValidOut#	C3	V <sub>SS</sub>	D19	V <sub>SS</sub>	J3	TIntSel
A9	V <sub>SS</sub>	C4	V <sub>SS</sub>	D20	V <sub>DD</sub> I/O	J4	Int0#
A10	SysADC7	C5	V <sub>SS</sub>	D21	V <sub>DD</sub> I/O	J18	SysAD52
A11	SysADC3	C6	V <sub>DD</sub>	E1	SysCmd0	J19	SysAD20
A12	SysADC1	C7	WrRdy#	E2	DisDValidO#	J20	SysAD51
A13	SysADC4	C8	V <sub>SS</sub>	E3	DWBTrans#	J21	SysAD19
A14	SysAD62	C9	SysID1	E4	O3Return#	K1	Int1#
A15	SysAD30	C10	V <sub>DD</sub>	E18	SysAD57	K2	V <sub>SS</sub>
A16	SysAD28	C11	SysADC2	E19	SysAD25	K3	V <sub>SS</sub>
A17	SysAD59	C12	V <sub>SS</sub>	E20	SysAD56	K4	V <sub>SS</sub>
A18	V <sub>DD</sub> I/O	C13	SysAD63	E21	SysAD24	K18	V <sub>DD</sub>
A19	V <sub>DD</sub> I/O	C14	V <sub>DD</sub>	F1	SysCmd1	K19	V <sub>DD</sub>
A20	V <sub>SS</sub>	C15	SysAD29	F2	V <sub>SS</sub>	K20	V <sub>DD</sub>
A21	V <sub>SS</sub>	C16	V <sub>SS</sub>	F3	V <sub>SS</sub>	K21	V <sub>DD</sub>
B1	V <sub>SS</sub>	C17	SysAD58	F4	V <sub>SS</sub>	L1	Int2#
B2	V <sub>SS</sub>	C18	V <sub>DD</sub> I/O	F18	V <sub>DD</sub>	L2	Int3#
B3	V <sub>DD</sub> I/O	C19	V <sub>SS</sub>	F19	V <sub>DD</sub>	L3	Int4#
B4	V <sub>DD</sub> I/O	C20	V <sub>DD</sub> I/O	F20	V <sub>DD</sub>	L4	Int5#
B5	ColdReset#	C21	V <sub>DD</sub> I/O	F21	SysAD55	L18	SysAD17
B6	Release#	D1	V <sub>DD</sub> I/O	G1	SysCmd2	L19	SysAD49
B7	ExtRqst#	D2	V <sub>DD</sub> I/O	G2	SysCmd3	L20	SysAD18
B8	BusMode	D3	V <sub>SS</sub>	G3	SysCmd4	L21	SysAD50
B9	SysID2	D4	V <sub>SS</sub>	G4	SysCmd5	M1	RMode#/BKTGIO#
B10	V <sub>DD</sub>	D5	IC	G18	SysAD23	M2	V <sub>DD</sub>
B11	SysADC6	D6	V <sub>DD</sub>	G19	SysAD54	M3	V <sub>DD</sub>
B12	V <sub>SS</sub>	D7	RdRdy#	G20	SysAD22	M4	V <sub>DD</sub>
B13	SysADC0	D8	V <sub>SS</sub>	G21	SysAD53	M18	V <sub>SS</sub>
B14	V <sub>DD</sub>	D9	SysID0	H1	SysCmd6	M19	V <sub>SS</sub>
B15	SysAD61	D10	V <sub>DD</sub>	H2	V <sub>DD</sub>	M20	V <sub>SS</sub>
B16	V <sub>SS</sub>	D11	SysADC5	H3	V <sub>DD</sub>	M21	V <sub>SS</sub>

**Caution** Leave the IC pin open.

**Remark** # indicates active low.

(2/2)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
N1	V <sub>DD</sub> I/O	T21	SysAD12	W2	V <sub>DD</sub> I/O	Y12	V <sub>DD</sub>
N2	NMI#	U1	NTrcClk	W3	V <sub>SS</sub>	Y13	SysAD3
N3	V <sub>DD</sub> I/O	U2	NTrcData0	W4	V <sub>SS</sub>	Y14	V <sub>SS</sub>
N4	BigEndian	U3	NTrcData1	W5	V <sub>DD</sub> PA2	Y15	SysAD37
N18	SysAD15	U4	NTrcData3	W6	V <sub>SS</sub>	Y16	SysAD39
N19	SysAD47	U18	SysAD10	W7	V <sub>DD</sub> I/O	Y17	SysAD40
N20	SysAD16	U19	SysAD42	W8	V <sub>DD</sub>	Y18	V <sub>DD</sub> I/O
N21	SysAD48	U20	SysAD11	W9	JTDI	Y19	V <sub>DD</sub> I/O
P1	V <sub>SS</sub>	U21	SysAD43	W10	V <sub>SS</sub>	Y20	V <sub>SS</sub>
P2	V <sub>SS</sub>	V1	NTrcData2	W11	SysAD1	Y21	V <sub>SS</sub>
P3	V <sub>SS</sub>	V2	NTrcEnd	W12	V <sub>DD</sub>	AA1	V <sub>SS</sub>
P4	V <sub>SS</sub>	V3	V <sub>SS</sub>	W13	SysAD35	AA2	V <sub>SS</sub>
P18	V <sub>DD</sub>	V4	V <sub>SS</sub>	W14	V <sub>SS</sub>	AA3	V <sub>DD</sub> I/O
P19	V <sub>DD</sub>	V5	V <sub>SS</sub> PA2	W15	SysAD38	AA4	V <sub>DD</sub> I/O
P20	V <sub>DD</sub>	V6	V <sub>SS</sub>	W16	V <sub>DD</sub>	AA5	V <sub>DD</sub> PA1
P21	SysAD46	V7	V <sub>DD</sub> I/O	W17	SysAD9	AA6	V <sub>DD</sub> I/O
R1	DivMode0	V8	V <sub>DD</sub>	W18	V <sub>SS</sub>	AA7	IC
R2	DivMode1	V9	JTMS	W19	V <sub>SS</sub>	AA8	JTDO
R3	DivMode2	V10	V <sub>SS</sub>	W20	V <sub>DD</sub> I/O	AA9	DrvCon
R4	V <sub>DD</sub> I/O	V11	SysAD33	W21	V <sub>DD</sub> I/O	AA10	V <sub>SS</sub>
R18	SysAD44	V12	V <sub>DD</sub>	Y1	V <sub>SS</sub>	AA11	SysAD0
R19	SysAD13	V13	SysAD4	Y2	V <sub>SS</sub>	AA12	SysAD2
R20	SysAD45	V14	V <sub>SS</sub>	Y3	V <sub>DD</sub> I/O	AA13	SysAD34
R21	SysAD14	V15	SysAD7	Y4	V <sub>DD</sub> I/O	AA14	SysAD36
T1	V <sub>DD</sub>	V16	V <sub>DD</sub>	Y5	V <sub>SS</sub> PA1	AA15	SysAD5
T2	V <sub>DD</sub>	V17	SysAD41	Y6	SysClock	AA16	SysAD6
T3	V <sub>DD</sub>	V18	V <sub>SS</sub>	Y7	JTRST#	AA17	SysAD8
T4	V <sub>DD</sub>	V19	V <sub>SS</sub>	Y8	V <sub>DD</sub>	AA18	V <sub>DD</sub> I/O
T18	V <sub>SS</sub>	V20	V <sub>DD</sub> I/O	Y9	JTCK	AA19	V <sub>DD</sub> I/O
T19	V <sub>SS</sub>	V21	V <sub>DD</sub> I/O	Y10	V <sub>SS</sub>	AA20	V <sub>SS</sub>
T20	V <sub>SS</sub>	W1	V <sub>DD</sub> I/O	Y11	SysAD32	AA21	V <sub>SS</sub>

**Caution** Leave the IC pin open.

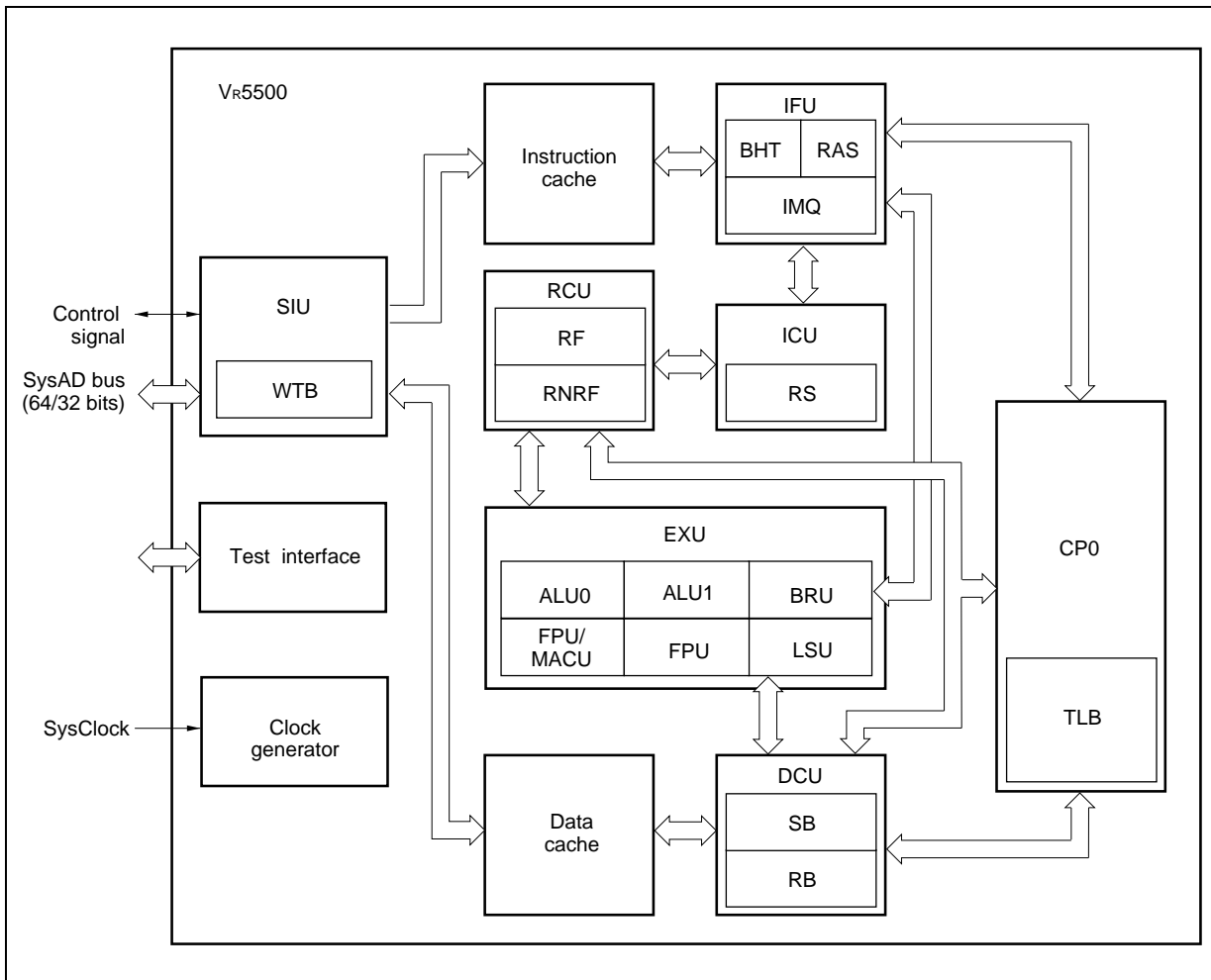
**Remarks** 1. # indicates active low.

**PIN NAMES**

BigEndian:	Big endian	PReq#:	Processor request
BKTGIO#:	Break/trigger input/output	RdRdy#:	Read ready
BusMode:	Bus mode	Release#:	Release
ColdReset#:	Cold reset	Reset#:	Reset
DisDValidO#:	Disable delay ValidOut#	SysAD(63:0):	System address/data bus
DivMode(2:0):	Divide mode	SysADC(7:0):	System address/data check bus
DrvCon:	Driver control	SysClock:	System clock
DWBTrans#:	Doubleword block transfer	SysCmd(8:0):	System command/data identifier bus
ExtRqst#:	External request	SysID(2:0):	System bus identifier
IC	Internally connected	TIntSel:	Timer interrupt selection
Int(5:0)#:	Interrupt	ValidIn#:	Valid input
JTCK:	JTAG clock	ValidOut#:	Valid output
JTDI:	JTAG data input	VDD:	Power supply for CPU core
JTDO:	JTAG data output	VDDIO:	Power supply for I/O
JTMS:	JTAG mode select	VDDPA1, VDDPA2:	Noise Sensitive VDD for PLL
JTRST#:	JTAG reset	Vss:	Ground
NMI#:	Non-maskable interrupt	VssPA1, VssPA2:	Noise Sensitive Vss for PLL
NTrcClk:	N-Trace clock	WrRdy#:	Write ready
NTrcData(3:0) :	N-Trace data output		
NTrcEnd:	N-Trace end		
O3Return#:	Out-of-Order Return mode		

**Remark** # indicates active low.

INTERNAL BLOCK DIAGRAM



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1. PIN FUNCTIONS

Remark # indicates active low.

1.1 List of Pin Functions

(1) System interface signals

Pin Name	I/O	Function
SysAD(63:0)	I/O	System address/data bus A 64-bit bus for communication between the processor and external agent. The lower 32 bits (SysAD(31:0)) are used in 32-bit bus mode.
SysADC(7:0)	I/O	System address/data check bus A bus for SysAD bus parity. Valid only during a data cycle. The lower 32 bits (SysADC(3:0)) are used in 32-bit bus mode.
SysCmd(8:0)	I/O	System command/data ID bus A 9-bit bus that transfers command and data identifiers between the processor and external agent
SysID(2:0)	I/O	System bus protocol ID These signals transfer request identifiers in the out-of-order return mode. The processor drives a valid identifier in synchronization with the activation of the ValidOut# signal. The external agent must drive valid identifiers in synchronization with the activation of the ValidIn# signal.
ValidIn#	Input	Valid In This signal indicates the external agent is driving a valid address or data onto the SysAD bus, a valid command or data identifier onto the SysCmd bus, or a valid request identifier onto the SysID bus in the out-of-order return mode.
ValidOut#	Output	Valid out This signal indicates the processor is driving a valid address or data onto the SysAD bus, a valid command or data identifier onto the SysCmd bus, or a valid request identifier onto the SysID bus in the out-of-order return mode.
RdRdy#	Input	Read ready This signal indicates the external agent is ready to accept a processor read request
WrRdy#	Input	Write ready This signal indicates the external agent is ready to accept a processor write request
ExtRqst#	Input	External request This signal indicates the external agent is requesting the right to use the system interface
Release#	Output	Releases interface This signal indicates the processor is releasing the system interface to external agent control
PReq#	Output	Processor request This signal indicates the processor has a request that is pending



(2) Initialization interface signals

(1/2)

Pin Name	I/O	Function
DivMode(2:0)		<p>Division mode</p> <p>These signals set the division ratio of PClock and SysClock as follows:</p> <p>111: 5.5                      110: 5                      101: 4.5                      100: 4                      011: 3.5                      010: 3                      001: 2.5                      000: 2</p> <p>Set the input levels of these signals before a power-on reset. Make sure that the levels of these signals do not change while the Vr5500 is operating.</p>
BigEndian	Input	<p>Endian mode</p> <p>This signal sets the byte ordering for addressing.</p> <p>1: Big endian                      0: Little endian</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p>
BusMode	Input	<p>Bus mode</p> <p>This signal sets the bus width of the system interface.</p> <p>1: 64 bits                      0: 32 bits</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p>
TIntSel	Input	<p>Interrupt source select</p> <p>This signal sets the interrupt source to be assigned to the IP7 bit of the Cause register.</p> <p>1: Timer interrupt                      0: Int5# input and external write request (SysAD5)</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p>
DisDValidO#	Input	<p>ValidOut# delay enable</p> <p>1: ValidOut# is active even while the address cycle is stalled                      0: ValidOut# is active during the address issuance cycle only</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p>
DWBTrans#	Input	<p>Doubleword block transfer enable (valid in 32-bit bus mode only)</p> <p>1: Disabled                      0: Enabled</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p>

**Remark** 1: High level, 0: Low level

(2/2)

Pin Name	I/O	Function
O3Return#	Input	<p>Out-of-Order Return mode</p> <p>This signal sets the protocol of the system interface.</p> <p>1: Normal mode 0: Out-of-order return mode</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p>
ColdReset#	Input	<p>Cold reset</p> <p>This signal completely initializes the internal status of the processor. Deassert it in synchronization with SysClock.</p>
Reset#	Input	<p>Reset</p> <p>This signal logically initializes the internal status of the processor. Deassert it in synchronization with SysClock.</p>
DrvCon	Input	<p>Drive control</p> <p>This signal sets the impedance of the external output driver.</p> <p>1: Low 0: Normal (recommended)</p> <p>Set the input level of this signal before a power-on reset. Make sure that the level of this signal does not change during VR5500 operation.</p> <p><b>Remark</b> Applies to revision 2.0 or later products. Fixed to 0 in revision 1.x products.</p>

**Remark** 1: High level, 0: Low level

The O3Return#, DWBTrans#, DisDValidO#, and BusMode signals are used for determining the protocol of the system interface. The protocol is selected as follows in accordance with the setting of these signals.

Protocol	O3Return#	DWBTrans#	DisDValidO#	BusMode
VR5000™ compatible	1	1	1	1
RM523x compatible	1	1	1	0
VR5432 native mode compatible	1	0	0	0
Out-of-order return mode	0	Arbitrary	Arbitrary	Arbitrary

**Remark** 1: High level, 0:Low level

RM523x is a product of PMC-Sierra, Inc.

**(3) Interrupt interface signals**

Pin Name	I/O	Function
Int(5:0)#	Input	<p>Interrupt</p> <p>These are general-purpose processor interrupt requests. The input states can be checked by the Cause register.</p> <p>Whether Int5# is acknowledged or not depends on the status of the TIntSel signal during reset.</p>
NMI#	Input	<p>Non-maskable interrupt</p> <p>This is the non-maskable interrupt request.</p>

**(4) Clock interface signals**

Pin Name	I/O	Function
SysClock	Input	System clock Clock input to the processor
V <sub>DD</sub> PA1 V <sub>DD</sub> PA2	–	V <sub>DD</sub> for PLL Power supply for the internal PLL
V <sub>SS</sub> PA1 V <sub>SS</sub> PA2	–	V <sub>SS</sub> for PLL Ground for the internal PLL

**(5) Power supply**

Pin Name	I/O	Function
V <sub>DD</sub>	–	Power supply pin for core
V <sub>DD</sub> IO	–	Power supply pin for I/O
V <sub>SS</sub>	–	Ground potential pin

**Caution** The V<sub>R5500</sub> uses two separate power supply pins. The power supply pins can be applied in any sequence. Power application to the pins must occur within 100ms of each other.

**(6) Test interface signals**

Pin Name	I/O	Function
NTrcData(3:0)	Output	Trace data Trace data output
NTrcEnd	Output	Trace end This signal indicates the end of a trace data packet.
NTrcClk	Output	Trace clock Clock for the test interface. The same clock as SysClock is output.
RMode#/ BKTGIO#	I/O	Reset mode/break trigger I/O When the JTRST# signal is active, this is a debug reset mode input signal . During normal operation this serves as a break or trigger I/O signal.
JTDI	Input	JTAG data input Serial data input for JTAG
JTDO	Output	JTAG data output Serial data output for JTAG. Output is performed in synchronization with the rise of JTCK.
JTMS	Input	JTAG mode select This signal selects the JTAG test mode.
JTCK	Input	JTAG clock input Serial clock input for JTAG. The maximum frequency is 33 MHz. There is no need for it to be synchronized with SysClock.
JTRST#	Input	JTAG reset input A signal for initializing the JTAG test module.

1.2 Recommended Connection of Unused Pins

(1) System interface pins

(a) 32-bit bus mode

The V<sub>R</sub>5500 allows selection of a SysAD bus width from 64 bits or 32 bits. When the 32-bit bus mode is selected, the V<sub>R</sub>5500 operates using only the required system interface pins. Therefore, set the unused pins as follows when operating the V<sub>R</sub>5500 in the 32-bit bus mode.

Pin Name	Recommended Connection of Unused Pins
SysAD(63:32)	Leave open
SysADC(7:4)	Leave open

(b) Normal mode

The V<sub>R</sub>5500 can process read/write transactions regardless of the order in which requests are issued in the out-of-order return mode. The SysID(2:0) signals are used to identify each request during this processing. Set these signals, which are not used in the normal mode, as follows.

Pin Name	Recommended Connection of Unused Pins
SysID(2:0)	Leave open

(c) Parity bus

The V<sub>R</sub>5500 allows selection of whether the data is protected using parity. When parity is used, the parity data is output from the processor or external agent to the SysADC bus.

However, whether the parity is used or not is selected by software, so unless the program is started, the V<sub>R</sub>5500 cannot determine the operation of the SysADC bus. Therefore, care must be taken to prevent the SysADC bus from being left open or in a high-impedance state.

Each pin of the SysADC bus should be connected to V<sub>DDIO</sub> via a high resistance value resistor when parity is not used.

**(2) Test interface pins**

The VR5500 can be used to perform testing and debugging via N-Wire and JTAG with the device mounted on the board. The test interface pins are used for connection with the external debug tool during this debugging. When this test interface is not going to be used and when it is in normal operation mode, set the test interface pins as follows.

Pin Name	Recommended Connection of Unused Pins
JTCK	Pull up
JTDI	Pull up
JTMS	Pull up
JTRST#	Pull up
JTDO	Leave open
NTrcClk	Leave open
NTrcData(3:0)	Leave open
NTrcEnd	Leave open
RMode#/BKTGIO#	Pull up

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>DDIO</sub>		-0.5 to +4.0	V
	V <sub>DD</sub>		-0.5 to +2.0	V
	V <sub>DDP</sub>		-0.5 to +2.0	V
Input voltage <sup>Note</sup>	V <sub>I</sub>		-0.5 to V <sub>DDIO</sub> + 0.3	V
		Pulse of less than 7 ns	-1.5 to V <sub>DDIO</sub> + 0.3	V
Operating case temperature	T <sub>c</sub>		-10 to +85	°C
Storage temperature	T <sub>stg</sub>		-40 to +125	°C

**Note** The upper limit of the input voltage (V<sub>ccIO</sub> + 0.3) is +4.0 V.

- Cautions**
1. Do not short-circuit two or more outputs at the same time.
  2. The maximum ratings shown in the table above indicate the point at which the product is on the verge of being physically damaged. Exceeding the maximum ratings even momentarily on any parameter may cause such damage. Therefore do not use the product under conditions which will violate these ratings.  
The specifications and conditions shown in the following DC Characteristics and AC Characteristics sections are the ranges within which the product can normally operate and the quality can be guaranteed.

Operating conditions

(1) 300 MHz product

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Supply voltage	V <sub>DDIO</sub>		2.375	2.625	V
			3.135	3.465	V
	V <sub>DD</sub>		1.425	1.575	V
	V <sub>DDP</sub>		1.425	1.575	V

**Caution** V<sub>DD</sub> can also be used with the voltage range of the 400 MHz product (1.6 to 1.7 V). Internal operation at 300 MHz is still guaranteed. The core block supply current in this case (MAX. 1.8 A) is the same value as the 400 MHz product.

(2) 400 MHz product

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Supply voltage	V <sub>DDIO</sub>		2.375	2.625	V
			3.135	3.465	V
	V <sub>DD</sub>		1.6	1.7	V
	V <sub>DDP</sub>		1.6	1.7	V

**Caution** V<sub>DD</sub> can also be used with the voltage range of the 300 MHz product (1.425 to 1.575 V). In this case, internal operation at 300 MHz is guaranteed only. The core block supply current in this case (MAX. 1.4 A) is the same value as the 300 MHz product.

**Supply Current**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Supply current of core block	I <sub>DD</sub>	300 MHz product, during normal operation, V <sub>DD</sub> = V <sub>DDP</sub> = 1.575 V		1.4	A
		400 MHz product, during normal operation, V <sub>DD</sub> = V <sub>DDP</sub> = 1.7 V		1.8	A
	I <sub>DD_sb</sub>	300 MHz product, in standby mode, V <sub>DD</sub> = V <sub>DDP</sub> = 1.575 V		0.35	A
		400 MHz product, in standby mode, V <sub>DD</sub> = V <sub>DDP</sub> = 1.7 V		0.45	A

**Remark** The supply current in the I/O block varies depending on the application used. It is normally 20% I<sub>DD</sub> or lower.

**DC Characteristics**

(1) When V<sub>DDIO</sub> = 2.5 V ±5%

(300 MHz product: T<sub>c</sub> = -10 to +85°C, V<sub>DDIO</sub> = 2.5 V ±5%, V<sub>DD</sub> = V<sub>DDP</sub> = 1.5 V ±5%)

(400 MHz product: T<sub>c</sub> = -10 to +85°C, V<sub>DDIO</sub> = 2.5 V ±5%, V<sub>DD</sub> = V<sub>DDP</sub> = 1.6 to 1.7 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V <sub>OH</sub>	V <sub>DDIO</sub> = MIN., I <sub>OH</sub> = 4 mA	0.8 × V <sub>DDIO</sub>		V
Output voltage, low	V <sub>OL</sub>	V <sub>DDIO</sub> = MIN., I <sub>OL</sub> = 4 mA		0.4	V
Input voltage, high <sup>Note 1</sup>	V <sub>IH</sub>		2.0	V <sub>DDIO</sub> + 0.3	V
Input voltage, low <sup>Note 1</sup>	V <sub>IL</sub>		-0.5	0.2 × V <sub>DDIO</sub>	V
		Pulse of less than 7 ns	-1.5	0.2 × V <sub>DDIO</sub>	V
Input voltage, high <sup>Note 2</sup>	V <sub>IHC</sub>		0.8 × V <sub>DDIO</sub>	V <sub>DDIO</sub> + 0.3	V
Input voltage, low <sup>Note 2</sup>	V <sub>ILC</sub>		-0.5	0.2 × V <sub>DDIO</sub>	V
		Pulse of less than 7 ns	-1.5	0.2 × V <sub>DDIO</sub>	V
Input current leakage, high	I <sub>LIH</sub>	V <sub>I</sub> = V <sub>DDIO</sub>		5.0	μA
Input current leakage, low	I <sub>LIL</sub>	V <sub>I</sub> = 0 V		-5.0	μA
Output current leakage, high	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DDIO</sub>		5.0	μA
Output current leakage, low	I <sub>LOL</sub>	V <sub>O</sub> = 0 V		-5.0	μA

- Notes**
1. Does not apply to the SysClock pin.
  2. Only applies to the SysClock pin.

(2) When  $V_{DDIO} = 3.3\text{ V} \pm 5\%$

(300 MHz product:  $T_c = -10$  to  $+85^\circ\text{C}$ ,  $V_{DDIO} = 3.3\text{ V} \pm 5\%$ ,  $V_{DD} = V_{DDP} = 1.5\text{ V} \pm 5\%$ )

(400 MHz product:  $T_c = -10$  to  $+85^\circ\text{C}$ ,  $V_{DDIO} = 3.3\text{ V} \pm 5\%$ ,  $V_{DD} = V_{DDP} = 1.6$  to  $1.7\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	$V_{OH}$	$V_{DDIO} = \text{MIN.}$ , $I_{OH} = 4\text{ mA}$	2.4		V
Output voltage, low	$V_{OL}$	$V_{DDIO} = \text{MIN.}$ , $I_{OL} = 4\text{ mA}$		0.4	V
Input voltage, high <sup>Note 1</sup>	$V_{IH}$		2.0	$V_{DDIO} + 0.3$	V
Input voltage, low <sup>Note 1</sup>	$V_{IL}$		-0.5	0.8	V
		Pulse of less than 7 ns	-1.5	0.8	V
Input voltage, high <sup>Note 2</sup>	$V_{IHC}$		$0.8 \times V_{DDIO}$	$V_{DDIO} + 0.3$	V
Input voltage, low <sup>Note 2</sup>	$V_{ILC}$		-0.5	$0.2 \times V_{DDIO}$	V
		Pulse of less than 7 ns	-1.5	$0.2 \times V_{DDIO}$	V
Input current leakage, high	$I_{LIH}$	$V_i = V_{DDIO}$		5.0	μA
Input current leakage, low	$I_{LIL}$	$V_i = 0\text{ V}$		-5.0	μA
Output current leakage, high	$I_{LOH}$	$V_o = V_{DDIO}$		5.0	μA
Output current leakage, low	$I_{LOL}$	$V_o = 0\text{ V}$		-5.0	μA

- Notes**
1. Does not apply to the SysClock pin.
  2. Only applies to the SysClock pin.



**Power-on Sequence**

The V<sub>R</sub>5500 uses two power supply pins. These power supply pins can be applied in any sequence. However, power may not be applied to one pin more than 100 ms before it is applied to the other.

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Power-on delay	t <sub>DF</sub>		0	100	ms

**Capacitance (T<sub>A</sub> = 25°C, V<sub>DDIO</sub> = V<sub>DD</sub> = V<sub>DDP</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	f <sub>c</sub> = 1 MHz		5.0	pF
Output capacitance	C <sub>OUT</sub>	Unmeasured pins returned to 0 V		7.0	pF

**AC Characteristics**

(300 MHz products: TC = -10 to +85, V<sub>DDIO</sub> = 2.5 V ±5%, 3.3 V ±5%, V<sub>DD</sub> = V<sub>DDP</sub> = 1.5 V ±5%)

(400 MHz product: TC = -10 to +85, V<sub>DDIO</sub> = 2.5 V ±5%, 3.3 V ±5%, V<sub>DD</sub> = V<sub>DDP</sub> = 1.6 to 1.7 V)

**Clock parameters (1/2)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
System clock high-level width	t <sub>CH</sub>		1.8		ns	
System clock low-level width	t <sub>CL</sub>		1.8		ns	
Pipeline clock frequency		300 MHz product	200	300	MHz	
		400 MHz product	200	400	MHz	
System clock frequency <sup>Note</sup>		300 MHz product	DivMode = 2:1	100	133	MHz
			DivMode = 2.5:1	80	120	MHz
			DivMode = 3:1	66.7	100	MHz
			DivMode = 3.5:1	57.2	85.7	MHz
			DivMode = 4:1	50	75	MHz
			DivMode = 4.5:1	44.5	66.6	MHz
			DivMode = 5:1	40	60	MHz
			DivMode = 5.5:1	36.4	54.5	MHz
		400 MHz product	DivMode = 2:1	100	133	MHz
			DivMode = 2.5:1	80	133	MHz
			DivMode = 3:1	66.7	133	MHz
			DivMode = 3.5:1	57.2	114	MHz
			DivMode = 4:1	50	100	MHz
			DivMode = 4.5:1	44.5	88.8	MHz
		DivMode = 5:1	40	80	MHz	
		DivMode = 5.5:1	36.4	72.7	MHz	

**Note** This is the frequency at which the operation of the internal PLL is guaranteed.

**Clock parameters (2/2)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
System clock cycle	tcp	300 MHz product	DivMode = 2:1	7.5	10	ns
			DivMode = 2.5:1	8.3	12.5	ns
			DivMode = 3:1	10	15	ns
			DivMode = 3.5:1	11.7	17.5	ns
			DivMode = 4:1	13.3	20	ns
			DivMode = 4.5:1	15	22.5	ns
			DivMode = 5:1	16.7	25	ns
			DivMode = 5.5:1	18.3	27.5	ns
		400 MHz product	DivMode = 2:1	7.5	10	ns
			DivMode = 2.5:1	7.5	12.5	ns
			DivMode = 3:1	7.5	15	ns
			DivMode = 3.5:1	8.8	17.5	ns
			DivMode = 4:1	10	20	ns
			DivMode = 4.5:1	11.3	22.5	ns
DivMode = 5:1	12.5	25	ns			
DivMode = 5.5:1	13.8	27.5	ns			
System clock jitter	tj			5	%	
System clock rise time	tcr			1.2	ns	
System clock fall time	tcf			1.2	ns	
JTAG clock frequency				33	MHz	

- Remarks**
1. The system clock jitter is a cycle-to-cycle jitter.
  2. The JTAG clock runs asynchronously to the system clock.

**System interface parameters**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data output hold time <sup>Note 1</sup>	tDM		1.0		ns
Data output delay time <sup>Note 1</sup>	tDO			5.0	ns
Data input setup time <sup>Note 2</sup>	tDS		1.5		ns
Data input hold time <sup>Note 2</sup>	tDH	300 MHz product	1.0		ns
		400 MHz product	0.5		ns

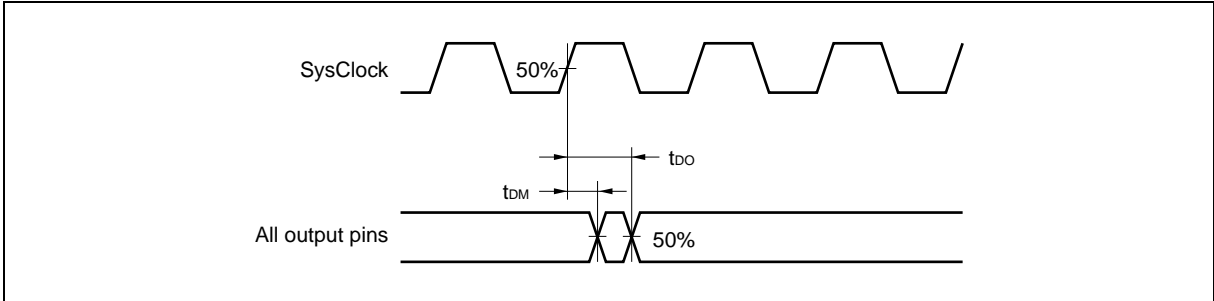
- Notes**
1. Applies to the Release#, ValidOut#, SysAD(63:0), SysADC(7:0), SysCmd(8:0), and SysID(2:0) pins.
  2. Applies to the ColdReset#, Reset#, Int(5:0), NMI#, ExtRqst#, RdRdy#, ValidIn#, SysAD(63:0), SysADC(7:0), SysCmd(8:0), and SysID(2:0) pins.

**Load coefficient**

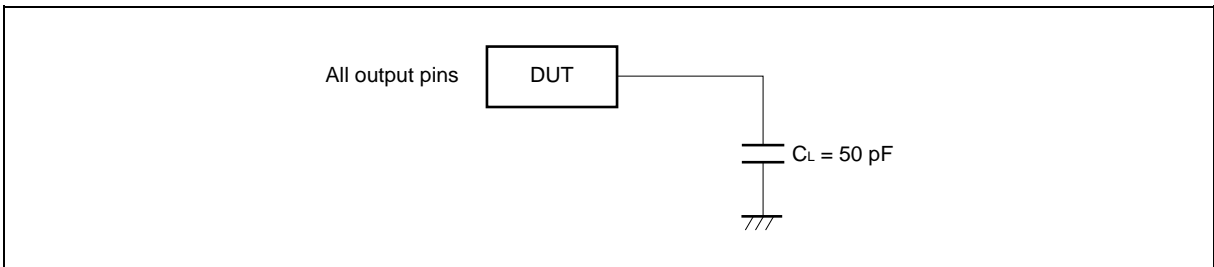
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Load coefficient	CLD			1.0	ns/25 pF

Measurement Conditions

Measurement points

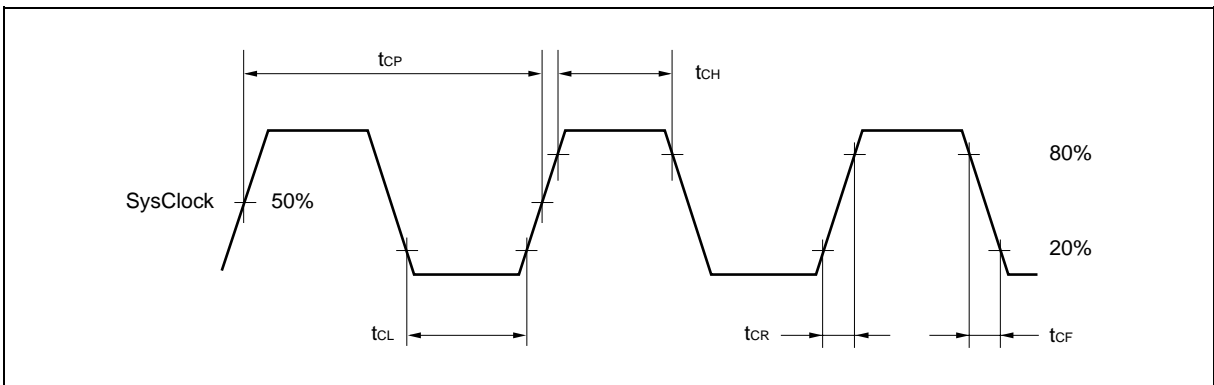


Load conditions

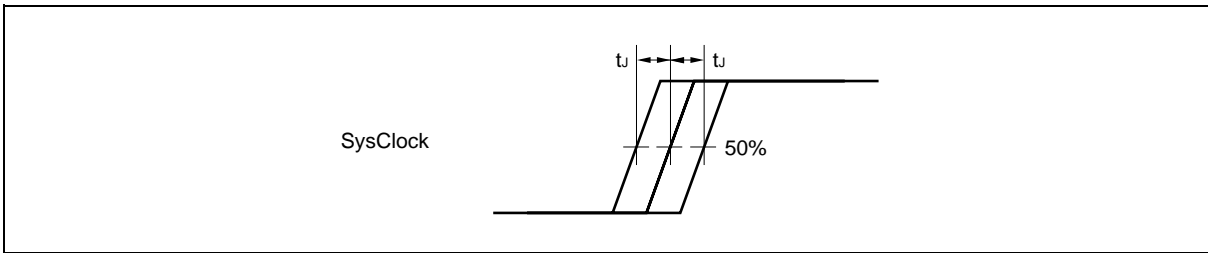


Timing Charts

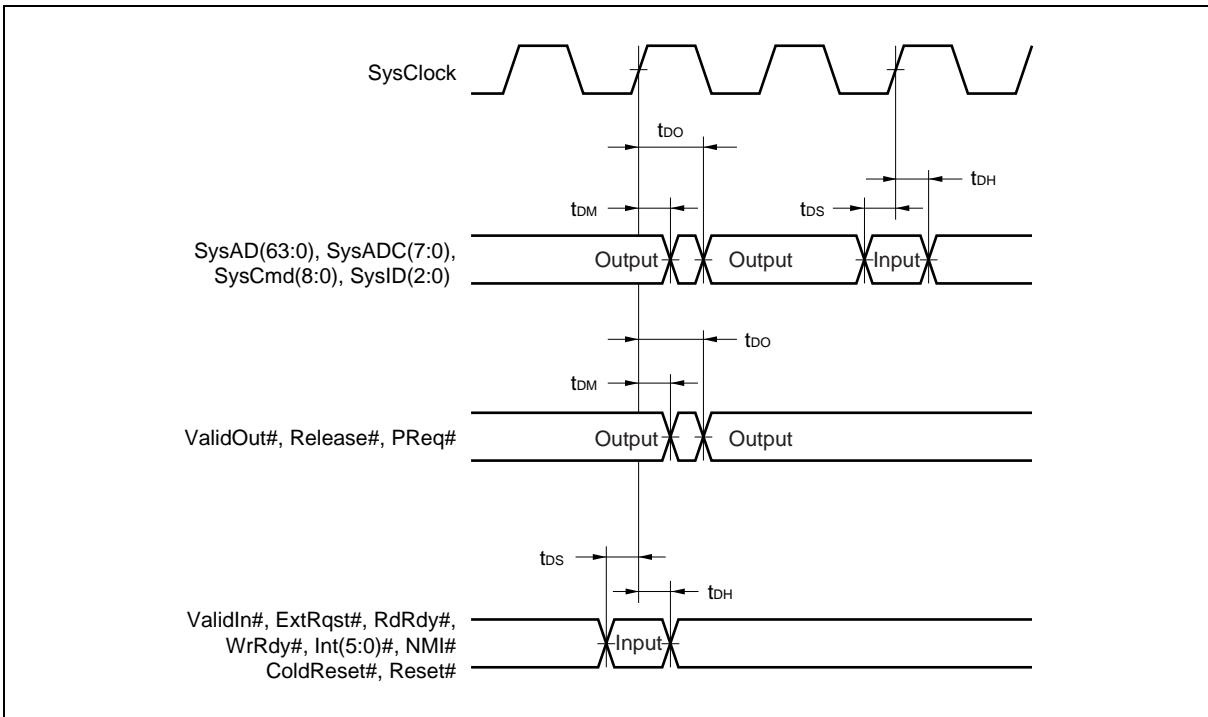
Clock timing



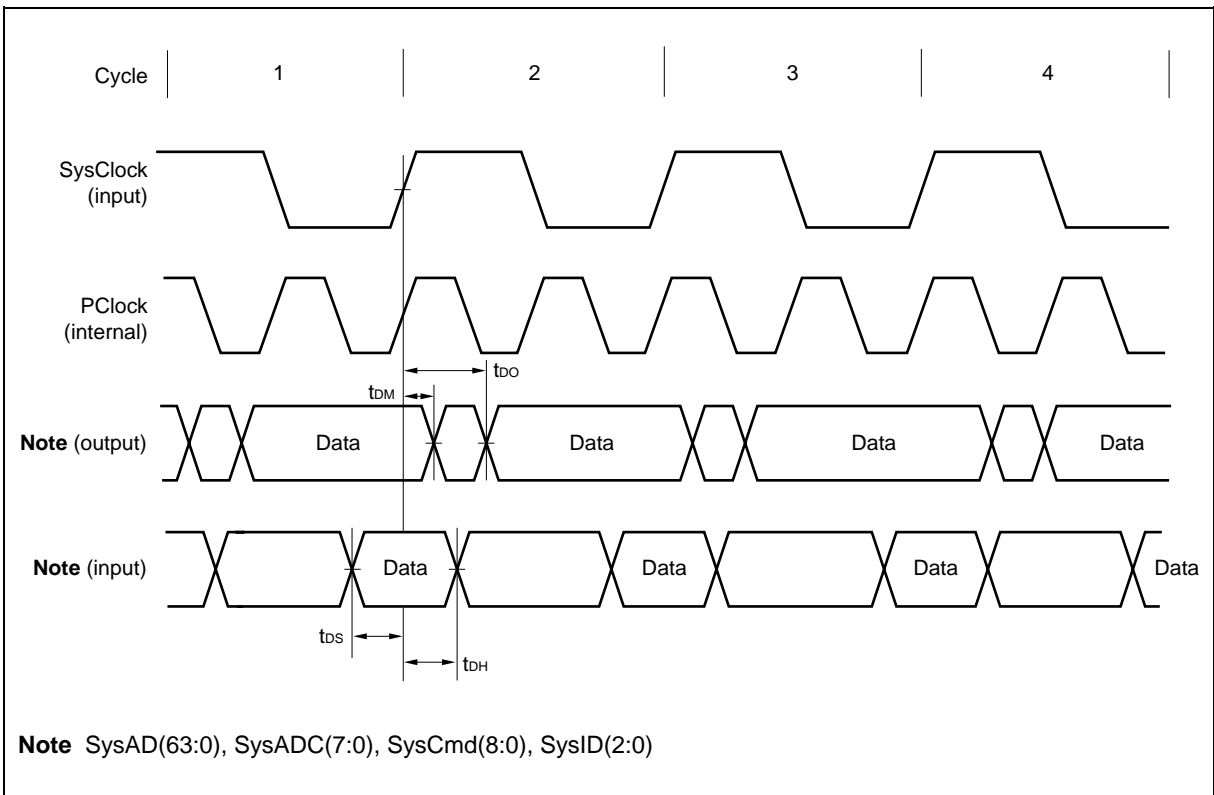
**Clock jitter**



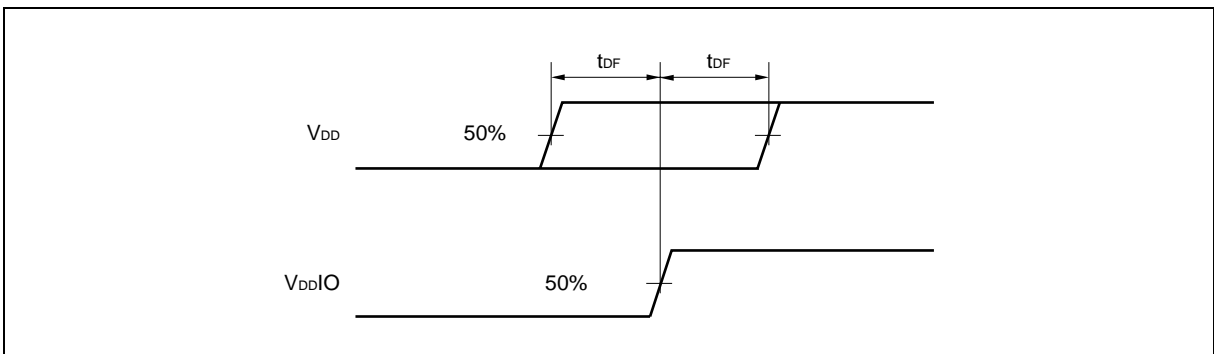
**System interface edge timing**



**Clock relationships (DivMode = 2:1)**

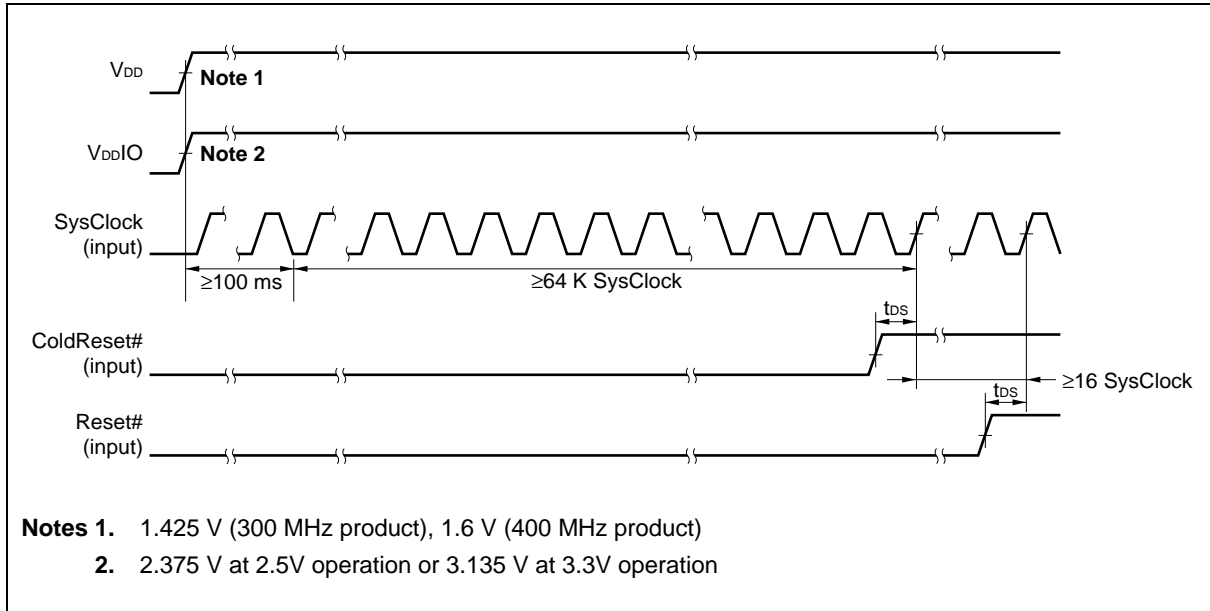


**Power-on sequence**

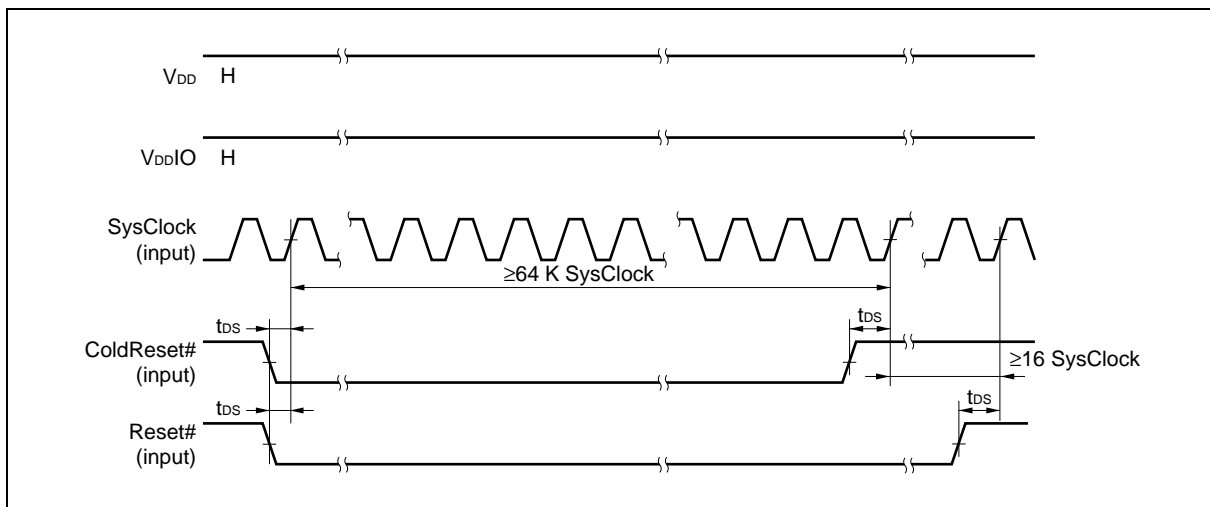


Reset Timing

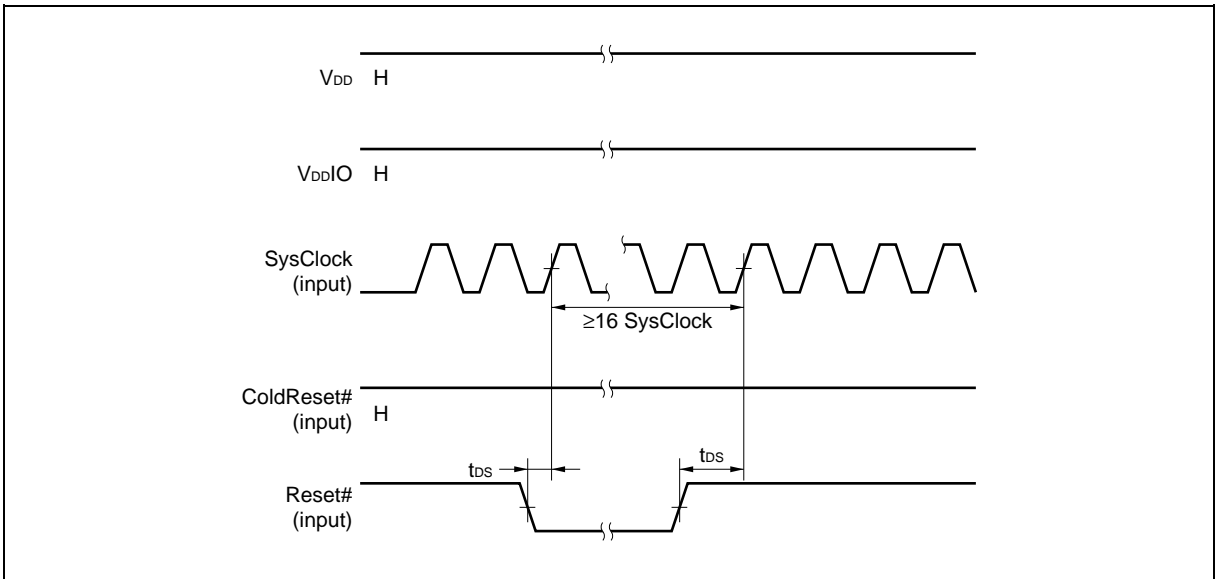
Power-on reset timing



Cold reset timing

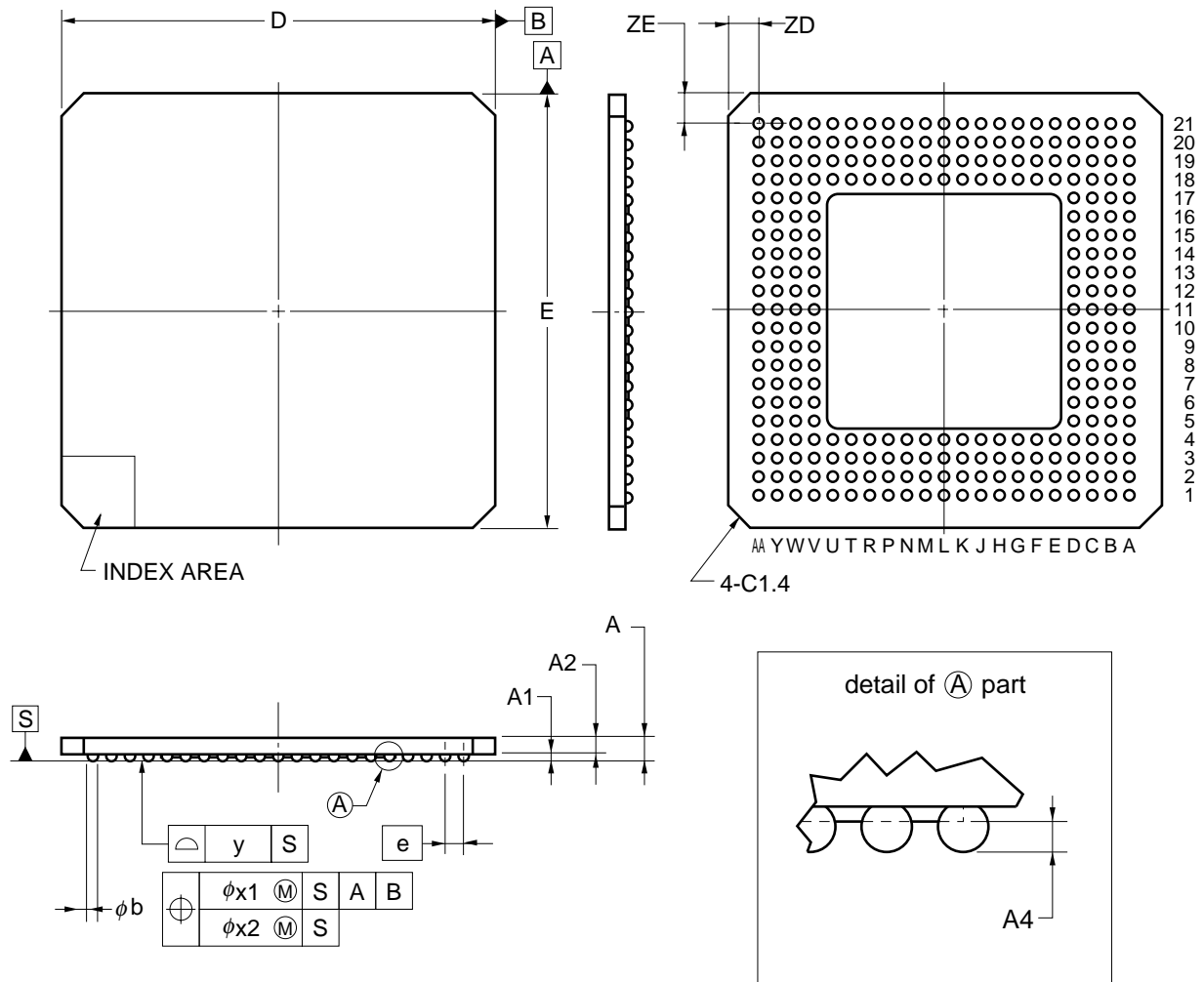


Warm reset timing



3. PACKAGE DRAWING

272-PIN PLASTIC BGA (CAVITY DOWN ADVANCED TYPE) (29x29)



ITEM	MILLIMETERS
D	29.00±0.20
E	29.00±0.20
e	1.27
A	1.75±0.30
A1	0.60±0.10
A2	1.15
A4	0.25MIN.
b	φ0.75±0.15
x1	0.30
x2	0.15
y	0.20
ZD	1.80
ZE	1.80

P272F2-127-BA1



**4. RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the following recommended conditions.

For details on the recommended soldering conditions, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 4-1. Surface mounting Type Soldering Conditions**

**μPD30550F2-300-NN1: 272-pin plastic BGA (C/D advanced type) (29 × 29)**

**μPD30550F2-400-NN1: 272-pin plastic BGA (C/D advanced type) (29 × 29)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	IR35-103-3

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

## NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference document** Electrical Characteristics for Microcomputer (U15170J)<sup>Note</sup>

**Note** This document number is that of Japanese version.

The related documents indicated in the publication may include preliminary versions. However, preliminary versions are not marked as such.

## Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

**NEC Electronics Inc. (U.S.)**

Santa Clara, California  
 Tel: 408-588-6000  
 800-366-9782  
 Fax: 408-588-6130  
 800-729-9288

**NEC do Brasil S.A.**

Electron Devices Division  
 Guarulhos-SP, Brasil  
 Tel: 11-6462-6810  
 Fax: 11-6462-6829

**NEC Electronics (Europe) GmbH**

Duesseldorf, Germany  
 Tel: 0211-65 03 01  
 Fax: 0211-65 03 327

• **Sucursal en España**

Madrid, Spain  
 Tel: 091-504 27 87  
 Fax: 091-504 28 60

• **Succursale Française**

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 Tel: 01-30-67 58 00  
 Fax: 01-30-67 58 99

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Milano, Italy  
 Tel: 02-66 75 41  
 Fax: 02-66 75 42 99

• **Branch The Netherlands**

Eindhoven, The Netherlands  
 Tel: 040-244 58 45  
 Fax: 040-244 45 80

• **Branch Sweden**

Taeby, Sweden  
 Tel: 08-63 80 820  
 Fax: 08-63 80 388

• **United Kingdom Branch**

Milton Keynes, UK  
 Tel: 01908-691-133  
 Fax: 01908-670-290

**NEC Electronics Hong Kong Ltd.**

Hong Kong  
 Tel: 2886-9318  
 Fax: 2886-9022/9044

**NEC Electronics Hong Kong Ltd.**

Seoul Branch  
 Seoul, Korea  
 Tel: 02-528-0303  
 Fax: 02-528-4411

**NEC Electronics Shanghai, Ltd.**

Shanghai, P.R. China  
 Tel: 021-6841-1138  
 Fax: 021-6841-1137

**NEC Electronics Taiwan Ltd.**

Taipei, Taiwan  
 Tel: 02-2719-2377  
 Fax: 02-2719-5951

**NEC Electronics Singapore Pte. Ltd.**

Novena Square, Singapore  
 Tel: 253-8311  
 Fax: 250-3583