HARRIS SEMICONDUCTOR

FRX130D, FRX130R, FRX130H

Radiation Hardened N-Channel Power MOSFETs

December 1997

Features

- 6A, 100V, $r_{DS(ON)} = 0.180\Omega$
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-RAD Specifications to 100K RAD (Si)
  - Defined End-Point Specs at 300K RAD (Si) and 1000K RAD (Si)
  - Performance Permits Limited Use to 3000K RAD (Si)
- Gamma Dot
  - Safe Operating Area Curve for Single Event Effects
  - SEE Immunity for LET of 36MeV/mg/cm^2 with V_{DS} up to 80% of Rated Breakdown and V_{GS} of 10V Off-Bias
- Dose Rate
  - Typically Survives 3E9 RAD (Si)/s at 80% BV_{DSS}
  - Typically Survives 2E12 if Current Limited to I_{DM}
- Photo Current
  - 1.50nA Per-RAD (Si)/s Typically
- Neutron
  - Maintain Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event
- Typically Survives 1E5 Ions/cm^2 Having an LET $\leq$ 35 MeV/mg/cm^2 and a Range 30μm at 80% BV_{DSS}

Ordering Information

PART NUMBER	PACKAGE	BRAND
FRX130D1	18 Ld CLCC	FRX130D1
FRX130D2	18 Ld CLCC	FRX130D2
FRX130D3	18 Ld CLCC	FRX130D3
FRX130D4	18 Ld CLCC	FRX130D4
FRX130R1	18 Ld CLCC	FRX130R1
FRX130R2	18 Ld CLCC	FRX130R2
FRX130R3	18 Ld CLCC	FRX130R3
FRX130R4	18 Ld CLCC	FRX130R4
FRX130H1	18 Ld CLCC	FRX130H1
FRX130H2	18 Ld CLCC	FRX130H2
FRX130H3	18 Ld CLCC	FRX130H3
FRX130H4	18 Ld CLCC	FRX130H4

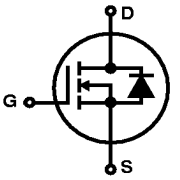
Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N-Channel and P-Channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD (Si) and 1000K RAD (Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^o) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

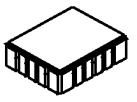
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Symbol



Package

18 LEAD CLCC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3144.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		FRX130D, R, H	UNITS
Drain to Source Voltage	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	100	V
Continuous Drain Current	I_D	6	A
$T_C = 100^oC$	I_D	4	A
Pulsed Drain Current	I_{DM}	18	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_T	11.4	W
$T_C = 100^oC$	P_T	4.5	W
Linear Derating Factor		0.09	$W/^oC$
Single Pulsed Avalanche Current, L = 100µH, (See Test Figure)	I_{AS}	18	A
Continuous Source Current (Body Diode)	I_S	6	A
Pulsed Source Current (Body Diode)	I_{SM}	18	A
Operating and Storage Temperature	T_{JC}, T_{STG}	-55 to 150	^oC
Lead Temperature (During Soldering) (Distance >0.063in (1.6mm) from Case, 10s Max)	T_L	300	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = 1mA, V_{DS} = V_{GS}	2.0		4.0	V
Gate-Body Leakage Forward	I_{GSSF}	V_{GS} = +20V	-		100	nA
Gate-Body Leakage Reverse	I_{GSSR}	V_{GS} = -20V	-		100	nA
Zero Gate Voltage Drain Current	I_{DSS1} I_{DSS2} I_{DSS3}	V_{DS} = 100V, V_{GS} = 0 V_{DS} = 80V, V_{GS} = 0 V_{DS} = 80V, V_{GS} = 0, $T_C = 125^oC$	- - -	-	1 0.025 0.25	µA
Rated Avalanche Current	I_{AR}	Time = 20µs	-	-	18	A
Drain to Source On-State Volts	$V_{DS(ON)}$	V_{GS} = 10V, I_D = 6A	-	-	1.130	V
Drain to Source On Resistance	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4A	-	-	0.180	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 6A	-	-	30	ns
Rise Time	t_r	Pulse Width = 3µs	-	-	100	
Turn-Off Delay Time	$t_{d(OFF)}$	Period = 300µs, Rg = 25Ω	-	-	200	
Fall Time	t_f	0 ≤ V_{GS} ≤ 10 (See Test Circuit)	-	-	100	
Gate-Charge Threshold	$Q_{g(TH)}$	V_{DD} = 50V, ID = 6A I_{GS1} = I_{GS2} 0 ≤ V_{GS} ≤ 20	1	-	4	nc
Gate-Charge On State	$Q_{g(ON)}$		17	-	70	
Gate-Charge Total	Q_{gM}		32	-	128	
Plateau Voltage	V_{GP}		3	-	12	V
Gate-Charge Source	Q_{gS}		3	-	14	nc
Gate-Charge Drain	Q_{gD}		8	-	32	
Diode Forward Voltage	V_{SD}	I_D = 6A, V_{GD} = 0	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	I = 6A; di/dt = 100A/µs	-	-	400	ns
Junction To Case	$R_{\theta JC}$		-	-	11	$^oC/W$
Junction To Ambient	$R_{\theta JA}$	Free Air Operation	-	-	250	

Typical Performance Curves Unless Otherwise Specified

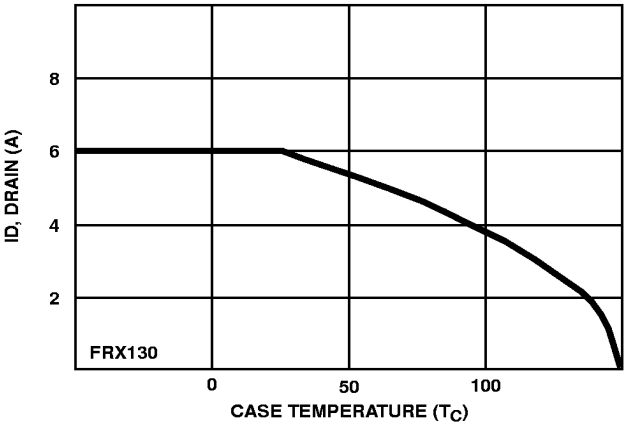


FIGURE 1. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

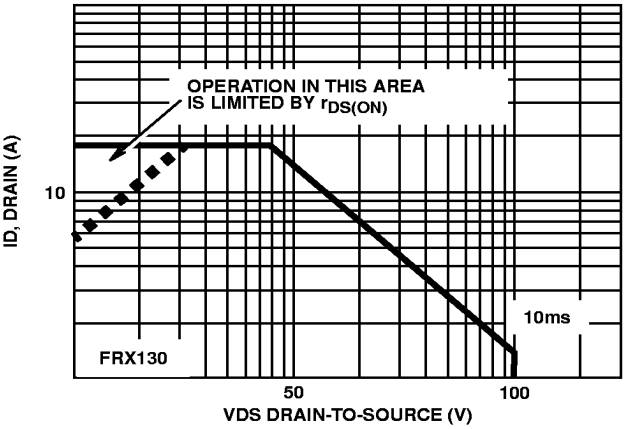


FIGURE 2. SAFE OPERATING AREA CURVE CASE TEMPERATURE = 25°C

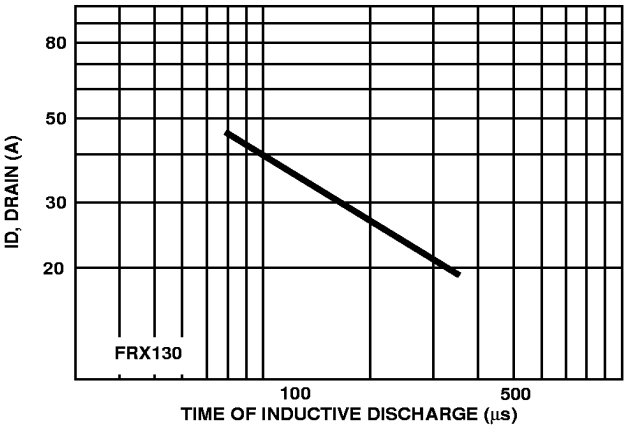


FIGURE 3. TYPICAL UNCLAMPED INDUCTIVE SWITCHING FAILURE ONSET AVALANCHE MODE

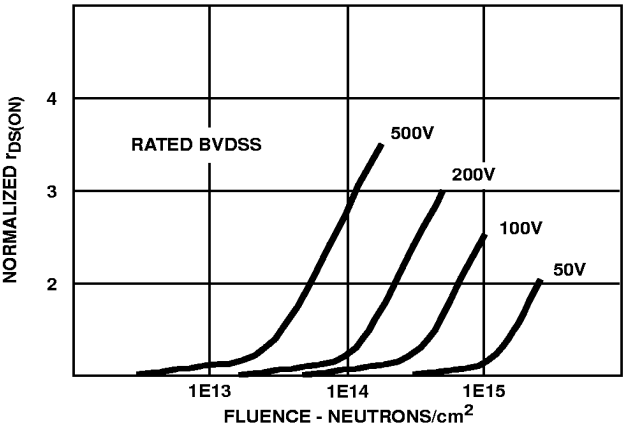


FIGURE 4. NORMALIZED ON-RESISTANCE vs NEUTRON FLUENCE N-CHANNEL

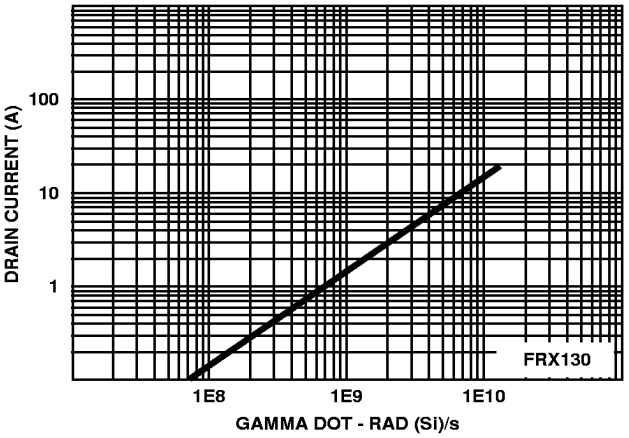


FIGURE 5. TYPICAL PHOTO CURRENT vs GAMMA RATE

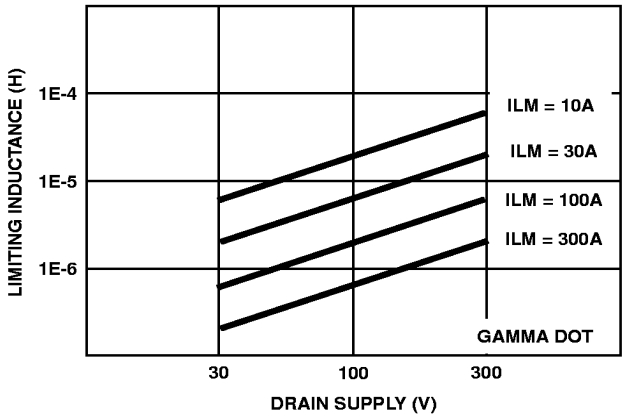


FIGURE 6. DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO I_{LM}

Test Circuits and Waveforms

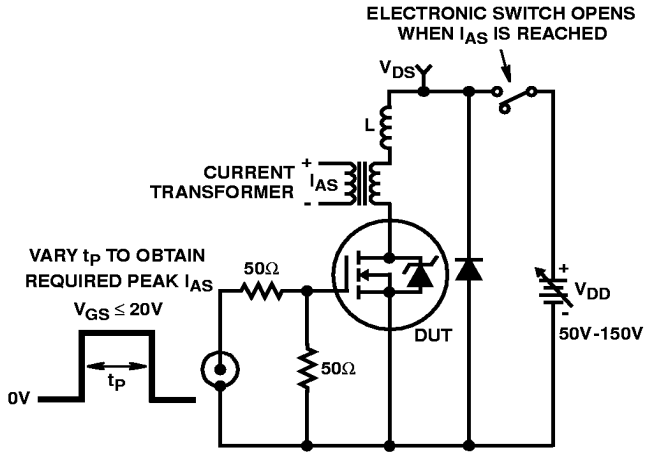


FIGURE 7. UNCLAMPED ENERGY TEST CIRCUIT

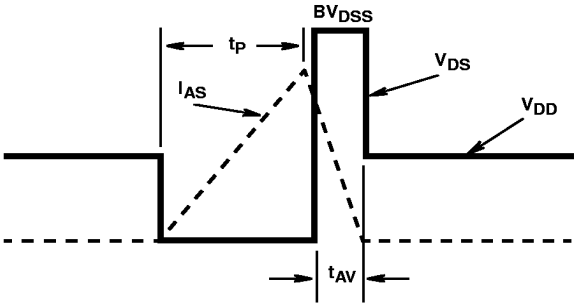


FIGURE 8. UNCLAMPED ENERGY WAVEFORMS

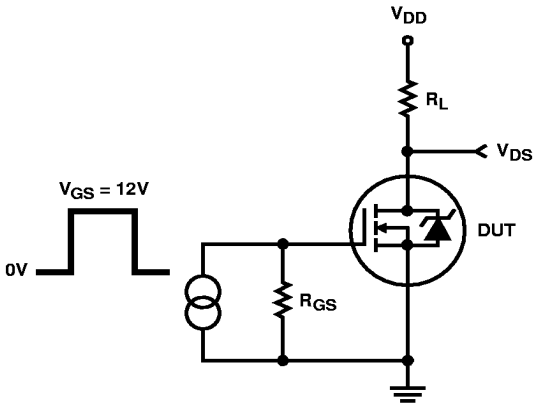


FIGURE 9. RESISTIVE SWITCHING TEST CIRCUIT

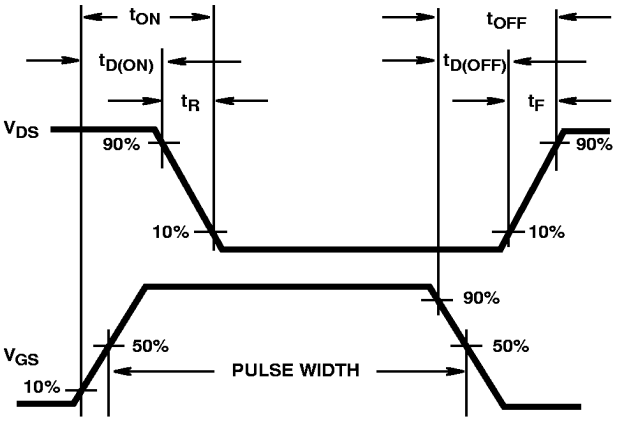
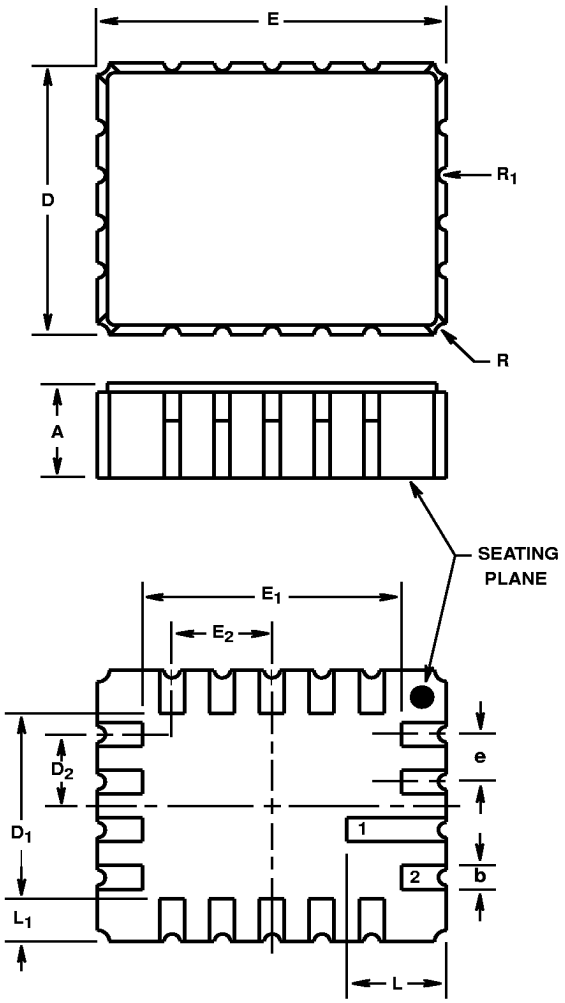


FIGURE 10. RESISTIVE SWITCHING WAVEFORMS

18 Pin CLCC

18 PIN CERAMIC LEADLESS CHIP CARRIER



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.112	2.34	2.84	-
b	0.020	0.030	0.51	0.76	-
D	0.275	0.295	6.99	7.49	-
D_1	0.175	0.215	4.45	5.46	-
D_2	0.070	0.080	1.78	2.03	-
E	0.340	0.360	8.64	9.14	-
E_1	0.240	0.280	6.10	7.11	-
E_2	0.095	0.105	2.42	2.66	-
e	0.050 BSC		1.27 BSC		-
L	0.085	0.115	2.16	2.92	-
L_1	0.035	0.055	0.89	1.39	-
R	0.007	0.017	0.18	0.43	4
R_1	0.003	0.013	0.08	0.33	4

NOTES:

1. No current JEDEC outline for this package.
2. All exposed metallized areas shall be plated with a minimum of 50 microinches of gold over nickel unless otherwise stated.
3. Metallized castellations shall be connected to the seating plane and extend upward toward top of package.
4. Corner shape (notch, radius, square, etc.) may vary at the manufacturer's option.
5. Unless otherwise specified, a minimum clearance of 0.010 inches (0.25mm) shall be maintained between all metallized areas.
6. Controlling dimension: Inch.
7. Revision 1 dated 6-93.

ELEMENT	PAD	PINS CONNECTED
GATE	A	5
DRAIN	B	1, 2, 3, 4, 16, 17, 18
SOURCE	C	6, 7, 8, 9, 10, 11, 12, 13, 14, 15