SONY

CXB1583Q

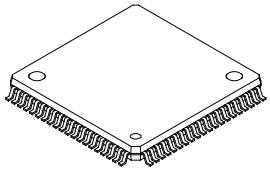
266Mbaud Fibre Channel Transceiver IC

Description

The CXB1583Q is a transceiver IC with the built-in PLLs into a single chip.

For receiver, the 265.625Mbaud serial data is received and it is output as a 10-bit parallel data; for transmitter, the 265.625Mbaud 10-bit parallel data is received and it is output as a serial data after conversion.

80 pin QFP (Plastic)



Features

- Transmitter/receiver into a single chip
- Conforms to ANSI X3T11 fibre channel standard
- PLL for a clock synthesizing and for clock recovery
- Single 3.3V power supply
- Low power consumption: 860mW (Typ.)
- 80-pin plastic package
- Comma signal detector
- Test pattern (±K28.5) generation circuit
- Loop-back circuit
- Supports data rage of 200Mbaud

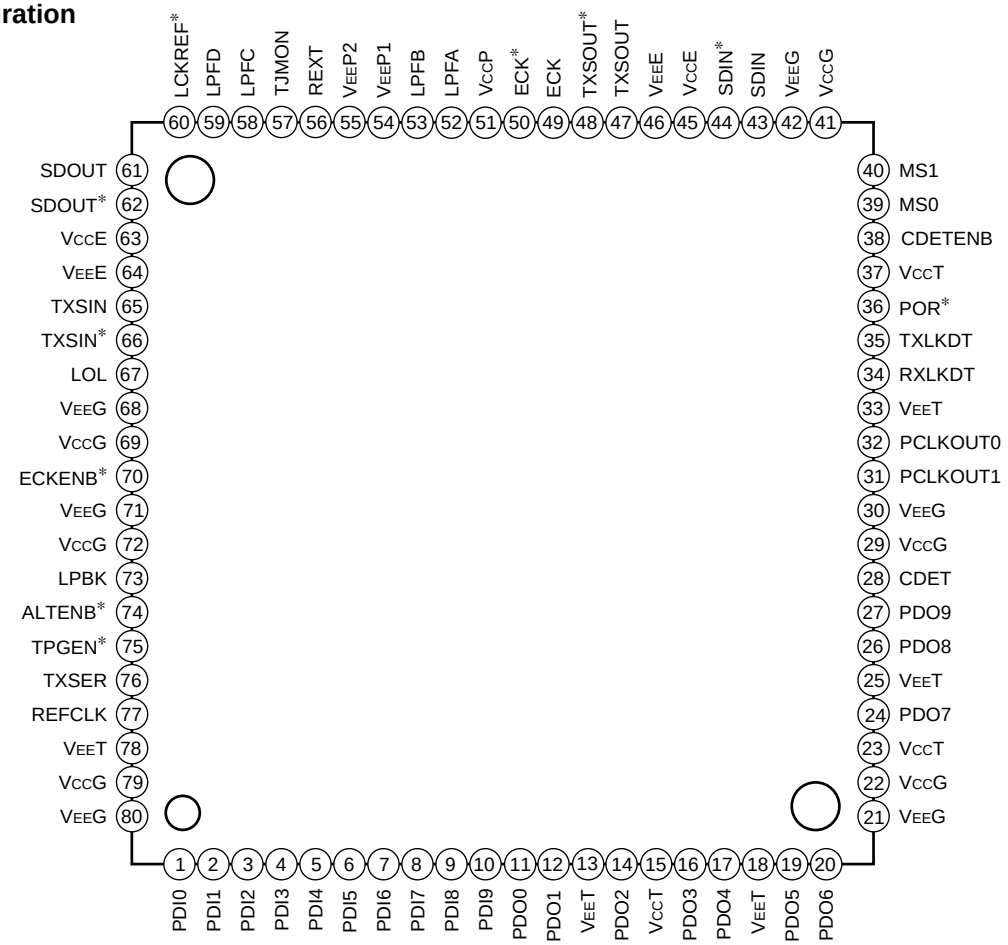
Applications

265.625Mbaud fibre channel

Structure

Bipolar silicon monolithic IC

Pin Configuration



E96501-ST

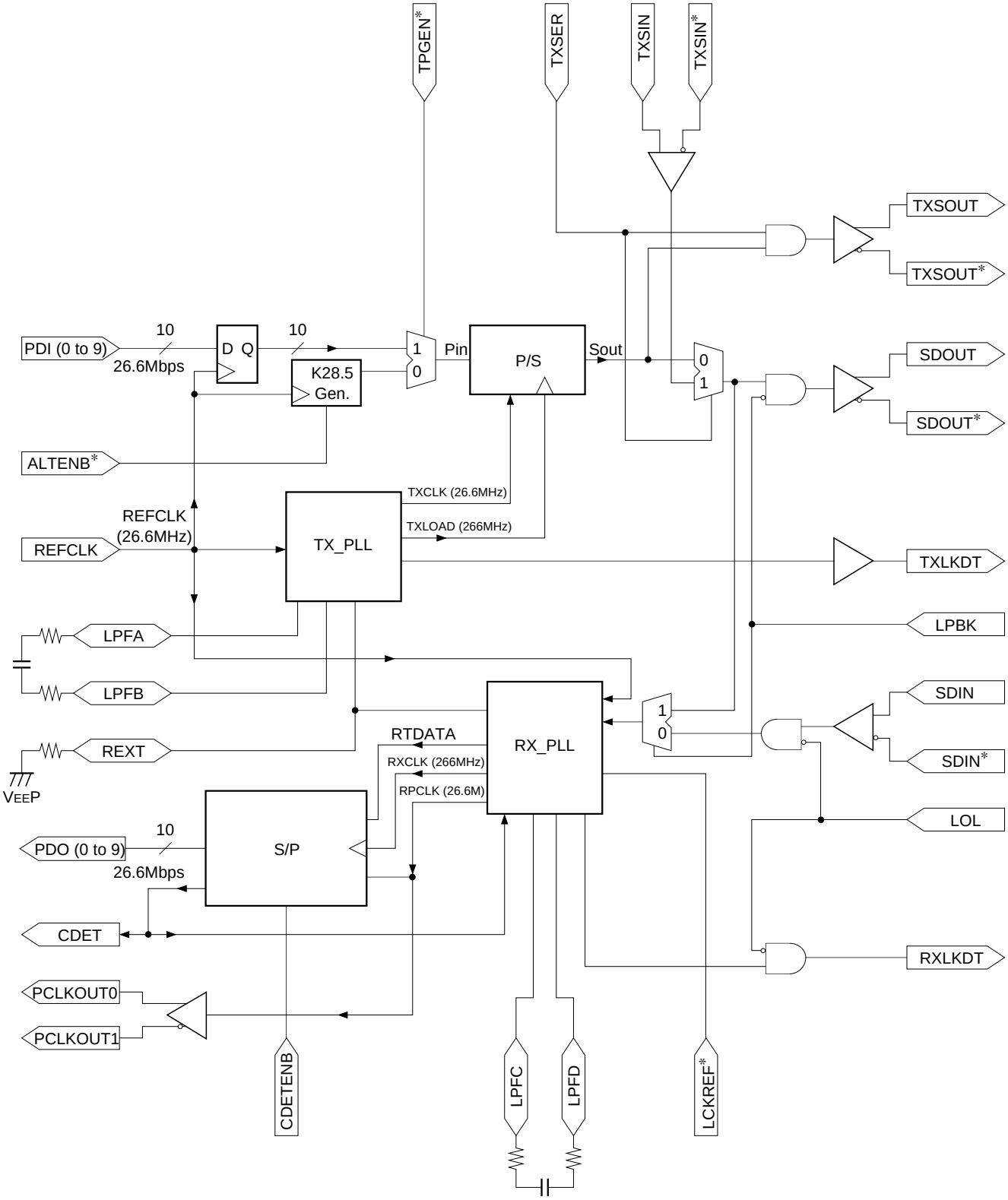
Absolute Maximum Ratings ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply	V_{CC}	–0.3		4	V
TTL DC input voltage	V_I_T	–0.5		5.5	V
ECL DC input voltage	V_I_E	V_{CC} – 2		V_{CC}	V
ECL differential input voltage	V_{IS}_E	–2		2	V
TTL output current (high level)	I_{OH}_T	–20		0	mA
TTL output current (low level)	I_{OL}_T	0		20	mA
ECL output current	I_O_E	–30		0	mA
Operating ambient temperature	Ta	–55		70	°C
Storage temperature	Tstg	–65		150	°C

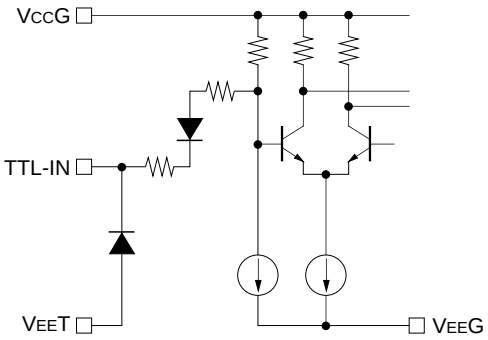
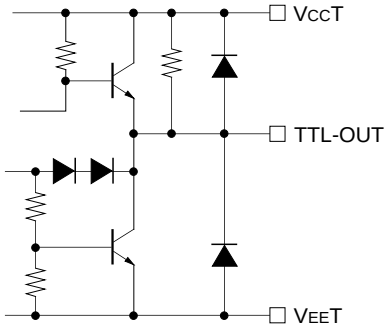
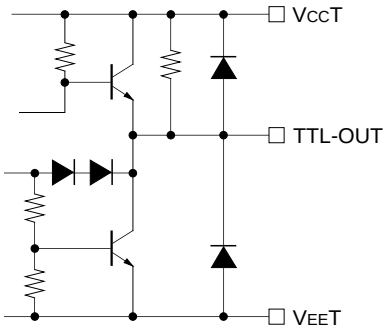
Recommended Operating Conditions ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = 0V)

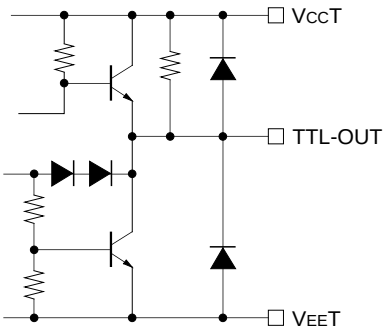
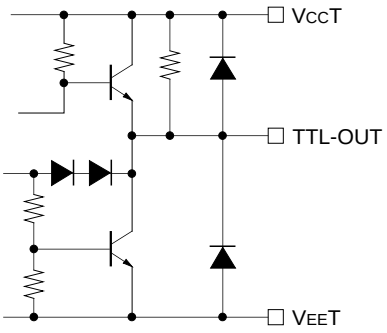
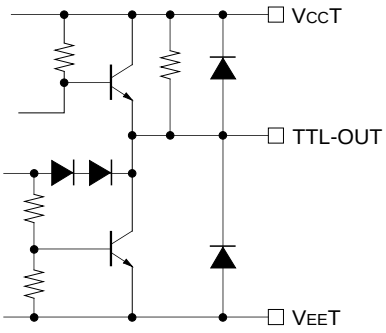
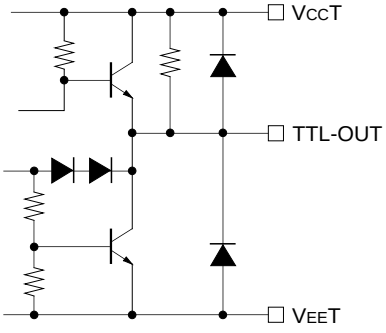
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3.135	3.3	3.465	V
Ambient temperature	Ta	0		70	°C

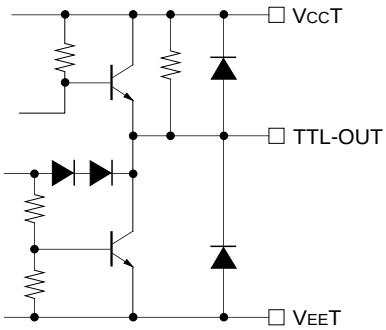
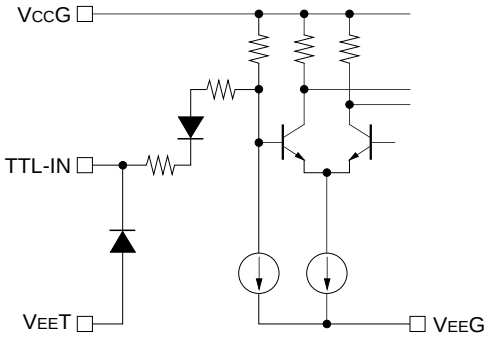
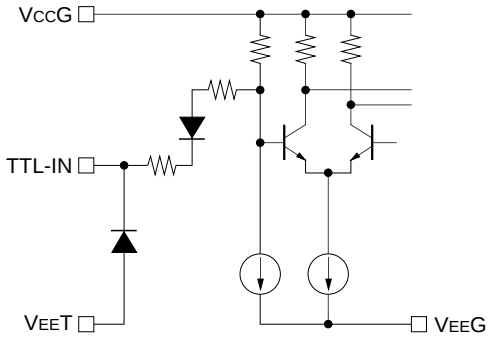
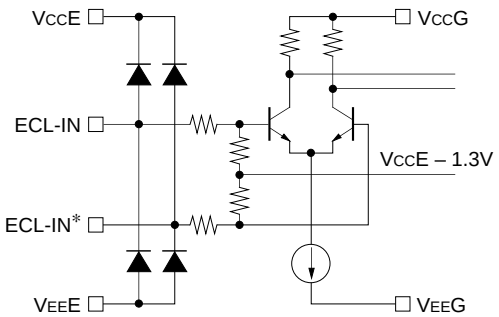
Block Diagram

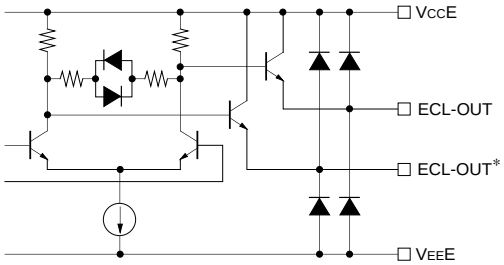
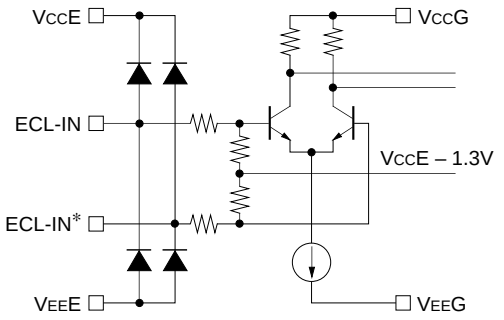
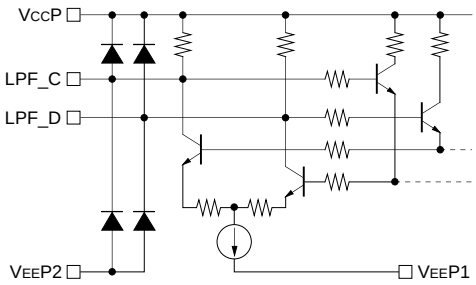
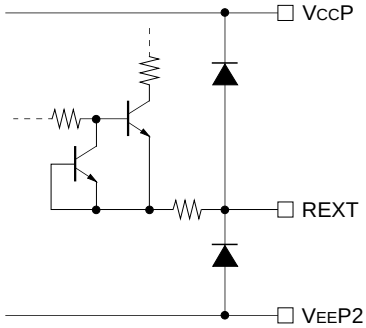


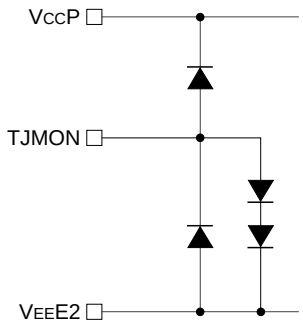
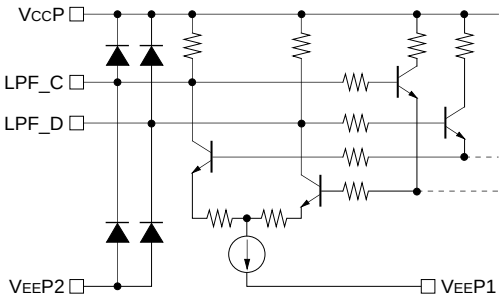
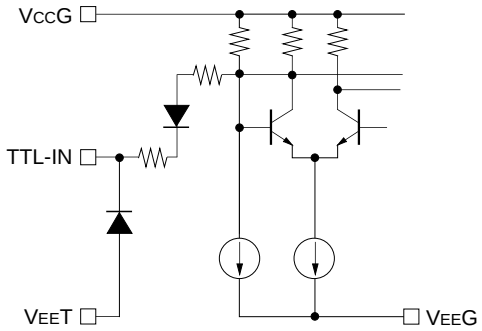
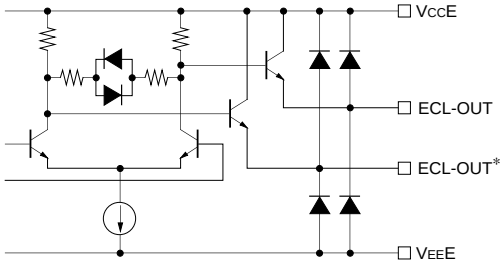
Pin Description

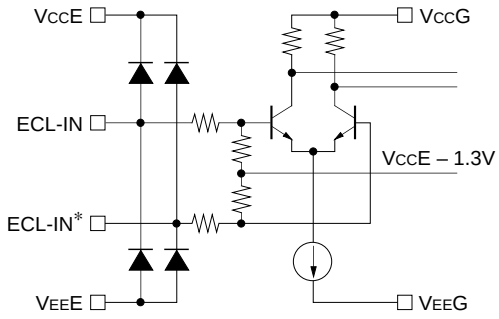
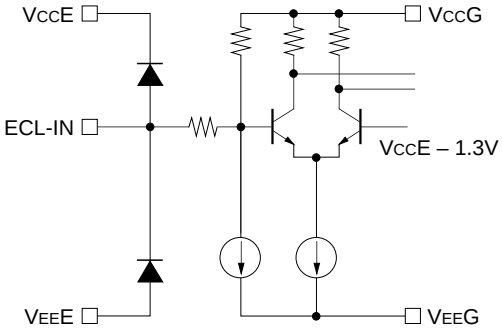
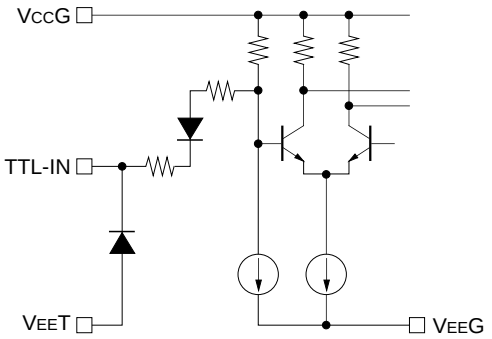
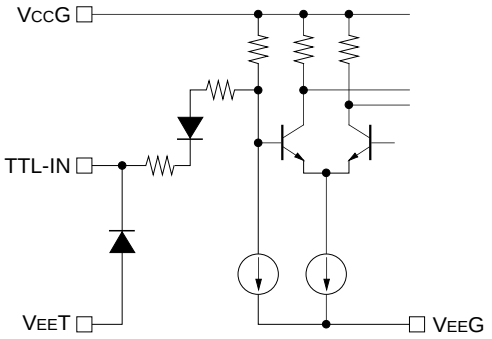
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
1 to 10	PDI0 to 9	TTL input	TTL level		Parallel data input.
11, 12, 14, 16, 17, 19, 20, 24, 26, 27	PDO0 to 9	TTL output	TTL level		Parallel data output.
13, 18, 25, 33, 78	VEET	Power supply	0V	—	Negative power supply for TTL input/output.
15, 23, 37	VCCT	Power supply	3.3V	—	Positive power supply for TTL output.
21, 30, 42, 68, 71, 80	VEEG	Power supply	0V	—	Negative power supply for internal logic gate.
22, 29, 41, 69, 72, 79	VCCG	Power supply	3.3V	—	Positive power supply for internal logic gate.
28	CDET	TTL output	TTL level		Byte synchronization output. Outputs high level when +Comma (0011111) or –Comma (1100000) is detected to the serial data.

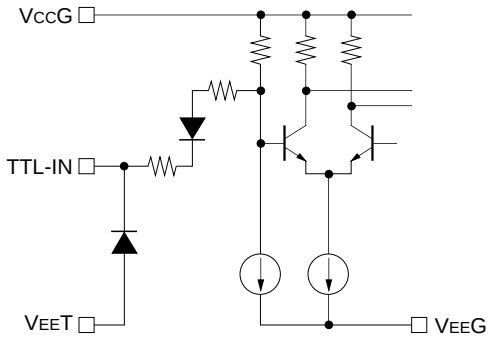
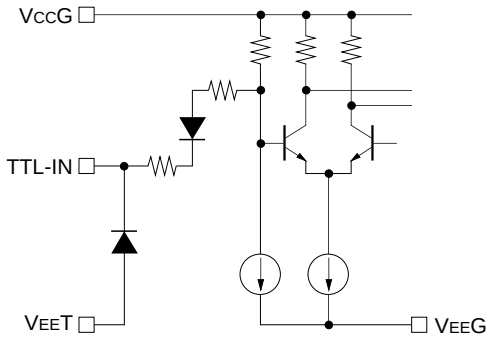
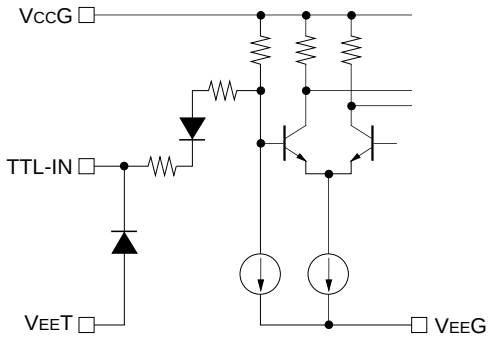
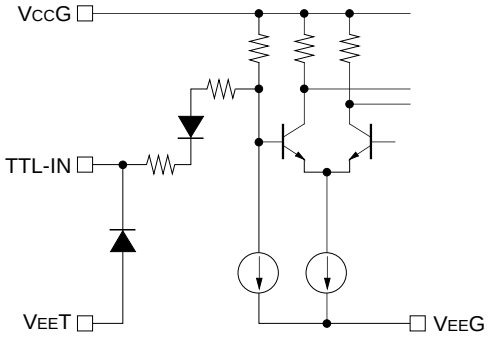
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
32	PCLKOUT0	TTL output	TTL level		Receive byte clock 0 output. This clock is used to take the parallel data (PDO0 to 9) at the next-stage system.
31	PCLKOUT1	TTL output	TTL level		Receive byte clock 1 output. PCLKOUT0 inverted clock.
34	RXLKDT	TTL output	TTL level		RX_PLL lock detection signal output. Outputs high level when the PLL is locked to the serial data or the serial data has no signal; Outputs low level when the PLL is not locked. RXLKDT output may sporadically go high when the PLL starts to lock to the serial data.
35	TXLKDT	TTL output	TTL level		TX_PLL lock detection signal output. Outputs high level when the PLL is locked to REFCLK and operating normally; Outputs low level when the PLL is not operating normally.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
36	POR*	TTL output	TTL level		Power-on reset signal output. Outputs high level after the power is turned on and low level is held for approximately 100ns.
38	CDETENB	TTL input	TTL level		Byte synchronization enable signal input. When high level is input, +Comma (0011111) or –Comma (1100000) is detected and the parallel data is synchronized with this byte. (See the Timing Chart.) When low level is input, byte synchronization is not performed.
39, 40	MS0, MS1	TTL input	3.3 V or TTL high level		Test pin. Connect to Vcc.
43, 44	SDIN SDIN*	ECL input (differ-ential)	ECL level		Serial data input.
45, 63	VCCE	Power supply	3.3V	—	Positive power supply for ECL input/output.
46, 64	VEEE	Power supply	0V	—	Negative power supply for ECL input/output.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
47, 48	TXSOUT TXSOUT*	ECL output (differential)	ECL level		Parallel/serial conversion output. This output is enabled when TXSER is high.
49, 50	ECK ECK*	ECL output (differential)	One is left open; another is connected to Vcc via 47kΩ.		Test pin. Connect either of these pins to Vcc via a 47kΩ resistor.
51	VCCP	Power supply	3.3V	—	Positive power supply for internal PLL.
52, 53	LPFA LPFB	External part connection	—		RX_PLL external loop filter connection. (See Fig. 1 of the Notes on Operation.)
54, 55	VEEP1 VEEP2	Power supply	0V	—	Negative power supply for internal PLL.
56	REXT	External part connection	—		Connects the resistor which determines the VCO center frequency. (See Fig. 1 of the Notes on Operation.)

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
57	TJMON	Test pin	0V		Junction temperature measurement.
58, 59	LPFC LPFD	External part connection	—		TX_PLL external loop filter connection. (See Fig. 1 of the Notes on Operation.)
60	LCKREF*	TTL input	TTL level		Lock-to-reference signal input. When this pin is set to low level, RX_PLL is forcibly locked to REFCLK.
61, 62	SDOUT SDOUT*	ECL output (differential)	ECL level		Serial data output for transmission. The serial data order is PDI0 → PDI9.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
65, 66	TXSIN TXSIN*	ECL input (differ-ential)	ECL level		Serial ECL data input. When TXSER is high, this input signal is output from SDOUT.
67	LOL	ECL input (single phase)	Open or ECL level		Lost-of-light signal input. Low level when this pin is left open.
70	ECKENB*	TTL input	3.3V or TTL high level		Test pin.
73	LPBK	TTL input	TTL level		Loop-back enable. If LPBK is set to high, the signal output from SDOUT when LPBK is low is transmitted to the RX input with the internal connection. In this time, SDOUT/ SDOUT* are fixed to low/high respectively and SDIN/SDIN* are both disabled.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
74	ALTENB*	TTL input	TTL level		Alternate disparity test pattern generation enable. When ALTENB* is set to low with TPGEN* low, K28.5 (+K28.5, –K28.5) is generated for the data stream output. When this pin is high, +K28.5 is generated.
75	TPGEN*	TTL input	TTL level		Test pattern generation enable. When this pin is low, +K28.5 (ALTENB*: high) or ±K28.5 (ALTENB*: low) is generated for the data stream output.
76	TXSER	TTL input	TTL level		Transmit serial data selector. When this pin is high, the serial data input from TXSIN is output from SDOUT and the serialized PDI0 to 9 signals are output from TXSOUT.
77	REFCLK	TTL input	TTL level		Transmit byte clock. This clock is used to take the PDI0 to 9 signals in the TXPLL. The RXPLL takes the frequency from REFCLK when LCKREF* is low. REFCLK is necessary after LCKREF* is set to high and the RXPLL is locked to the serial data.

CXB1583Q Functions

1. Data map to the 8b/10b alphabet notation

PDI0 is the start bit.

PDI, PDO	0	1	2	3	4	5	6	7	8	9
8b/10b alphabet notation	a	b	c	d	e	i	f	g	h	j

2. COMMA DETECT

When CDETENB is high and the SDIN input data row includes K28.5, PDO0 to 9 are synchronized with K28.5 and output. Byte synchronization is also performed to ±Comma.

Serial Data	PDO0 a	b	c	d	e	i	f	g	h	PDO9 j
+K28.5	0	0	1	1	1	1	1	0	1	0
Comma (positive)	0	0	1	1	1	1	1	X	X	X
Comma (negative)	1	1	0	0	0	0	0	X	X	X
–K28.5	1	1	0	0	0	0	0	1	0	1

3. TXSER, LPBK operation modes

Input		Output		
TXSER	LPBK	TXSOUT	SDOUT	PDO0 to 9
Low	Low	Disabled/Static	Serialized PDI	SDIN
Low	High	Disabled/Static	Disabled/Static	PDI
High	Low	Serialized PDI	TXSIN	SDIN
High	High	Serialized PDI	Disabled/Static	TXSIN

4. LCKREF* operation modes

LCKREF input level	RXPLL comparison signal
High	SDIN, SDIN*
Low	REFCLK

5. CDETENB

CDETENB input level	Operation
High	Byte synchronization with the Comma signal
Low	Byte synchronization function stop

Electrical Characteristics

DC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL high level input voltage	V_{IH}_T	2		5.5	V	
TTL low level input voltage	V_{IL}_T	0		0.8	V	
TTL high level input current	I_{IH}_T			20	µA	$V_{IH} = V_{CC}$
TTL low level input current	I_{IL}_T	–400			µA	$V_{IL} = 0$
TTL high level output voltage	V_{OH}_T	2.2			V	I_{OH} = –0.4mA
TTL low level output voltage	V_{OL}_T			0.5	V	I_{OL} = 2mA
ECL high level input voltage	V_{IH}_E	V_{CC} – 1.17		V_{CC} – 0.88	V	
ECL low level input voltage	V_{IL}_E	V_{CC} – 1.81		V_{CC} – 1.48	V	
ECL differential input voltage	V_{IS}_E	200		1000	mV	AC coupling input
ECL high level output voltage	V_{OH}_E	V_{CC} – 1.05		V_{CC} – 0.81	V	50Ω terminated to Vcc – 2 V
ECL low level output voltage	V_{OL}_E	V_{CC} – 1.81		V_{CC} – 1.55	V	50Ω terminated to Vcc – 2 V
ECL output amplitude	V_{OS}_E	650			mV	50Ω terminated to Vcc – 2 V
Current consumption	I_{CC}		260	341	mA	Output pins open
Power consumption	P_D		0.86	1.18	W	Output pins open

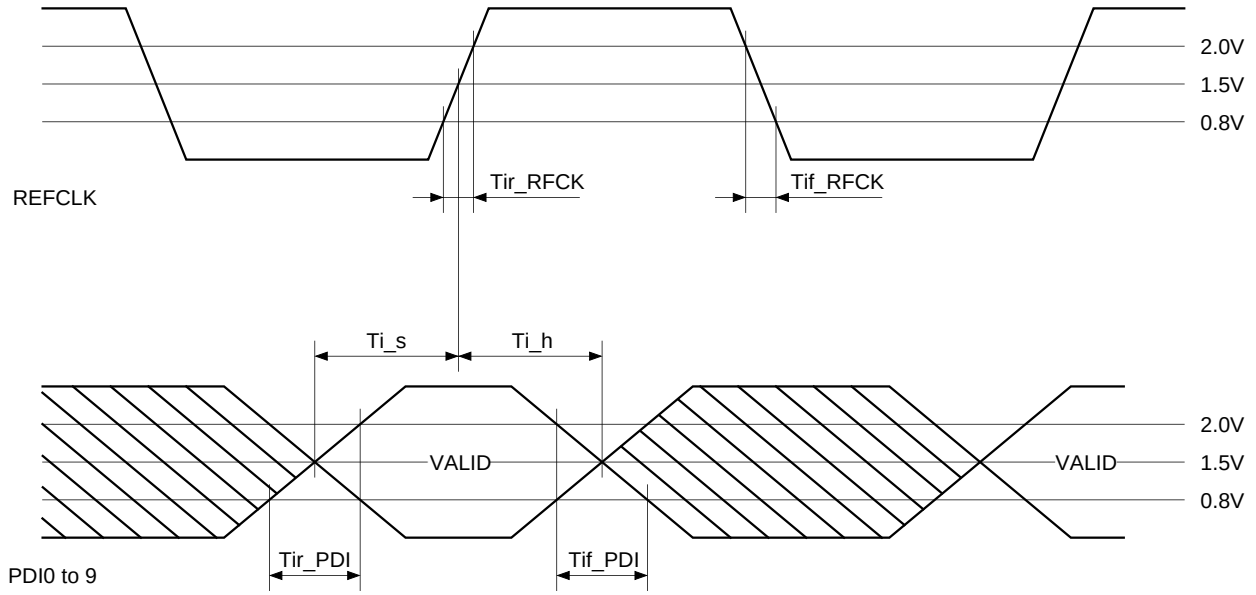
AC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
PDI rise time	Tir_PDI			10	ns	0.8 to 2.0V
PDI fall time	Tif_PDI			10	ns	2.0 to 0.8V
REFCLK rise time	Tir_RFCK	0.375		5	ns	0.8 to 2.0V
REFCLK fall time	Tif_RFCK	0.375		5	ns	2.0 to 0.8V
TTL output rise time	Tor_T			5	ns	0.8 to 2.0V, CL = 10pF
TTL output fall time	Tof_T			5	ns	2.0 to 0.8V, CL = 10pF
ECL output rise time	Tor_E			500	ps	20 to 80%, CL = 2pF
ECL output fall time	Tof_E			500	ps	20 to 80%, CL = 2pF
SDIN data rate	R_SDIN	190		280	Mbaud	
REFCLK cycle tolerance	Ttol_RFCK	–200	0	200	ppm	SDIN cycle reference
REFCLK duty cycle	DC_RFCK	40		60	%	
PCLKOUT0 and 1 skew	Tskew	–3		3	ns	
PDI setup time	Ti_s	4			ns	REFCLK reference
PDI hold time	Ti_h	3			ns	REFCLK reference
PDO setup time	To_s	10			ns	PCLKOUT0 reference
PDO hold time	To_h	12			ns	PCLKOUT0 reference
TX deterministic jitter (p-p)	DJ			0.08	UI	Serial data output
TX random jitter (p-p)	RJ			0.15	UI	Serial data output
RX jitter tolerance	JT			0.7	UI	Serial data input

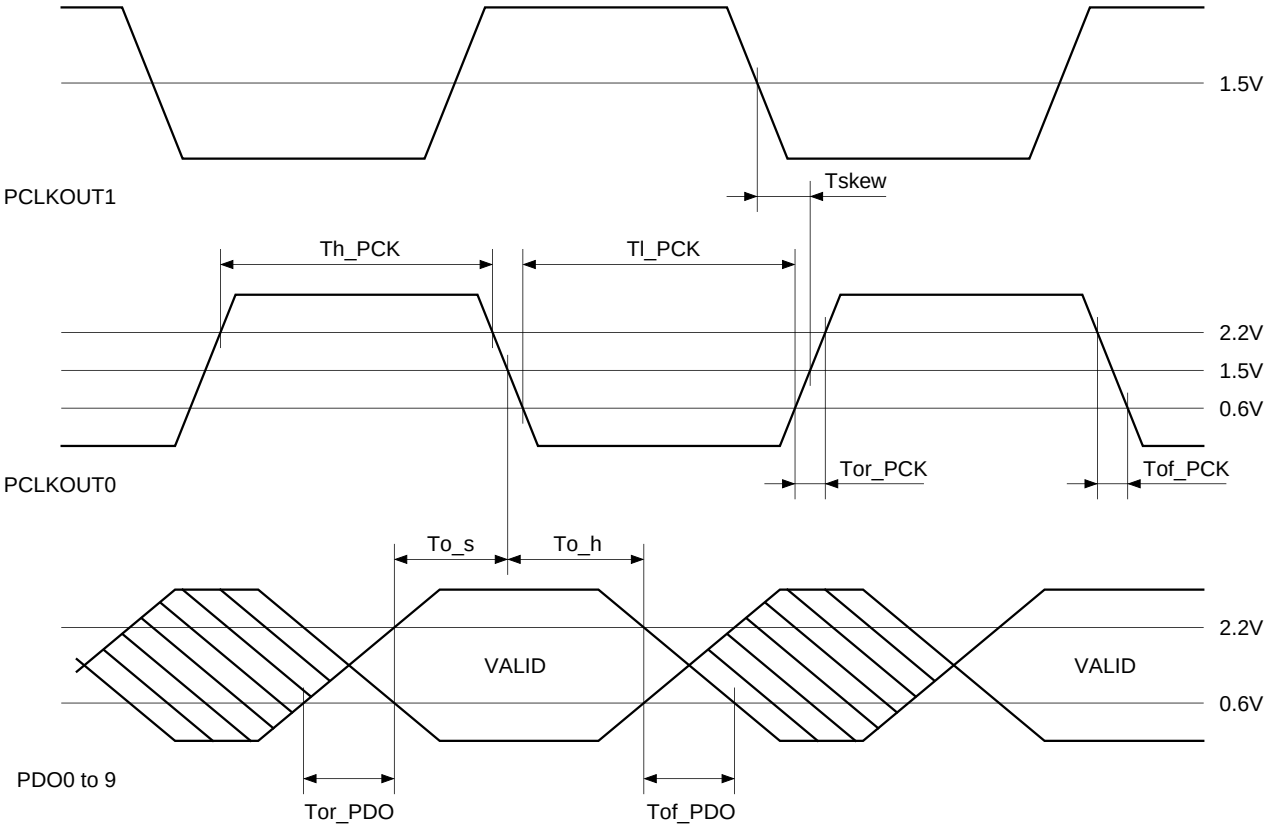
PLL AC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TX/PX PLL frequency acquisition time	Tfa			500	µs	Loop damping capacitance = 0.01µF
RX PLL bit synchronization time	Tbs			2500	bit	

Timing Chart for TX

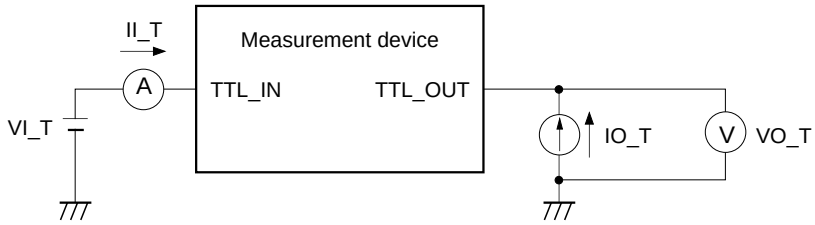


Timing Chart for RX

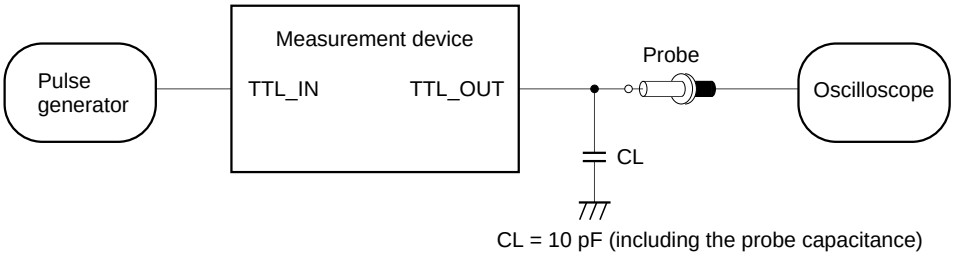


Electrical Characteristics Measurement Circuit

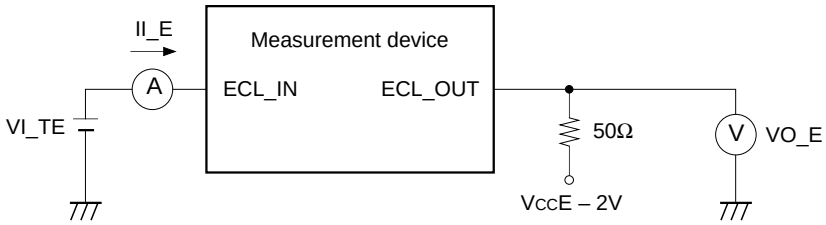
(See “Fig. 3 Power Supply Circuit” regarding the power supply.)



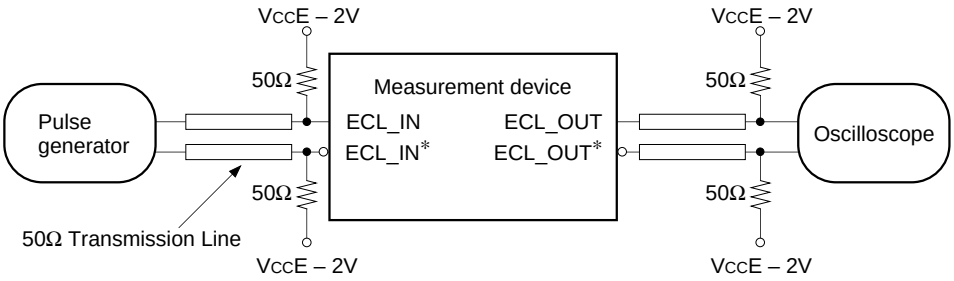
(a) TTL I/O DC characteristics measurement circuit



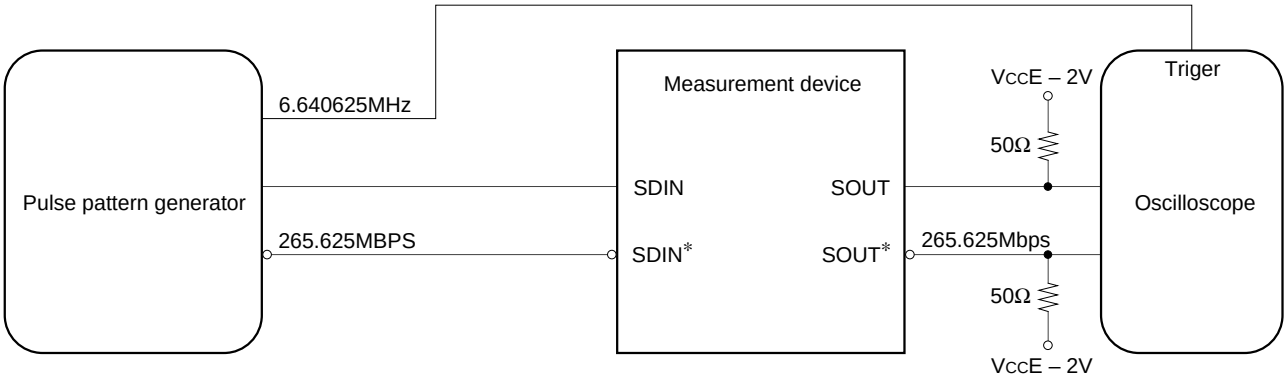
(b) TTL I/O AC characteristics measurement circuit



(c) ECL I/O DC characteristics measurement circuit



(d) ECL I/O AC characteristics measurement circuit

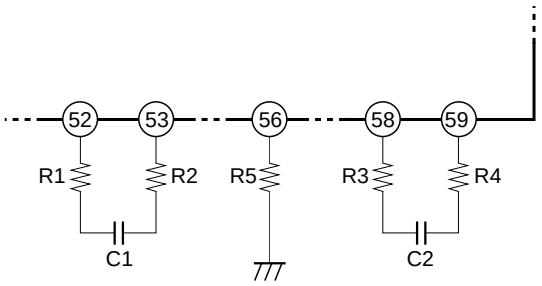


(e) Jitter characteristics measurement circuit

Notes on Operation

1. Clock synthesizer (PLL)

The CXB1583Q has a PLL-based clock synthesizer for generating the serial data transfer frequency (transmission bit clock) and clock recovery circuit for recovering the clock from the reception serial data. These circuits require the external loop filters and external resistors which determine the VCO center frequency. The external part circuit and recommended constant values are shown in the figure below. The parasitic capacitance attached to the pins which are used to connect external parts should be kept as small as possible in order to obtain the good PLL characteristics.

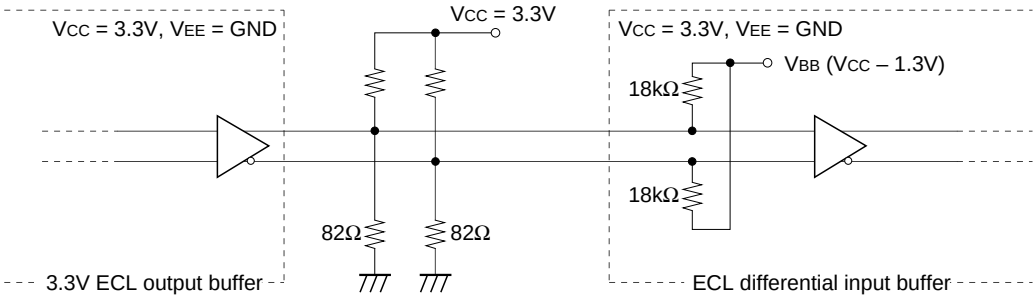


C1 : 0.01µF
C2 : 0.01µF
R1 : 1.8kΩ
R2 : 1.8kΩ
R3 : 2.0kΩ
R4 : 2.0kΩ
R5 : 2.2kΩ

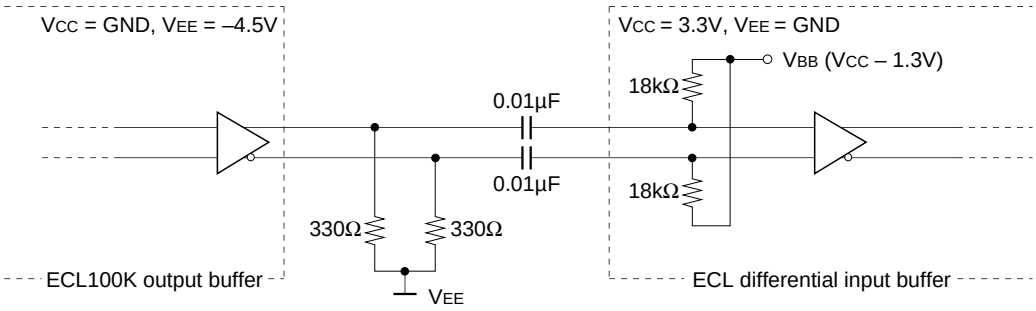
Fig. 1. External Part Circuit and Recommended Constants

2. ECL input circuit

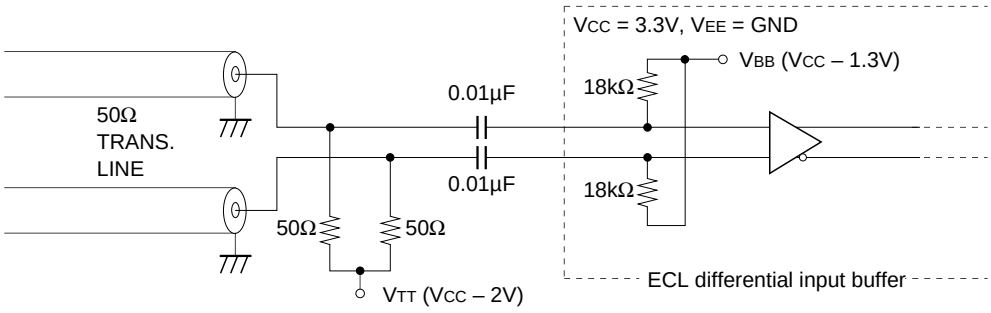
The ECL differential input pins are biased to V_{BB} (V_{CC} – 1.3 V) via an 18kΩ resistor in the IC. See the figures below for ECL differential input methods.



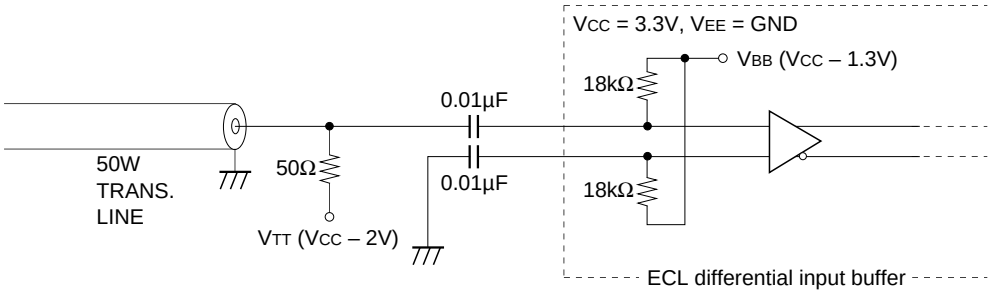
(a) ECL differrential signal from 3.3V ECL output buffer



(b) ECL differrential signal from ECL 100K output buffer



(c) ECL differrential signal from 50Ω transmission line



(d) ECL single signal from 50Ω transmission line

Fig. 2. ECL Input Circuits

3. Example of power supply circuit

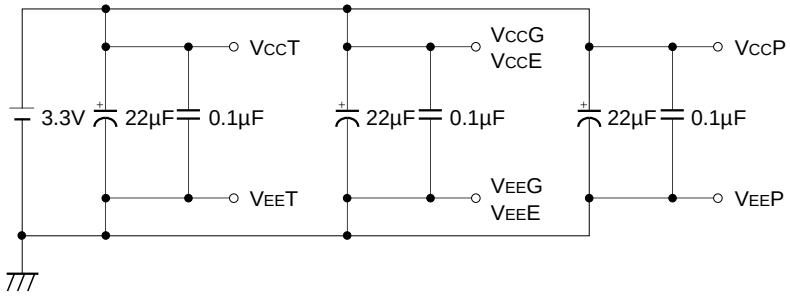


Fig. 3. Example of power supply circuit

4. Power-on reset signal (POR*)

The CXB1583Q has the power-on reset signal (POR*). This signal functions as a system reset signal when the power is turned on, the low level of signal is output for approximately 100ns and then the high level results.

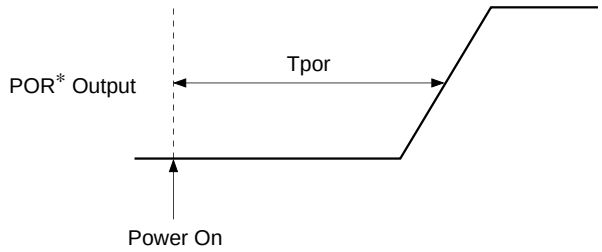
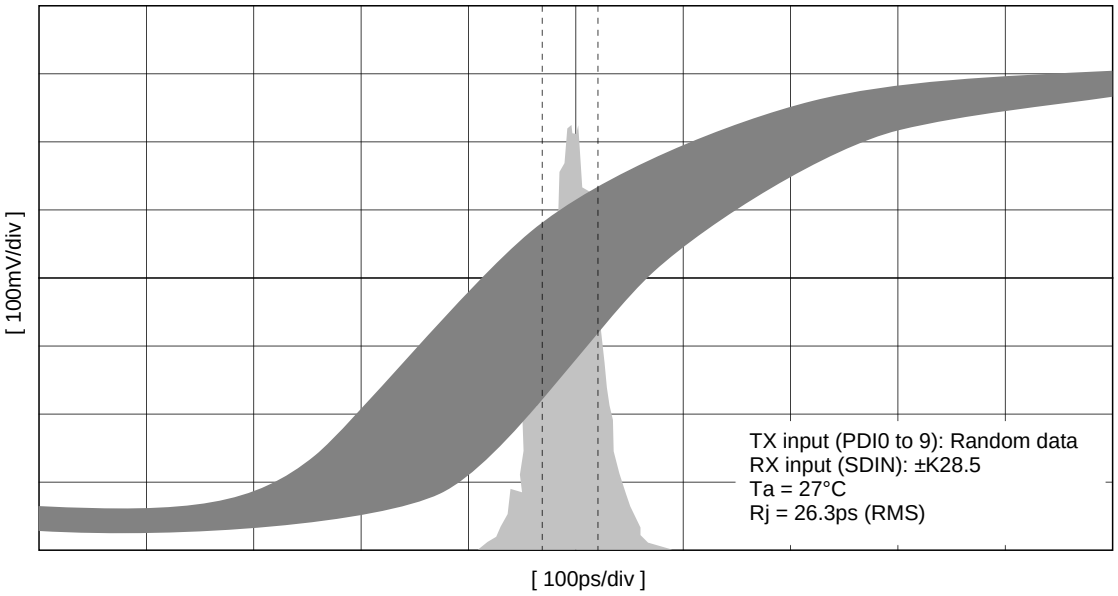


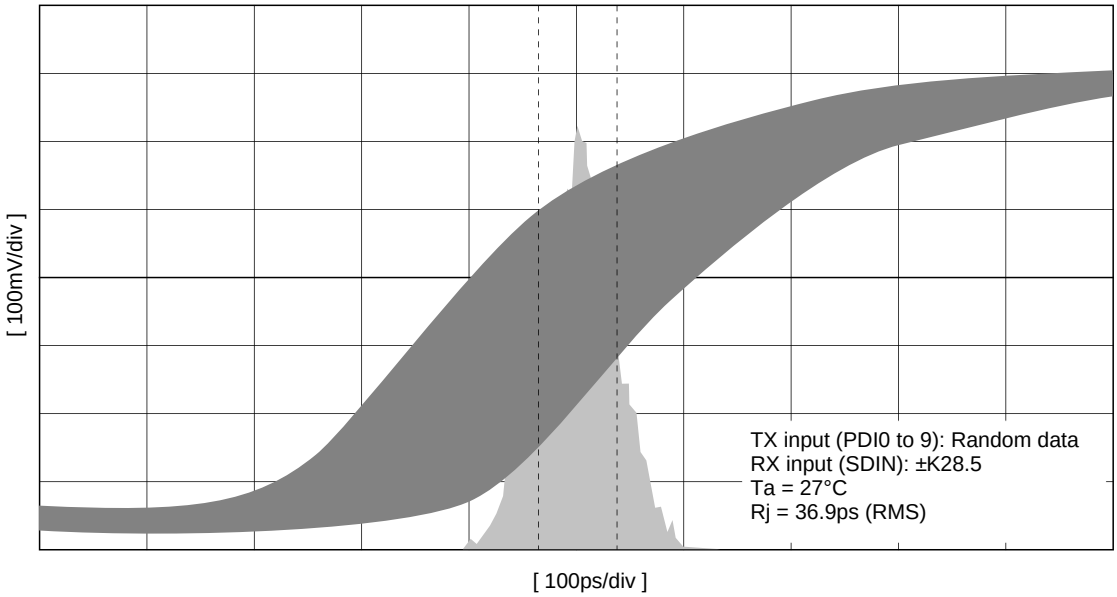
Fig. 4. Power-on reset signal

Example of Representative Characteristics

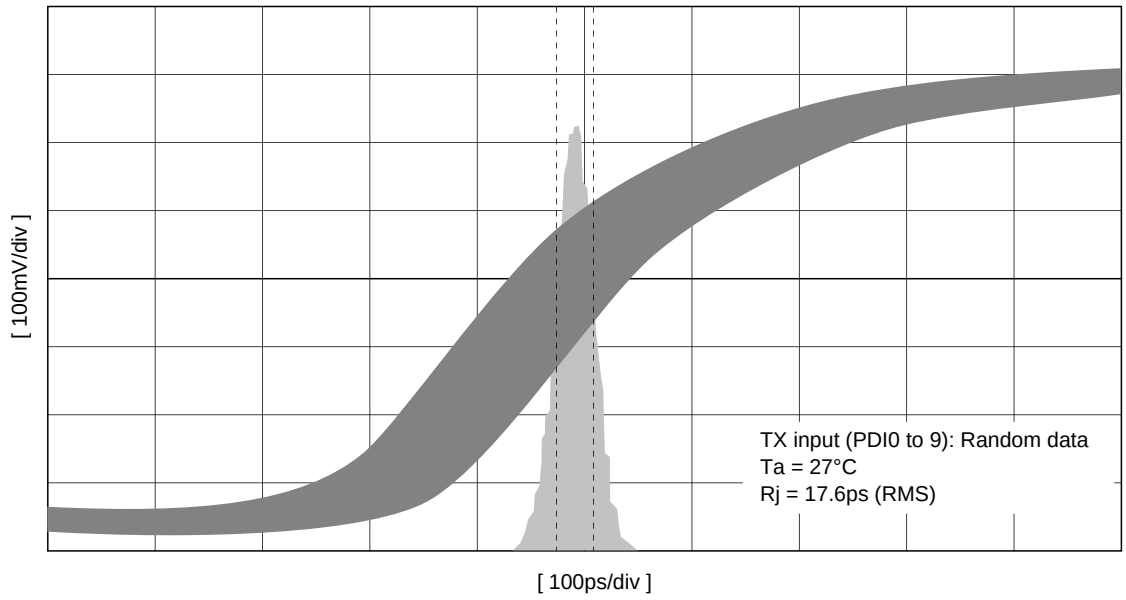
Example of Rj measurement (RX recovered clock, 266MHz operation)



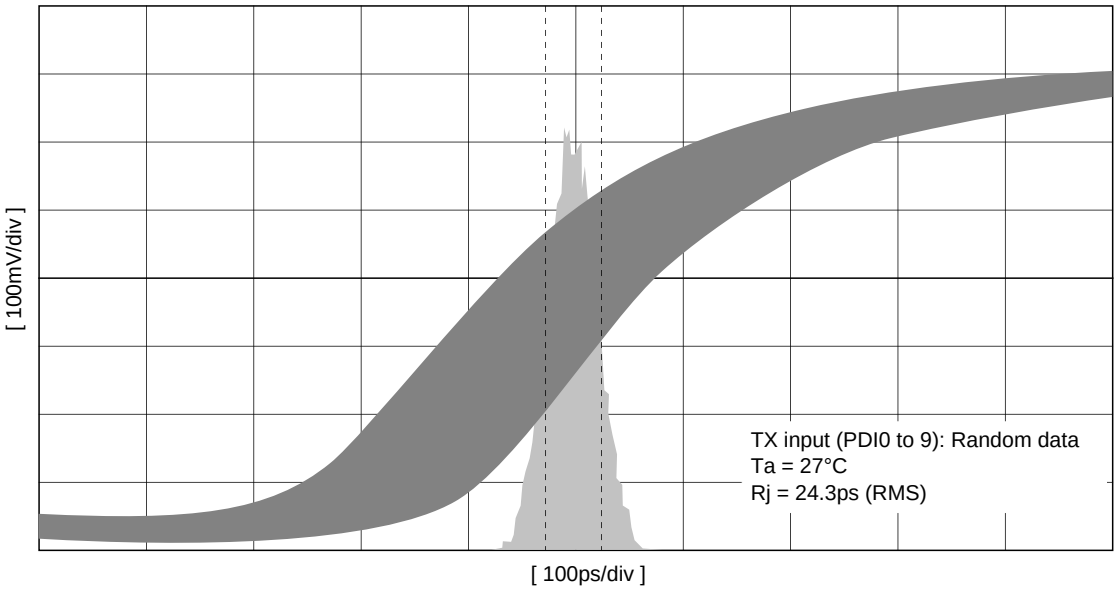
Example of Rj measurement (RX recovered clock, 200MHz operation)



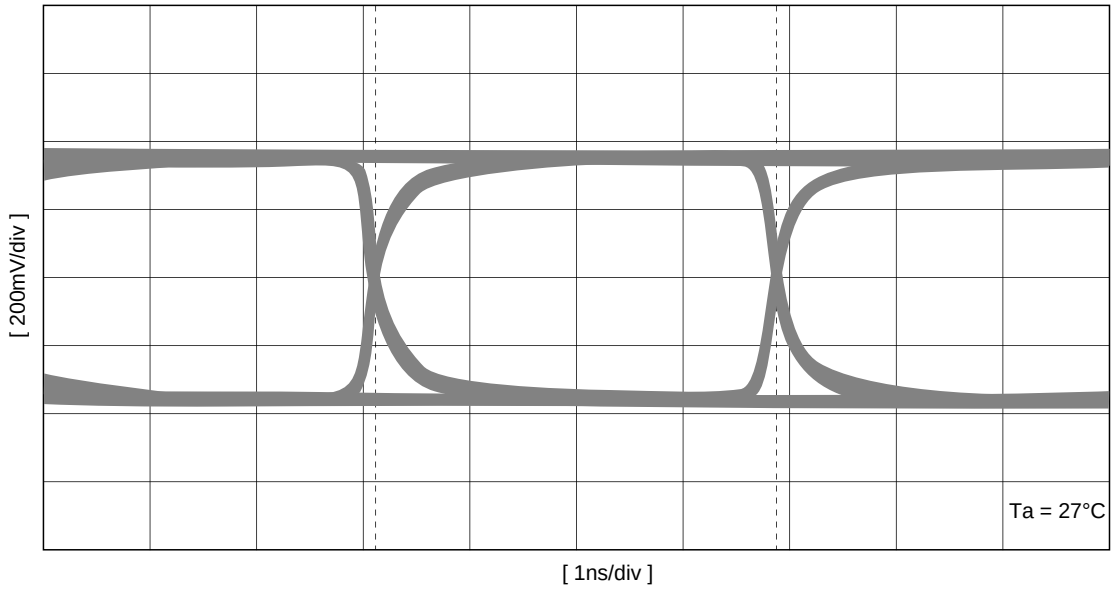
Example of Rj measurement (SDOUT, 266Mbps operation)



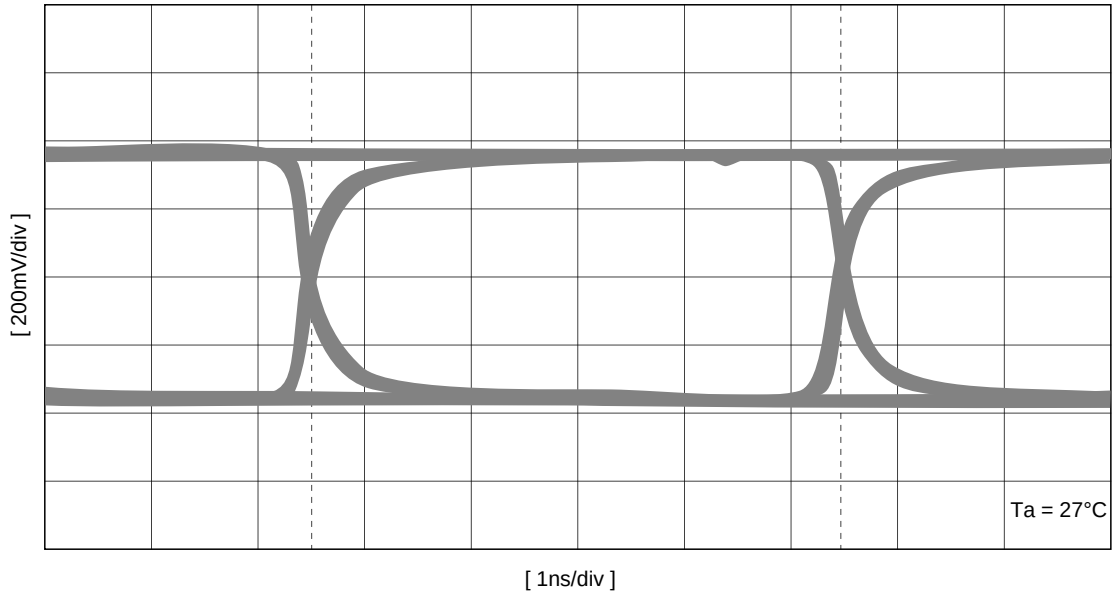
Example of Rj measurement (SDOUT 200Mbps operation)



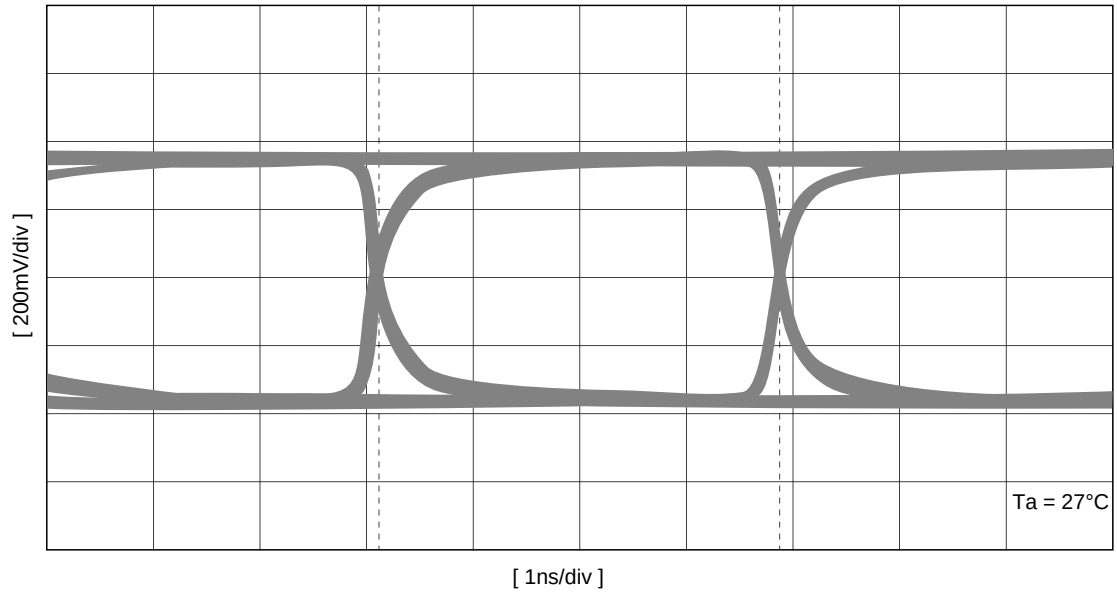
Eye pattern (TX SDOUT, 266Mbps operation)



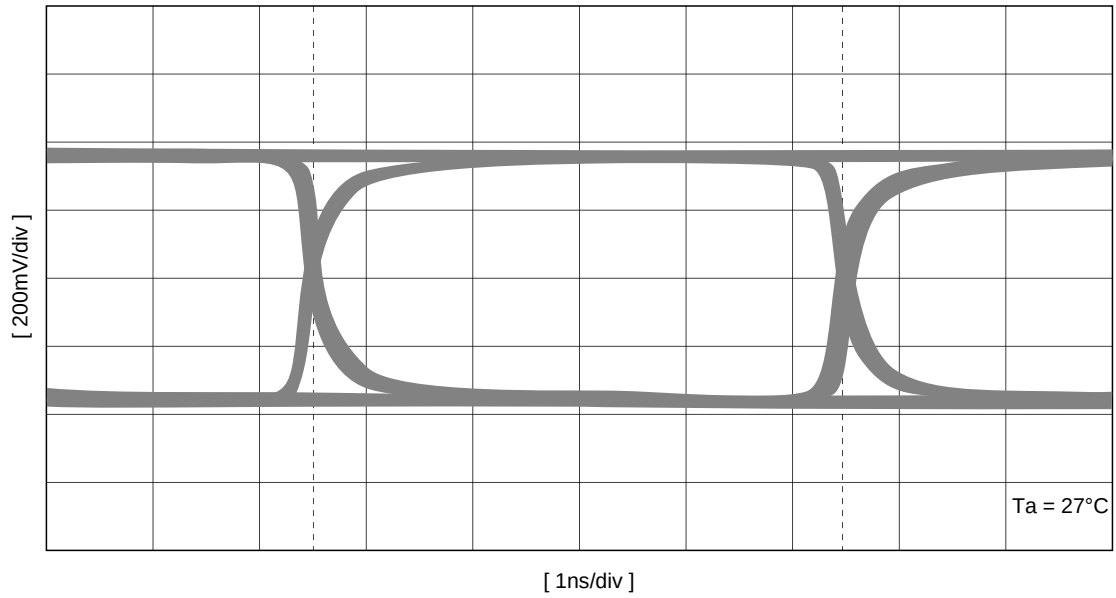
Eye pattern (TX SDOUT, 200Mbps operation)



Eye pattern (RX retimed data, 266Mbps operation)

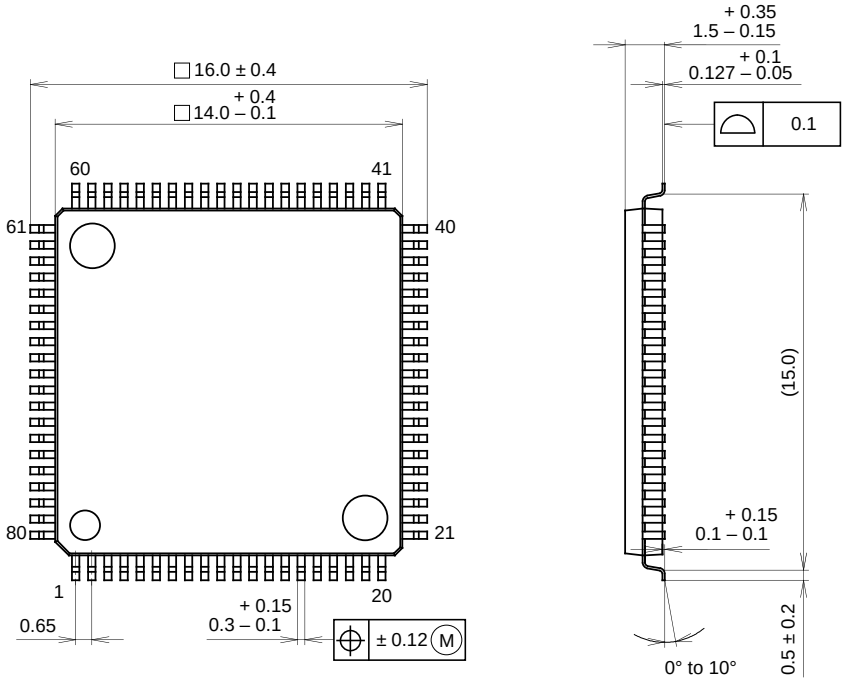


Eye pattern (RX retimed data, 200Mbps operation)



Package Outline Unit: mm

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.6g