

16 x 16-bit Parallel Multiplier

LMU17/217

FEATURES

- 45 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces AMD Am29517
- Single Clock Architecture with Register Enables
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
 - 64-pin Plastic DIP
 - 64-pin Sidebrazed, Hermetic DIP
 - 68-pin Plastic LCC, J-Lead
 - 68-pin Pin Grid Array
 - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The LMU17 and LMU217 are 16-bit parallel multipliers with high speed and low power consumption. They are pin and functionally compatible with AMD Am29517 devices. The LMU17 and LMU217 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU17 and LMU217 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded. Loading of the A and B registers is controlled by the

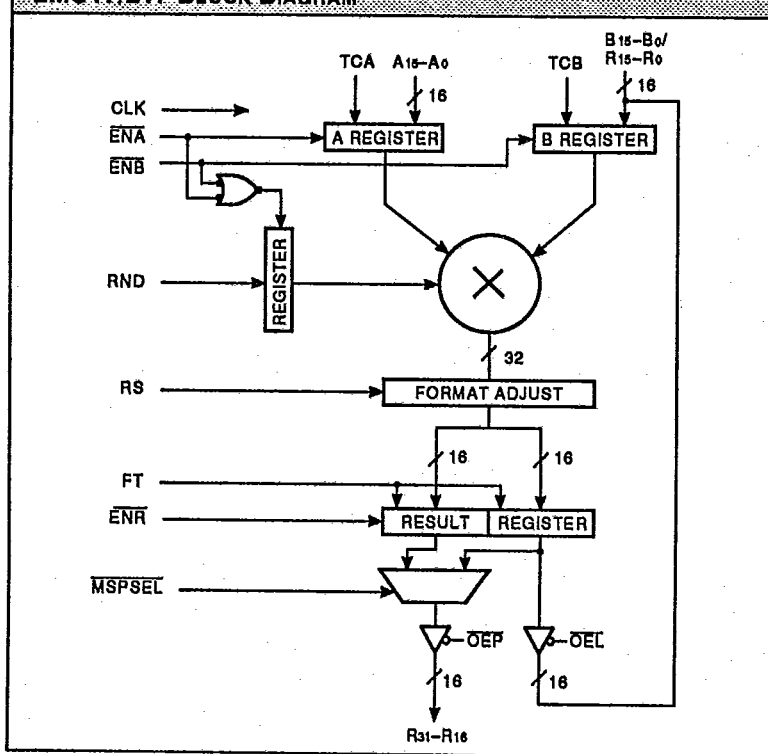
ENA and ENB controls. When high, these prevent application of the clock to the respective register. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of CLK, providing either ENA or ENB are low. RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB position of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the ENR control. When ENR is high, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. MSPSEL low causes the MSP outputs to be driven by the most significant half of the result. MSPSEL high routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B input port through a separate three-state buffer.

LMU17/217 BLOCK DIAGRAM



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16 x 16-bit Parallel Multiplier

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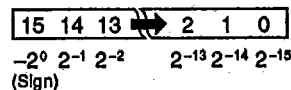
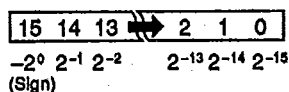
LMU17/217

INPUT FORMATS

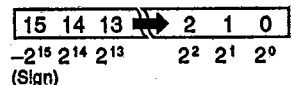
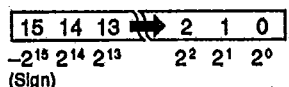
A1N

B1N

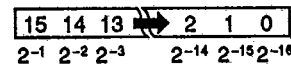
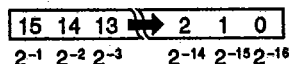
Fractional Two's Complement (TCA, TCB = 1)



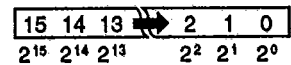
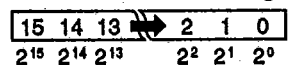
Integer Two's Complement (TCA, TCB = 1)



Unsigned Fractional (TCA, TCB = 0)



Unsigned Integer (TCA, TCB = 0)

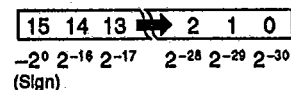
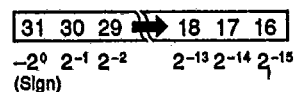


OUTPUT FORMATS

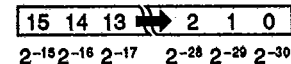
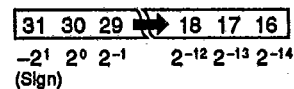
MSP

LSP

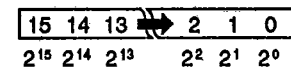
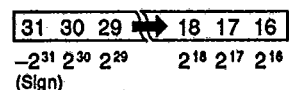
Fractional Two's Complement (RS = 0)



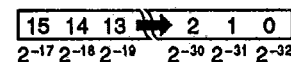
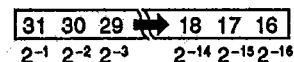
Fractional Two's Complement—Shifted (RS = 1)



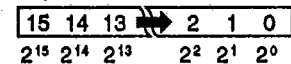
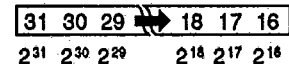
Integer Two's Complement (RS = 1)



Unsigned Fractional (RS = 1)



Unsigned Integer (RS = 1)



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LDS.17/217-A

MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
V _{CC} supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	I _{OH} = -2.0 mA	3.5			V
V _{OL}	Output Low Voltage	I _{OL} = 8.0 mA			0.5	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{IX}	Input Current	Ground ≤ V _{IN} ≤ V _{CC}			±20	μA
I _{OZ}	Output Leakage Current	Ground ≤ V _{OUT} ≤ V _{CC}			±20	μA
I _{OS}	Output Short Current	V _{OUT} = Ground, V _{CC} = Max (Notes 4, 8)			-250	mA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

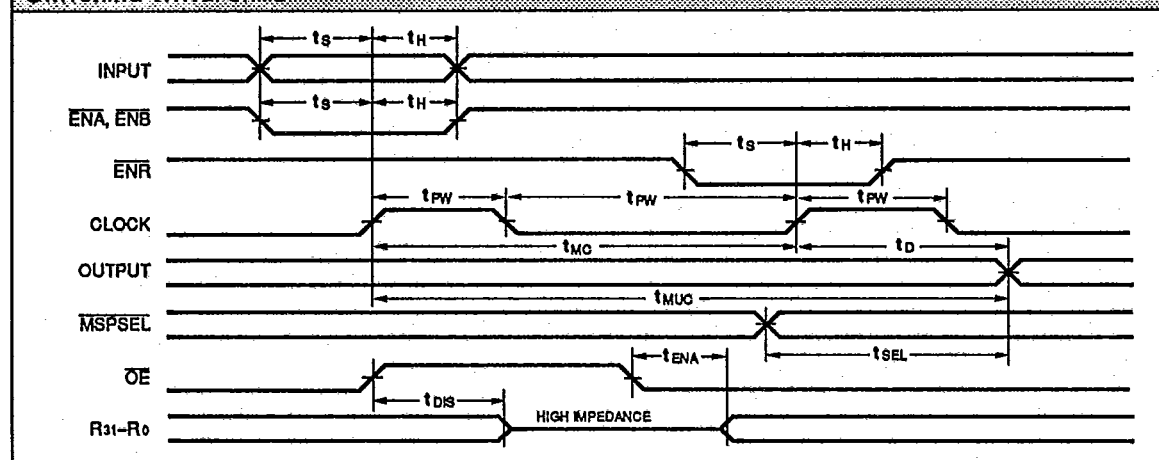
COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	LMU17/217-					
		65		55		45	
		Min	Max	Min	Max	Min	Max
t _{MC}	Multiply Time (Clocked)		65		55		45
t _{MUC}	Unclocked Multiply Time		85		75		65
t _D	Output Delay		30		30		30
t _{SEL}	Output Select Delay		25		25		25
t _{ENA}	Output Enable Time (Note 11)		25		25		25
t _{DIS}	Output Disable Time (Note 11)		25		25		25
t _{PW}	Clock Pulse Width	15		15		15	
t _H	Input Register Hold Time	3		3		3	
t _S	Input Register Setup Time	15		15		15	

MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LMU17/217-					
		75		65		55	
		Min	Max	Min	Max	Min	Max
t _{MC}	Multiply Time (Clocked)		75		65		55
t _{MUC}	Unclocked Multiply Time		95		85		75
t _D	Output Delay		35		30		30
t _{SEL}	Output Select Delay		30		30		30
t _{ENA}	Output Enable Time (Note 11)		25		25		25
t _{DIS}	Output Disable Time (Note 11)		25		25		25
t _{PW}	Clock Pulse Width	20		15		15	
t _H	Input Register Hold Time	3		3		3	
t _S	Input Register Setup Time	15		15		15	

SWITCHING WAVEFORMS

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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs

C = capacitive load per output

V = supply voltage

F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tEN/tDIS test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified IOL and IOH plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

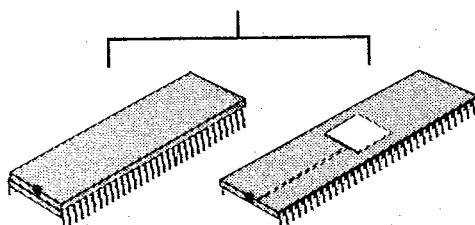
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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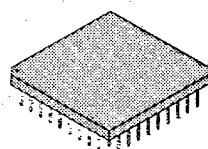
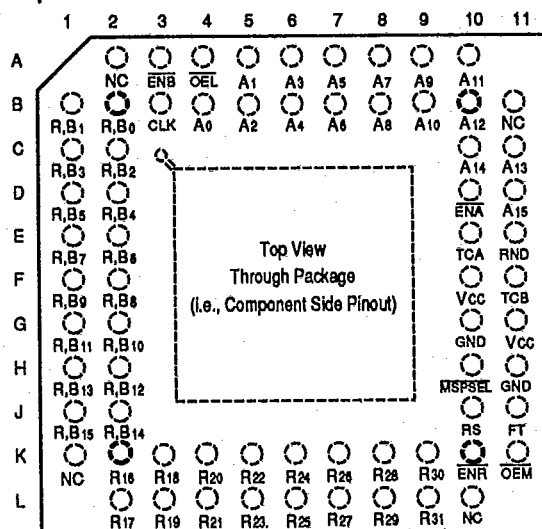
LMU17 — ORDERING INFORMATION

64-pin

A4	1	64	A5
A3	2	63	A6
A2	3	62	A7
A1	4	61	A8
A0	5	60	A9
OEL	6	59	A10
CLK	7	58	A11
ENB	8	57	A12
R0,B0	9	56	A13
R1,B1	10	55	A14
R2,B2	11	54	A15
R3,B3	12	53	ENA
R4,B4	13	52	RND
R5,B5	14	51	TCA
R6,B6	15	50	TCB
R7,B7	16	49	VCC
R8,B8	17	48	VCC
R9,B9	18	47	GND
R10,B10	19	46	GND
R11,B11	20	45	MSPSEL
R12,B12	21	44	FT
R13,B13	22	43	RS
R14,B14	23	42	OEM
R15,B15	24	41	ENR
R16	25	40	R31
R17	26	39	R30
R18	27	38	R29
R19	28	37	R28
R20	29	36	R27
R21	30	35	R26
R22	31	34	R25
R23	32	33	R24



68-pin



Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMU17PC65	LMU17DC65	LMU17GC65
55 ns	• • 55	• • 55	• • 55
45 ns	• • 45	• • 45	• • 45
-55°C to +125°C — COMMERCIAL SCREENING			
75 ns		LMU17DM75	LMU17GM75
65 ns		• • 65	• • 65
55 ns		• • 55	• • 55
-55°C to +125°C — EXTENDED SCREENING			
75 ns		LMU17DME75	LMU17GME75
65 ns		• • 65	• • 65
55 ns		• • 55	• • 55
-55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMU17DMB75	LMU17GMB75
65 ns		• • 65	• • 65
55 ns		• • 55	• • 55

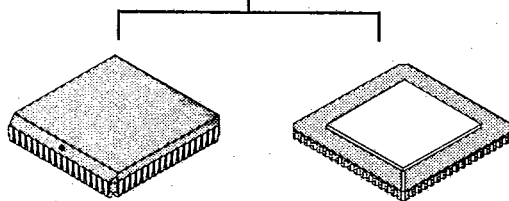
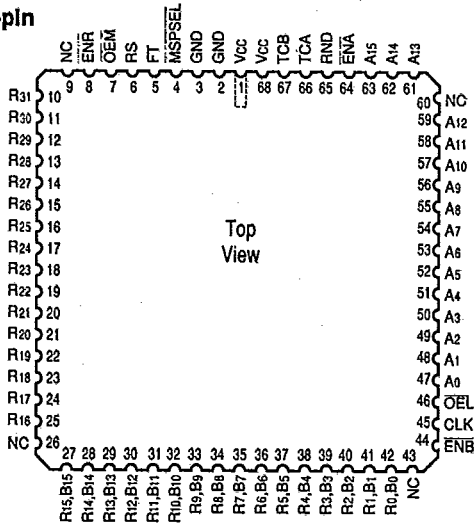
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LMU217 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMU217JC65	LMU217KC65		
55 ns	▪ ▪ 55	▪ ▪ 55		
45 ns	▪ ▪ 45	▪ ▪ 45		
	-55°C to +125°C — COMMERCIAL SCREENING			
75 ns		LMU217KM75		
65 ns		▪ ▪ 65		
55 ns		▪ ▪ 55		
	-55°C to +125°C — EXTENDED SCREENING			
75 ns		LMU217KME75		
65 ns		▪ ▪ 65		
55 ns		▪ ▪ 55		
	-55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMU217KMB75		
65 ns		▪ ▪ 65		
55 ns		▪ ▪ 55		

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