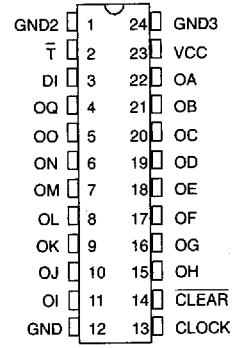
DALLAS SEMICONDUCTOR

DS129x Eliminator

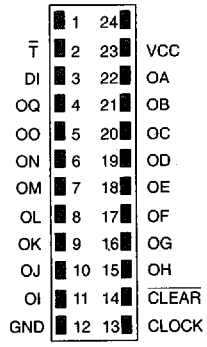
FEATURES

- Replaces 8 or 16 hard-to-get-at manual switches
- Options printed circuit board via software
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Serial Interface Chip
- Low-power CMOS
- Switch setting changes occur simultaneously
- DS1290 and DS1292 maintain settings in the absence of power; DS1291 and DS1293 are volatile
- Over 10 years of data retention for DS1290 and DS1292

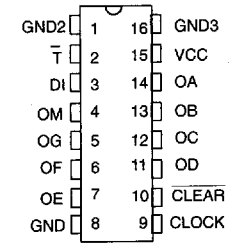
PIN ASSIGNMENT



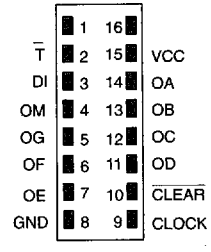
DS1293 24-Pin DIP (300 Mil) See Mech. Drawings Section



DS1292 24-Pin Encapsulated Package (450 Mil) See Mech. Drawings Section



DS1291 16-Pin DIP (300 Mil) See Mech. Drawings Section



DS1290 16-Pin Encapsulated Package (450 Mil) See Mech. Drawings Section

DESCRIPTION

The DS129x Eliminator replaces manual switches used to option printed circuit boards. Up to sixteen output pins can be set to a logic level or interrogated by three signals: clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 and DS1292 will maintain high or low level outputs, duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

PIN DESCRIPTION

$\overline{T}$	–	Transfer
DI	–	Data Input
O_A–O_Q	–	Switch Outputs
CLOCK	–	Clock Input
$\overline{CLEAR}$	–	All Outputs Set Low
V_{CC}	–	+5 Volts
GND	–	Ground
GND2	–	Missing on DS1292. Must be grounded on DS1293.
GND3	–	Missing on DS1292. Must be grounded on DS1293.

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OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control (see "Block Diagram" in Figure 1). The DS1290/DS1291 Eliminator is an 8-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control. Data can be entered into the registers only when the transfer input ($\overline{T}$) is at a high level. While at a high level, the transfer function allows serial entry of data via the data input pin (DI). The outputs 0_Q through 0_B remain in the state that was set prior to $\overline{T}$ being driven to a high level. Output 0_A will change state as new data is entered. This output provides a method of feeding back actual output settings prior to setting the $\overline{T}$ input low (Figure 2). When the $\overline{T}$ input is driven low, new data that has been input into the 16-bit shift register is now locked at outputs 0_Q through 0_A. When the $\overline{T}$ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while $\overline{T}$ is high on the low-to-high transition of the CLOCK input. Data can be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The $\overline{CLEAR}$ input will always set all outputs to low level regardless of the level of the CLOCK or $\overline{T}$ input.

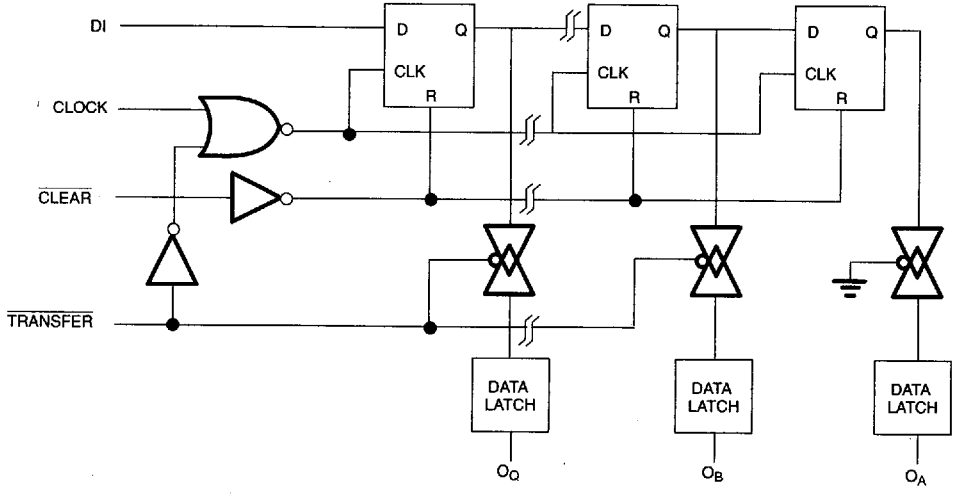
DATA RETENTION MODE

The DS129x Eliminator provides full functional capability when V_{CC} is greater than 4.5 volts and will ignore all inputs when V_{CC} reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As V_{CC} falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power-up when V_{CC} rises above approximately 3 volts, the power switching circuit connects external V_{CC} to the shift register and disconnects the lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for 10 ms minimum. During power transients the 16 outputs will track the level of V_{CC} if set to logic 1 and will remain at ground level if set to Logic 0.

TYPICAL APPLICATION – ELIMINATOR

The DS129x and DS1206 combine to make a programmable nonvolatile DIP switch that can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, they need only be set once; they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Serial Interface Chip. The DS1206 samples four address lines and the chip enable signal looking for a special pattern for 24 consecutive cycles (see the DS1206 data sheet). When a proper match is found, the address lines and one data line become control and data signals that are used to program and verify the settings of the DS129x. All of the signaling sent to the DS1206 and subsequently to the DS1292 is generated by software-controlled read cycles that have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

BLOCK DIAGRAM - DS129x Figure 1



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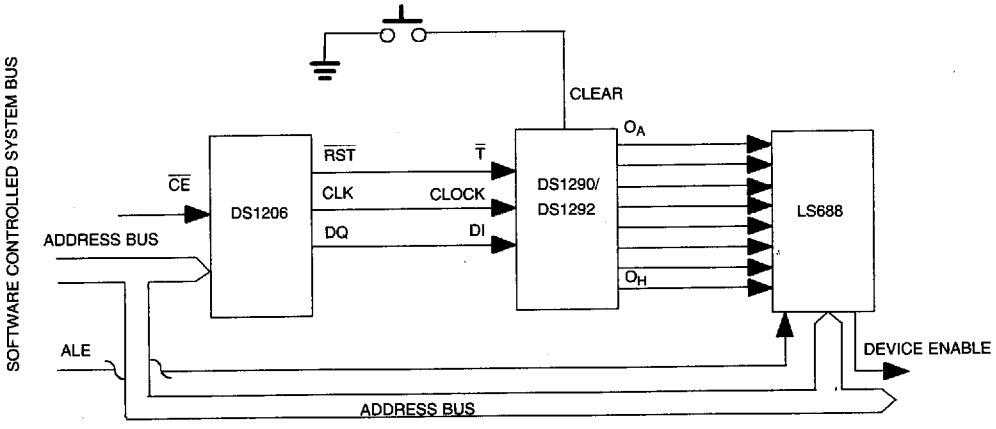
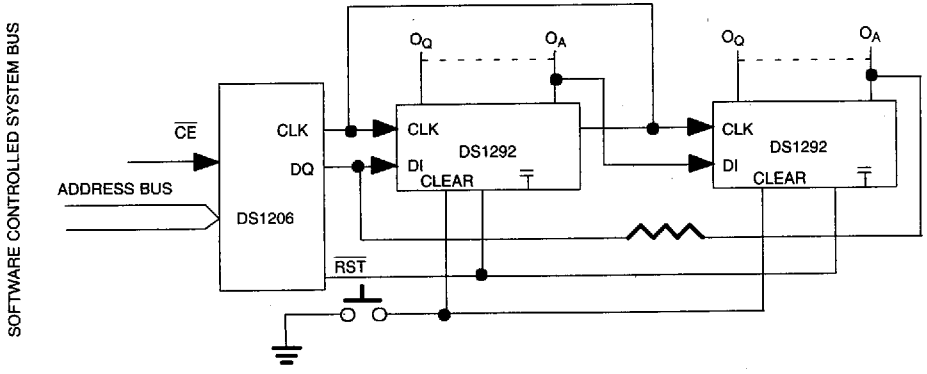
PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



MODULAR EXPANSION OF THE ELIMINATOR Figure 3



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		3	5	mA	
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Logic 1 Output @ 2.4V	I_{OH}	-1.0			mA	2
Logic 0 Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLOCK}			10	MHz	
Width of Clock Pulse	tw_{CLOCK}	50			ns	3
Width of Clear Pulse	tw_{CLEAR}	50			ns	3
Data Setup Time	t_{SU}	30			ns	3
Data Hold Time	t_H	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	t_{PHLC}			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3

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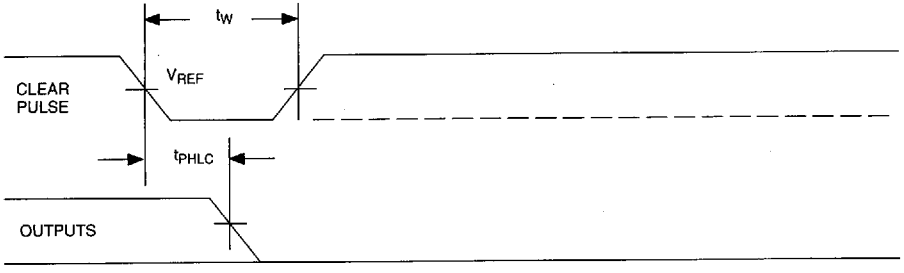
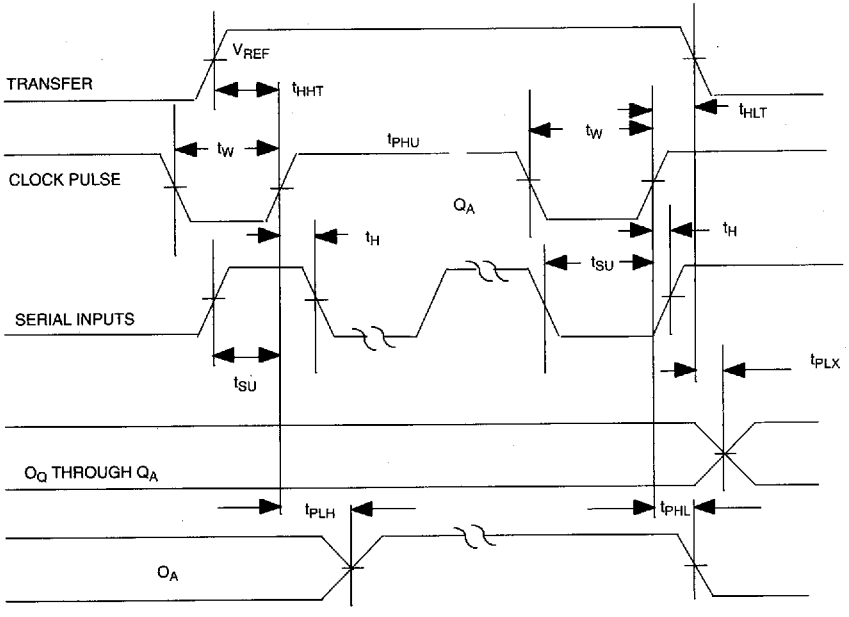
AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			50	ns	3
Recovering on Power-Up	t_{REC}	10			ms	
Propagation Delay Time High to Low Level Transfer to O Out	t_{PLX}			50	ns	3
Transfer High to Clock Input High	t_{HHT}	50			ns	3
Transfer Low from Clock Input High	t_{HLT}	50			ns	3

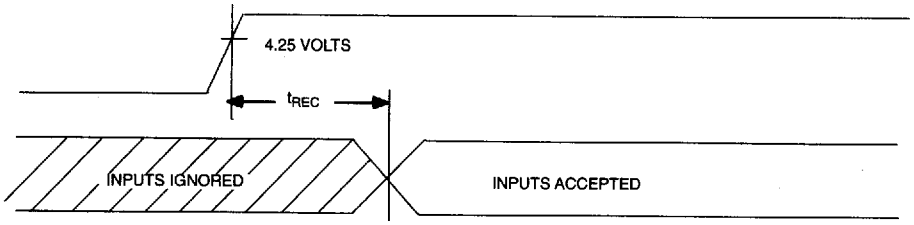
TIMING DIAGRAM: CLEAR CONTROL (3)



TIMING DIAGRAM: TRANSFER DATA (3)



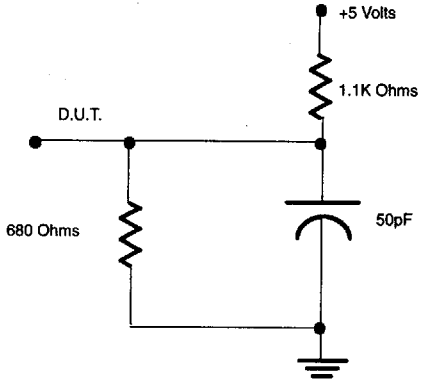
TIMING DIAGRAM: POWER-UP (3)



NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. V_{REF} = 1.5 volts.
4. Clock and transfer inputs have internal pull-down resistors of 20K ohms typical. Clear has an internal pull-up resistor of 20K ohms typical.

OUTPUT LOAD Figure 4



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