CMOS 8-BIT MICROCONTROLLERS
TMP90C840AN/TMP90C841AN
TMP90C840AF/TMP90C841AF

1. OUTLINE AND CHARACTERISTICS

The TMP90C840A is a high-speed advanced 8-bit micro controller applicable to a variety of equipment.

With its 8-bit CPU, ROM, RAM, A/D converter, multi-function timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90C840A allows the expansion of external memories for programs (up to 56K byte) and data (1M byte). The TMP90C841A is the same as the TMP90C840A but without the ROM.

The TMP90C840AN/841AN is a 64-pin shrink DIP product. (SDIP64-P-750)
The TMP90C840AF/841AF is a 64-pin flat package product. (QFP64-P-1420A)

The characteristics of the TMP90C840A include:

(1) Powerful instructions: 163 basic instructions, including
Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions

(2) Minimum instruction executing time: 320 ns (at 12.5 MHz oscillation frequency)

(3) Internal ROM: 8K byte (The TMP90C841A does not have a built-in ROM.)

(4) Internal RAM: 256 byte

(5) Memory expansion
Program memory: 64K byte
Data memory: 1M byte

(6) 8-bit A/D converter (6 channels)

(7) General-purpose serial interface (1 channel)
Asynchronous mode, I/O interface mode

(8) Multi-function 16-bit timer/event counter (1 channel)

(9) 8-bit timers (4 channel)

(10) Stepping motor control port (2 channel)

(11) Input/Output ports (90C840A: 54 pins, 90C841A: 28pins)

(12) Interrupt function: 10 internal interrupts and 4 external interrupts

(13) Micro Direct Memory Access (DMA) function (11 channels)

(14) Watchdog timer

(15) Standby function (4 HALT mode)

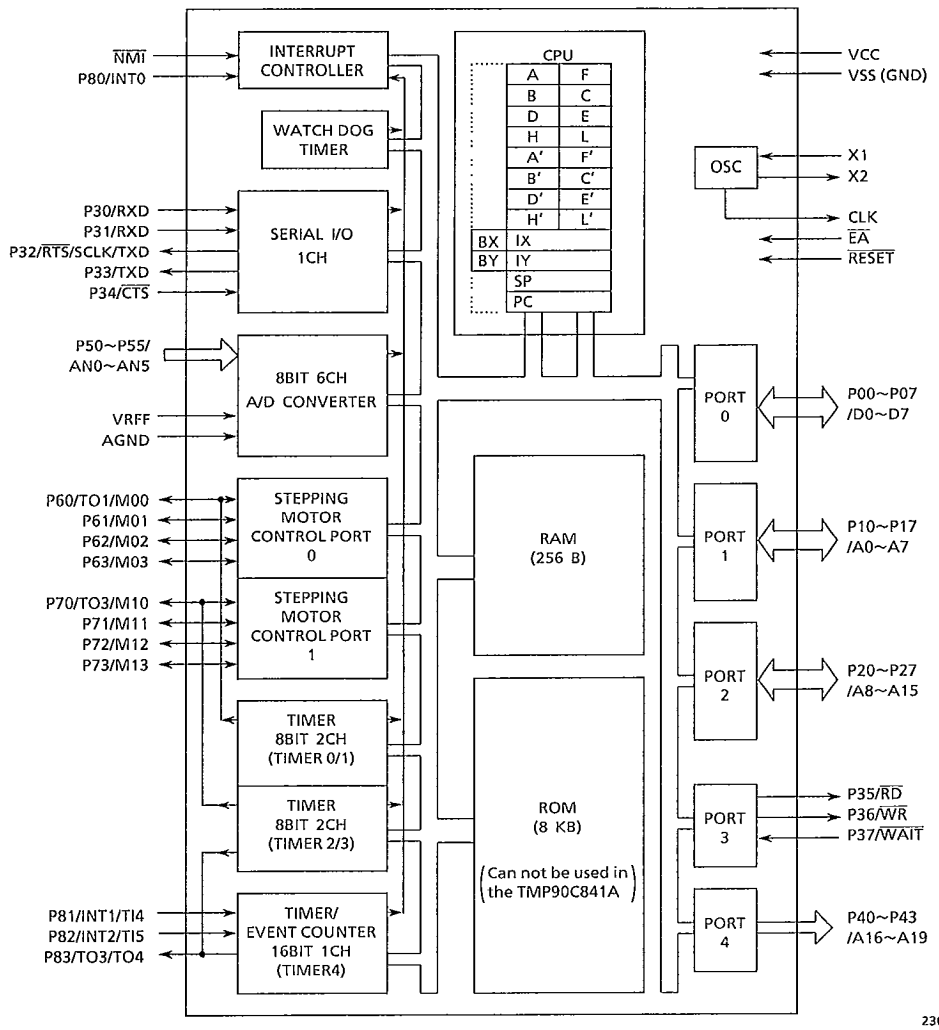

Figure 1 TMP90C840A Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1-(1)shows pin assignment of the TMP90C840AN/841AN.

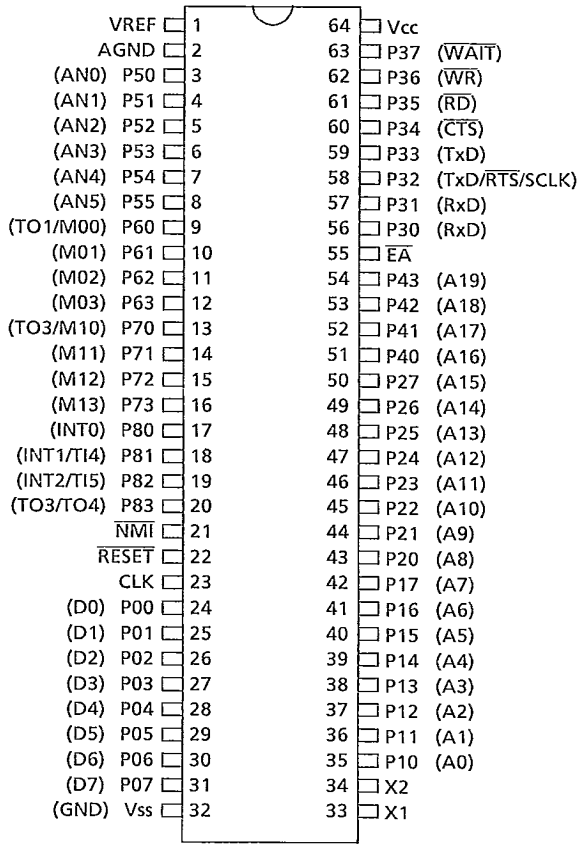

Figure 2.1- (1) Pin Assignment (Shrink Dual Inline Package)

Figure 2.1-(2) shows pin assigunment of the TMP90C840AF/841AF.

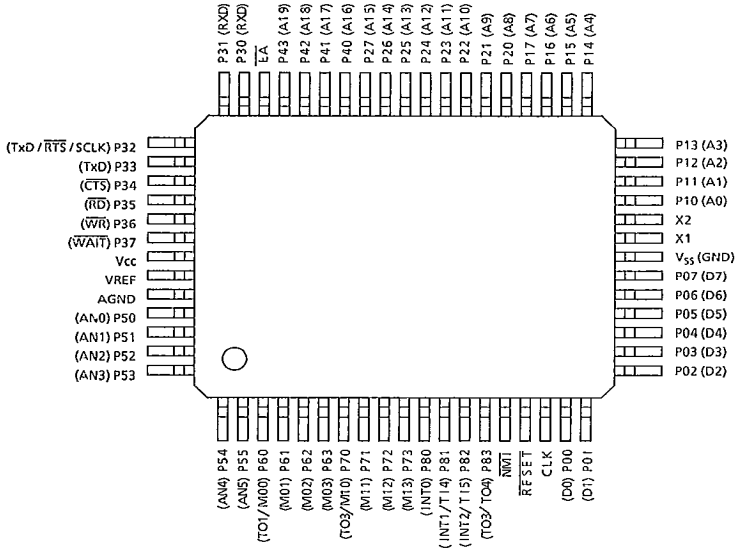

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Figure 2.1- (2) Pin Assignment (Flat Package)

2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
P00~P07	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
/D0~D7		3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10~P17	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
/A0~A7		Output	Address bus: The lower 8 bits address bus for external memory
P20~P27	8	I/O	Port 2: 8-bit I/O port that allows selection on bit basis
/A8~A15		Output	Address bus: The upper 8 bits address bus for external memory
P30	1	Input	Port 30: 1-bit input port
/RxD			Receiver Serial Data
P31	1	Input	Port 31: 1-bit input port
/RxD			Receiver Serial Data
P32	1	Output	Port 32: 1-bit output port
/TxD			Transmitter serial Data
/$\overline{RTS}$			Request to send serial data
/SCLK			Serial clock output
P33	1	Output	Port 33: 1-bit output port
/TxD			Transmitter Serial Data
P34	1	Input	Port 34: 1-bit input port
/$\overline{CTS}$			Clear to send Serial data
P35	1	Output	Port 35: 1-bit output port
/$\overline{RD}$			Read: Generates strobe signal for reading external memory
P36	1	Output	Port 36: 1-bit output port
/$\overline{WR}$			Write: Generates strobe signal for writing into external memory
P37	1	Input	Port 37: 1-bit input port
/$\overline{WAIT}$			Wait: Input pin for connecting slow speed memory or peripheral LSI
P40~P43	4	Output	Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis
/A16~A19			Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50~P55	6	Input	Port 5: 6-bit input port
/AN0~AN5			Analog input: 6 analog inputs to A/D converter
VREF	1		Input of reference voltage to A/D converter

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Table 2.2 Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
AGND	1		Ground pin for A/D converter
P60~P63 /M00~M03 /TO1	4	I/O	Port 6: 4-bit I/O port that allows I/O selection on bit basis
		Output	Stepping motor control port 0
		Output	Timer output 1: Output of Timer 0 or 1
P70~P73 /M10~M13 /TO3	4	I/O	Port 7: 4-bit I/O port that allows I/O selection on bit basis
		Output	Stepping motor control port 1
		Output	Timer output 3: Output of Timer 2 or 3
P80 /INT0	1	Input	Port 80: 1-bit input port
			Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable)
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port
			Interrupt request pin 1: interrupt request pin (Rising/falling edge is programmable)
			Timer input 4: Counter/capture trigger signal for Timer 4
P82 /INT2 /TI5	1	Input	Port 82: 1-bit input port
			Interrupt request pin 2: rising edge interrupt request pin
			Timer input 5: capture trigger signal for Timer 4
P83 /TO3 /TO4	1	Output	Port 83: 1-bit output port
			Timer output 3/4: Output of Timer 2, 3 or 4
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
$\overline{EA}$	1	Input	External access: Connects with Vcc pin in the TMP90C840A using internal ROM, and with GND pin in the TMP90C841A with no internal ROM.
$\overline{RESET}$	1	Input	Reset : Initializes the TMP90C840A/841A. (Built-in pull-up resister)
X1/X2	2	Input/ Output	Pins for quartz crystal or ceramic resonator
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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3. OPERATION

This chapter describes the functions and the basic operations of the TMP90C840A /841A in every block.

The following is a description of TMP90C840A which can also be applied to TMP90C841A, if not specifically defined otherwise.

3.1 CPU

TMP90C840A includes a high performance 8 bit CPU. For the function of the CPU, see the previous chapter "TLCS-90 CPU". This chapter explains exclusively the functions of the CPU of TMP90C840A which are not described in the chapter "TLCS-90 CPU".

3.1.1 Reset

The basic timing of the reset operation is indicated in Figure 3.1 (1). In order to reset the TMP90C840A, the $\overline{\text{RESET}}$ input must be maintained at the "0" level for at least ten system clock cycles (10 states : 2 μsec at 10 MHz) within an operating voltage band and with a stable oscillation. When a reset request is accepted, all I/O ports (Port 0 /data bus D0 to D7, Port 1/address bus A0 to A7, Port 2/address bus A8 to A15, Port 6 and Port 7) function as input ports (high impedance state). The P35 ($\overline{\text{RD}}$), P36 ($\overline{\text{WR}}$) and CLK pins that always function as output ports turn to the "1" level, and the other output ports (Port 4/address bus A16 to A19 and P83) turn to the "0" level. The dedicated input ports remain unchanged. The registers of the CPU also remain unchanged. Note, however, that the program counter PC, the interrupt enable flag IFF and the bank registers BX and BY are cleared to "0". Register A shows an undefined status.

When the reset is cleared, the CPU starts executing instructions from the address 0000H.

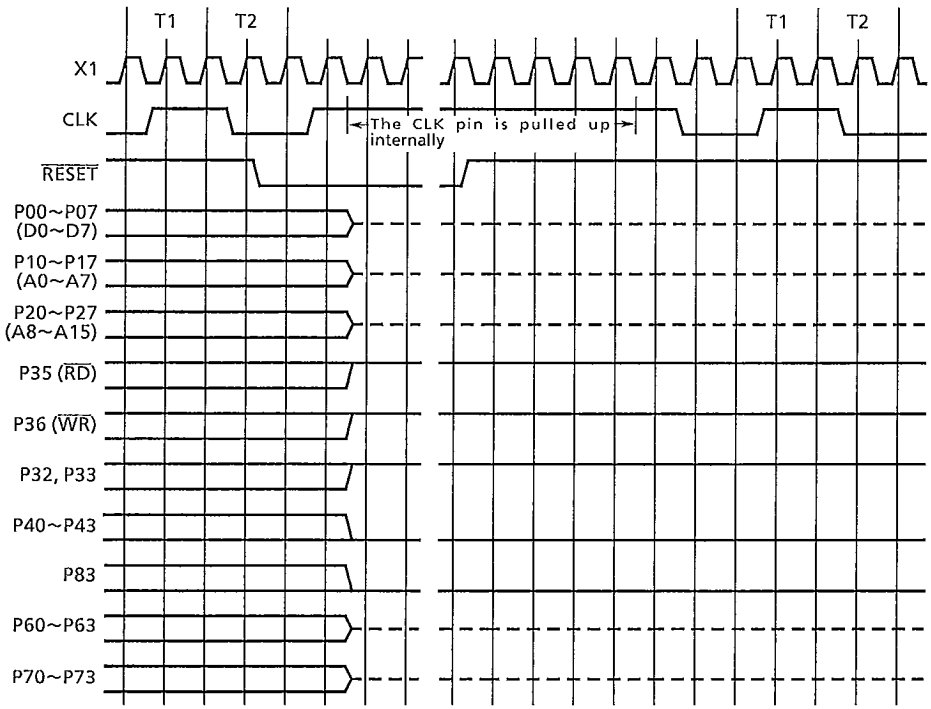

Figure 3.1 (1a) TMP90C840A Reset Timing

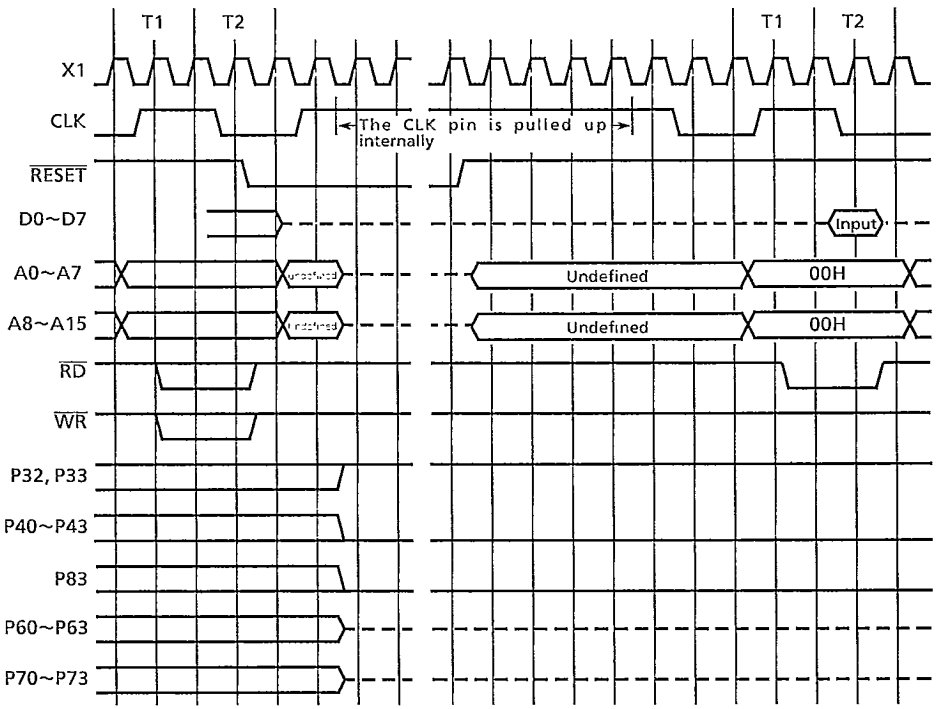

Figure3.1 (1b) TMP90C841A Reset Timing

3.1.2 EXF (Exchange Flag)

For TMP90C840A, "EXF", which is inverted when the command "EXX" is executed to transfer data between the main register and the auxiliary register, is allocated to the first bit of memory address FFD2H.

WDMOD (FFD2H)	7	6	5	4	3	2	1	0
bit Symbol	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	EXF	DRIVE
Read/Write	R/W	R/W		R/W	R/W		R	R/W
Resetting Value	1	0	0	0	0	0	Undefined	0
Function	1 : WDT Enable	WDT Detecting time 00: 2^{17}/fc 01: 2^{15}/fc 10: 2^{13}/fc 11: 2^{27}/fc		Warming up time 0: 2^{14}/fc 1: 2^{16}/fc	Standby mode 00: RUN mode 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode		Invert each time EXX instruction is executed	1: to drive pins in STOP mode

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3.1.3 Wait Control

For TMP90C840A, a wait control register (WAITC) is allocated to the 6th and 7th bits of memory address FFC7H.

P3CR (FFC7H)

	7	6	5	4	3	2	1	0
bit Symbol	WAITC1	WAITC0	RDE	ODE	TXDC1	TXDC0	RXDC1	RXDC0
Read/Write	R/W		R/W	R/W	R/W		R/W	
Resetting Value	0	0	0	0	0	0	0	0
Function	Wait control 00: 2state wait 01: normal wait 10: non wait 11: reserved		RD control 0: $\overline{RD}$ for only external access 1: Always $\overline{RD}$	P33 control 0: CMOS 1: Open drain	P33 00: Out 01: Out 10: TxD 11: TxD	P32 Out TxD Out $\overline{RTS}$/SCLK	P31 00: In 01: In 10: RxD 11: Not used	P30 In RxD In

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3.1.4 Bank Register

For TMP90C840A, BX and BY registers are allocated to memory addresses FFECH (BX register) and FFEDH (BY register), respectively. In these registers, only the low-order 4 bits are valid, and the high-order 4 bits are undefined. These undefined bits become "1" whenever they are read.

BX (FFECH)

	7	6	5	4	3	2	1	0
bit Symbol					BX3	BX2	BX1	BX0
Read/Write					R/W			
Resetting Value					0	0	0	0

BY (FFEDH)

	7	6	5	4	3	2	1	0
bit Symbol					BY3	BY2	BY1	BY0
Read/Write					R/W			
Resetting Value					0	0	0	0

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3.2 Memory Map

The TMP90C840A supports a program memory of up to 64K bytes and a data memory of maximum 1M bytes.

The program memory may be assigned to the address space from 00000H to 0FFFFH, while the data memory can be allocated to any address from 00000H to FFFFFH.

(1) Internal ROM

The TMP90C840A internally contains an 8K-byte ROM. The address space from 0000H to 1FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses 0010H to 007FH in this internal ROM area are used for the entry area for the interrupt processing.

The TMP90C841A does not have a built-in ROM; therefore, the address space 0000H ~1FFFH is used as external memory space.

(2) Internal RAM

The TMP90C840A also contains a 256 byte RAM, which is allocated to the address space from FEC0H to FFBFH. The CPU allows the access to a certain RAM area (FF00H to FFBFH, 192 bytes) by a short operation code (opcode) in a "direct addressing mode".

The addresses from FF10H to FF7FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O

The TMP90C840A provides a 48-byte address space as an internal I/O area, whose addresses range from FFC0H to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3.2 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

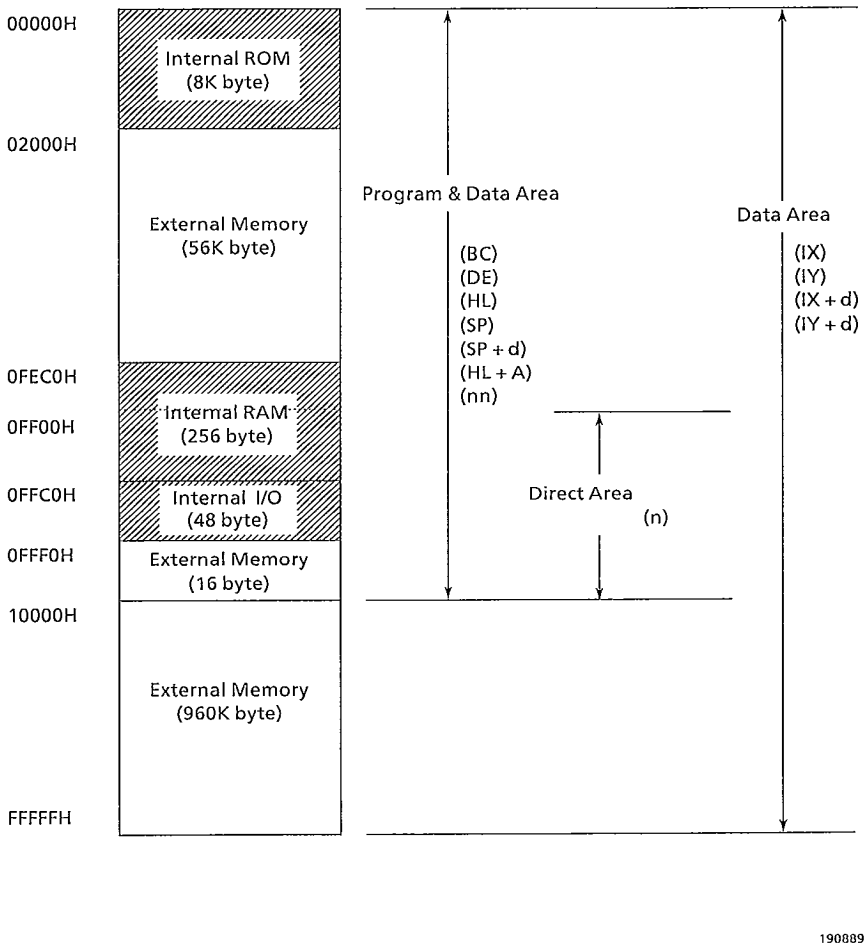

Figure 3.2 Memory Map

3.3 Interrupt Functions

The TMP90C840A supports a general purpose interrupt processing mode and a micro DMA processing mode that enables automatic data transfer by the CPU for internal and external interrupt requests. After the reset state is released, all interrupt requests are processed in the general purpose interrupt processing mode. However, they can be processed in the micro DMA processing mode by using a DMA enable register to be described later.

Figure 3.3 (1) is a flowchart of the interrupt response sequence.

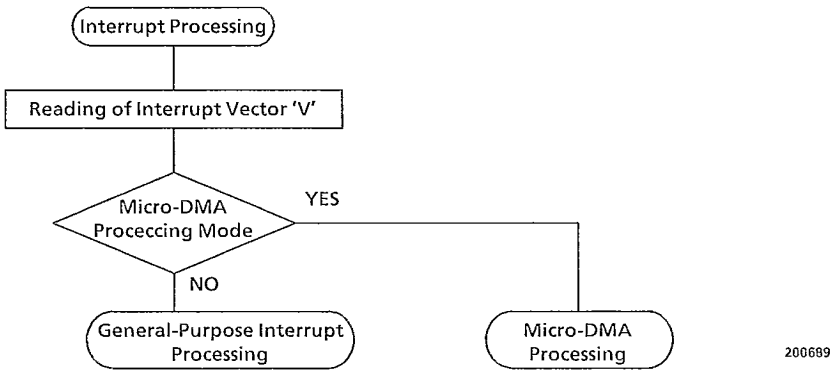

Figure 3.3 (1) Interrupt Response Flowchart

When an interrupt is requested, the source of the interrupt transmits the request to the CPU via an internal interrupt controller. The CPU starts the interrupt processing if it is a non-maskable or maskable interrupt requested in the EI state (interrupt enable flag (IFF) ="1"). However, a maskable interrupt requested in the DI state (IFF="0") is ignored. An interrupt request is sampled by the CPU at the falling edge of the CLK signal in the last bus cycle of each instruction.

Having acknowledged an interrupt, the CPU reads out the interrupt vector from the internal interrupt controller to find out the interrupt source.

Then, the CPU checks if the interrupt requests the general purpose interrupt processing or the micro DMA processing, and proceeds to each processing.

As the reading of an interrupt vecotors is performed in the internal operating cycles, the bus cycle results in dummy cycles.

3.3.1 General Purpose Interrupt Processing

A general purpose interrupt is processed as shown in Figure 3.3. (2).

The CPU stores the contents of the program counter PC and the register pair AF (including the interrupt enable flag (IFF) before the interrupt) into the stack, and resets the interrupt enable flag IFF to "0" (disable interrupts). In then transfers the value of the interrupt vector "V" to the program counter, and the processing jumps to an interrupt processing program.

The overhead for the entire process from accepting an interrupt to jumping to an interrupt processing program is 20 states.

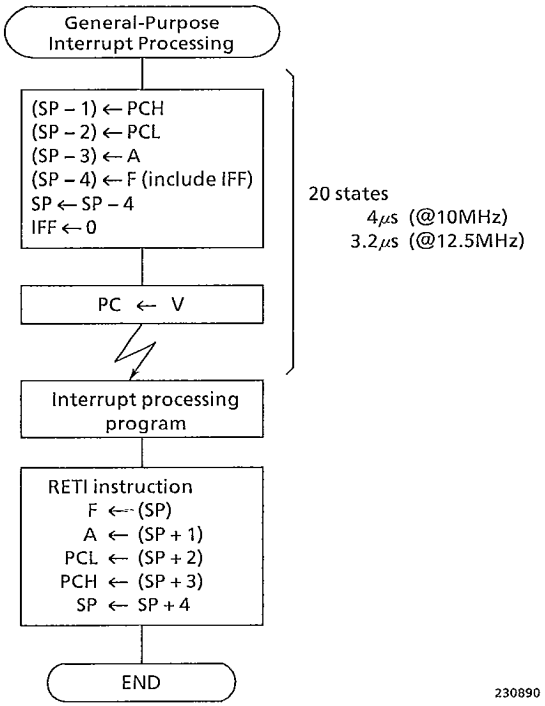

Figure 3.3 (2) General Purpose Interrupt Processing Flowchart

An interrupt (Maskable and Nonmaskable) processing program ends with a RETI instruction.

When this instruction is executed, the data previously stacked from the program counter PC and the register pair AF are restored. (Returns to the interrupt enable flag (IFF) before the interrupt.)

After the CPU reads out the interrupt vector, the interrupt source acknowledges that the CPU accepts the request, and clears the request.

A non-maskable interrupt cannot be disabled by programming. A maskable interrupt, on the other hand, can be enabled or disabled by programming. An interrupt enable flip flop (IFF) is provided on the bit 5 of Register F in the CPU. The interrupt is enabled or disabled by setting IFF to "1" by the EI instruction or to "0" by the DI instruction, respectively. IFF is reset to "0" by the reset operation or the acceptance of any interrupt (including non-maskable interrupt). The interrupt can be enabled after the subsequent instruction of EI instruction is executed.