Rockwell

Advanced FAXENGINE™ Family

INTRODUCTION

The Advanced FAXENGINE™ family provides a complete set of facsimile machine functions integrated into a two-device set. Each FAXENGINE consists of one of two Integrated Facsimile Controllers (IFC) and one of four synchronous half-duplex facsimile modems, as shown in Table 1, providing the OEM with great flexibility in producing a robust line of facsimile machines.

The IFC performs the primary facsimile machine control and monitoring functions interfacing with major fax machine components. The MC24™ embedded processor provides a 16M byte direct memory accessing capability, which combined with the IFC's integrated DRAM controller, provides support for page memory features such as out-of-paper receive, memory polling, broadcasting, confidential transmission, and relay transmission. Scanner, printer, and keyboard interfaces, as well as motor control and the modem interface, are included. These programmable functions and interfaces support a wide range of hardware peripherals. T.4 (MH/MR) and T.6 (MMR) image compression functions are performed in IFC hardware.

An integrated flash ADC, combined with Rockwell's Proprietary Image Corrections System (RPICS™), provides state-of-the-art image processing performance on both text and half tone images.

Four different MONOFAX® modems are available with selection depending upon the desired applications. The R96DFXL and R144EFXL support V.29 and V.17 fax machines, while the RFX96V12 and RFX144V12 add integrated fax/digital answering machine functionality by providing a 5.7 kbps voice codec that yields 12 minutes of voice storage per 4-Mbits of memory.

To reduce OEM time to market, a royalty free license is available for the use of Rockwell's fax machine example/application program. This code can be used by the OEM as a basis for developing a customer's specific fax machine application, and requires modifications to achieve production worthiness.

FEATURES

- Facsimile processing firmware provides:
  - A real-time multitasking environment
  - Modular software design
  - T.30 protocol and call progress support
  - T.4/T.6 MH/MR/MMR control
  - Fax copy, transmit, and receive capabilities
  - Page memory features
  - Digital Answering Machine features
- Group 3 facsimile transmission/reception
  - CCITT V.29, V.27 ter, V.21 channel 2, T.4, T.30
  - CCITT V.33 and V.17 (R144EFXL, RFX144V12)
  - HDLC framing at all speeds
- Digital Answering Machine support
  - 5.7 kbps voice codec (RFX96V12, RFX144V12)
  - ARAM support
- Internal MC24 CPU (65C02 based)
  - 24-bit address, 10 MHz clock speed
  - Programmable wait states for external devices
- Compression/decompression in hardware
  - MH/MR standard
  - MMR (IFC-MVM)
  - Alternate compression/decompression (IFC-MVM)
- DRAM controller
- Real time clock
- Programmable thermal printer interface
  - Print widths to 4096 pixels
  - On-chip thermal head temperature A/D converter
  - Supports TPH printers including latchless 2-split printing mode
  - 5 ms minimum print line time

(Continued)

Table 1. Advanced FAXENGINE Family Overview

Advanced FAXENGINE Family			Application				
Advanced FAXENGINE Model	Facsimile Modem	Integrated Fax Controller	V.29	Page Memory	V.17	Digital Answering Machine	T.6 MMR
R96FEM	R96DFXL	IFC-MV	yes	yes			
R144FEM	R144EFXL	IFC-MV	yes	yes	yes		
R96FEMV	RFX96V12	IFC-MV	yes	yes		yes	
R144FEMV	RFX144V12	IFC-MV	yes	yes	yes	yes	
R96FEM-MMR	R96DFXL	IFC-MVM	yes	yes			yes
R144FEM-MMR	R144EFXL	IFC-MVM	yes	yes	yes		yes
R96FEMV-MMR	RFX96V12	IFC-MVM	yes	yes		yes	yes
R144FEMV-MMR	RFX144V12	IFC-MVM	yes	yes	yes	yes	yes

Data Sheet
(Preliminary)

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FEATURES (Continued)

- Programmable scanner interface
  - —Supports CIS and CCD Scanners
  - —Scan widths to 2048 pixels
  - —5 ms minimum scan line time
- Rockwell's Proprietary Image Corrections System (RPICS)
  - —On-chip 6-bit flash A/D
  - —2 scanner shading correction modes
  - —Dynamic contrast control
  - —Edge enhancement
  - —Configurable dither table (8 x 8 x 8-bit programmable pattern)
  - —2 dimensional B4 to A4 reduction
- Programmable control for two independent stepper motors or single motor operation
- Programmable operator panel interface
  - —Directly supports 32 keys, 8 LEDs, and one LCD
  - —Extendable with external circuitry
- General Purpose Input/Output (GPIO) pins with programmable direction control
- Packages: Modem in 100-pin Plastic Quad Flat Pack (PQFP) and IFC in 144-pin Thin Quad Flat Pack (TQFP)

FAXENGINE Development System

A FAXENGINE development system, which can be purchased to reduce OEM design costs and time to market, includes:

1. The FAXENGINE Evaluation System (FEES-MV): a stand-alone development board that acts as the fax machine motherboard. The FEES-MV includes an IFC socket, ROM and RAM, keyboard/LED/LCD modules, speaker, phone jack, microphone, printer and scanner and motor interfaces, and data access arrangement (DAA) circuitry. Video processing and modem daughter boards are also included.

2. A FAXENGINE ROM Emulator (MC24FERE) is a computer- based code development aid with breakpoint and trace capability for debugging customer created firmware that will operate in the FAXENGINE external ROM.

HARDWARE DESCRIPTION

The Advanced FAXENGINE Family general hardware interface is illustrated in Figure 1, and functional hardware interface signals are shown in Figure 2.

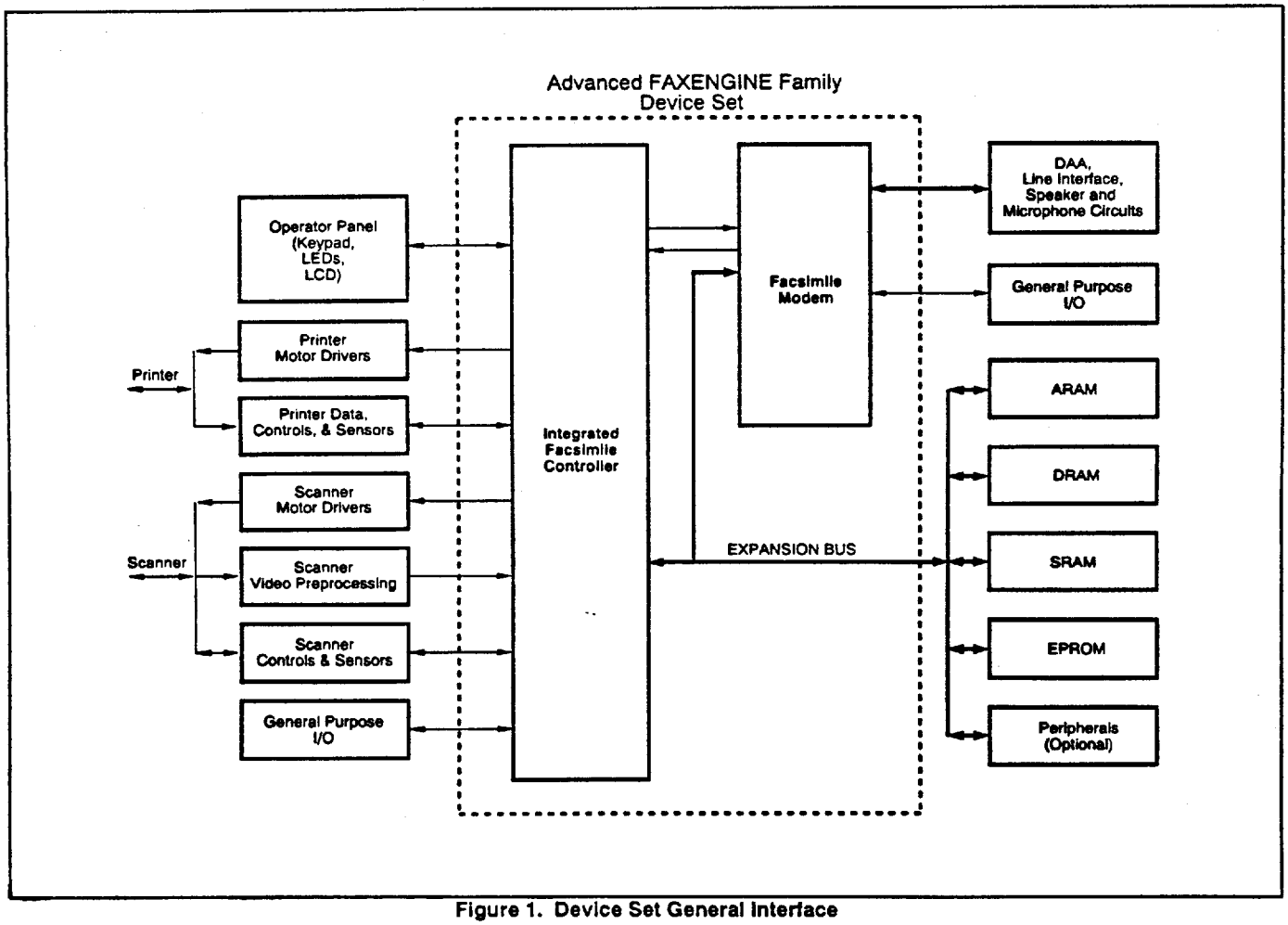


Figure 1. Device Set General Interface

INTEGRATED FACSIMILE CONTROLLER (IFC)

The Integrated Facsimile Controllers are the IFC-MV and the IFC-MVM.

Each IFC contains an internal 8-bit microprocessor and dedicated circuitry optimized for facsimile image processing and machine control and monitoring.

Microprocessor. The microprocessor is an enhanced MC24 central processing unit (CPU). This CPU provides fast instruction (10 MHz clock speed) execution and memory efficient input/output bit manipulation. The CPU connects to other internal IFC functions over a 24-bit address/8-bit data bus and dedicated control lines. The bus is routed outside the IFC for external memory access.

Scanner, Printer Motor Control. Eight outputs are provided to external current drivers; four for the scanner motor and four for the printer motor.

The printer and scanner motor outputs can be programmed as general purpose outputs (GPO) for application with a single motor.

Independent scan and print line times are supported.

Thermal Printer Control. The thermal printer interface consists of programmable data, latch, clock, and up to 4 strobe signals. Programmable timing supports traditional thermal printers, as well as the newer latchless split mode printers, and line lengths up to 4096 pixels. The IFC also includes an internal TPH temperature A/D converter.

Expansion Bus Control. Address, data, control, status, interrupt, and decoded chip select signals support connection to external ROM, external RAM (ARAM, DRAM, and SRAM), and optional peripheral devices. Dedicated internal DMA logic is included for scanner, T.4, and printer access of internal and/or external RAM.

Operator Interface. Four keyboard inputs, eight strobe outputs, and two control outputs support the operator interface.

A 32-key keypad can be supported directly, and an 8 x n keyboard can be supported with minimal external circuitry, where $n \leq 15$.

Up to eight LEDs and one LCD module can be directly driven.

Scanner and Video Control. Six programmable control and timing signals support common CCD and CIS scanners. The video control function provides signals for controlling the scanner and for processing its video output.

Scanner Flash A/D Interface. An internal 6-bit flash A/D converter is provided.

T.4/T.6 Compressor/Decompressor. Each IFC provides MH and MR data compression and decompression per CCITT Recommendation T.4.

The IFC-MVM adds MMR data compression and decompression per CCITT Recommendation T.6 in dedicated hardware. Compression and decompression can be alternated on a line-by-line basis.

Video Processing. Each IFC performs shading correction to correct scanner data for non-uniformities in the scanner sensor and light source. Less than 1k-byte of RAM is required to support pixel-by-pixel or one per 8 pixels shading correction.

Edge enhancement and dynamic contrast control (Auto background control, contrast control, MTF) are also performed.

The IFCs includes an 8 x 8 dither table, which is programmable and stored in internal RAM (8 bits per table entry).

The IFCs also include an image data processing port to allow the customer to access scan data prior to video processing in order to perform proprietary processing.

External ROM. External ROM stores all the FAXENGINE program object code.

Internal RAM. 1k-byte of internal RAM is available to support shading correction, line buffers, or the CPU.

External RAM. External RAM is used by the FAXENGINE embedded CPU. It can also be used for shading RAM and line buffer RAM. Five internal DMA channels support scanner, printer, and T.4 access of the external shading and line buffer RAM. A sixth DMA channel is available to support T.4/T.6 access to external page memory.

External DRAM Support. One of four external DRAM configurations is used to support page and/or voice memory, and the IFC includes a DRAM controller. The DRAM controller supports refresh during battery operation.

For a more cost effective approach, ARAM can be used instead of DRAM for voice storage.

Real Time Clock (RTC). The IFCs include a battery backed-up real time clock. The life of the RTC is 32 years, and leap year compensation is included.

FACSIMILE MODEM

The synchronous half-duplex facsimile modems are the R96DFXL, R144EFXL, RFX96V12, and the RFX144V12.

All the facsimile modems support Group 3 fax, HDLC framing, tone generation and detection, and DTMF reception. The modems can operate over the public switched telephone network (PSTN) or the general switched telephone network (GSTN) through line terminations provided by a data access arrangement (DAA). The modems all satisfy the requirements specified by CCITT recommendations V.29, V.27 ter, V.21 Channel 2, and T.4, meet the binary signaling requirements of T.30, operate at 9600, 7200, 4800, 2400, or 300 bps, and include the V.27 short training sequence option.

The R144EFXL and RFX144V12 also satisfy CCITT recommendations V.33 and V.17 providing the additional data rates of 14400 and 12000 bps, and include the V.29 short training sequence option.

A 5.7 kbps voice codec is integrated with the facsimile modem in the RFX96V12 and RFX144V12, allowing for the storage of 12 minutes of voice in one 4-Mbits memory.

HARDWARE INTERFACE DESCRIPTION

Scanner Interface

Scanner Control

Four output signals: START, CLK1, CLK2, /CLK1
Scan line period: 5 to 40 ms
Control signal rising and falling edges are independently programmable
Scanner light source control (with GPIO)

Scan Data Transfer Control

Scan start delay: 0 to 2047 dots
Line length: 8 to 2048 dots, modulo 8

Video Circuitry Control

Two output signals: VIDCTL0, VIDCTL1
VIDCTL0 rising and falling edges: Independently programmable within each dot period
VIDCTL1 rising and falling edges: Independently programmable within a scan line period

Video A/D Interface

Internal 6-bit flash (FADC)
ADC clock provided by IFC
Programmable ADC sample position
External VREF+ and VREF- inputs

Image data processing port

11 data and control signals multiplexed with GPIO
VID0-VID7 = parallel output port for multi-level FADC data or shading corrected data, or reduced shading corrected data
VDC0-VID1 = control signals for synchronization with video port data
VDC2 = bi-level data input for externally processed image data

Video Processing

Dither table: 8 x 8 x 8-bit programmable pattern
Automatic shading correction: Up to 50% ADC range, pixel-by-pixel, or 1 per 8 pixels
Dynamic background control
Automatic contrast and brightness control
Multi-level/bi-level B4-to-A4 reduction (2-dimensional)
Edge enhancement
Half-toning
Normal mode OR-ing

Printer Interface

Print Data Interface

Three output signals: PDAT, PCLK, PLAT
Polarity control: Independently programmable for all three outputs
Line period: 5 to 40 ms
Number of dots: 8 to 4096 dots, modulo 8
Printer data clock: 2 to 128 TSTCLKs

Strobe Generation

Strobe count: 0 to 4 strobes
Polarity control: Strappable
Programmable Printer data clock and strobe clock
- Strobe clock = 1 to 32 Printer data clocks

Strobe period: 1 to 256 strobe clocks
Strobe off time adjustable to 1 to 256 strobe clocks
Non-overlapping strobes

Temperature A/D Conversion

Implemented with comparator, DAC, and auto-convert counter: Selectable internal filter
Resolution: 6 bits
Accuracy: 1/2 LSB
Output update rate < 80 ms

External Bus Interface

Chip Selects

/ROMCS is the ROM chip select
/MCS is the modem chip select
/CS0 and /CS1 are two general chip selects
/CS2-/CS5 are four additional chip selects multiplexed with GPIO12-GPIO15, respectively

RAM Interface

Wait states for RAM chip select: 0 to 3
Programmable RAM size:
(8k-byte, 32k-byte, 64k-byte, 1M-byte
RAM access time: 70 ns with 0 wait states (at 7 MHz)

DRAM Interface

3 DRAM chip selects /CAS0-/CAS2, with common /RAS and write signal, /DWR
Three DRAM blocks
- Size of each block is programmable (256k-byte, 512k-byte, 1M-byte, and 4M-byte), as is access speed (60 to 150 ns, 0 or 1 wait state)

CAS-before RAS refresh with programmable rate (128 ms, 16 ms, or 8 ms per 1024 cycles)
Refresh during battery operation is supported

External ROM Interface

Wait states for ROM chip select: 0 to 3
ROM access time: 70 ns with 0 wait states (at 7 MHz)

External I/O Interface

Wait states for I/O chip select: 0 to 7

External Interrupts

1-4 external interrupt signals are available
/MIRQ is a dedicated modem interrupt
3 external interrupts are multiplexed with GPIO signals:
/IRQ5 and /IRQ1 are active low interrupts multiplexed with GPIO17 and GPIO18
IRQ8 is an active high interrupt multiplexed with GPIO16

Power-On Reset (BATRESN) Input

/BATRES input initializes the FAXENGINE at power on. /PWRDWN input controls switching between primary and battery power.

Reset (/RESET) Input/Output

Open drain input/output: Can accept external reset input or provide reset output to external circuit. External RESET will not reset the RTC or stop DRAM refresh.

Watchdog Timer

IFC watchdog timer serviced by the IFC.

Programmable watchdog enable.

Programmable time-out period before reset.

Tone Generator

Single tone output.

Programmable frequency: 20 to 4000 Hz

General Purpose I/O (GPIO)

IFCs	R96DFXL	R144EFXL	RFX96V12	RFX144V12
20 GPIO	8 GPIO	8 GPIO		
	5 GPI	5 GPI	8 GPI	8 GPI
8 GPO			8 GPO	8 GPO

Programmable direction control is provided for all IFC GPIO signals.

System Timing

Timing source: External oscillator or modem clock.

Two internal timer interrupts: 1 ms and MSINT time, where MSINT = the programmable Mechanical Subsystem Timer.

RTC Interface

32-year RTC with leap year compensation.

Included crystal oscillator uses 32.768 or 65.536 kHz crystal. (Fast DRAM refresh during battery operation requires higher frequency crystal.)

ENVIRONMENTAL AND POWER REQUIREMENTS

Advanced FAXENGINE family environmental specifications are shown in Table 2, with power requirements are given in Table 3.

IFC INTERFACE SIGNALS

The IFC hardware signal pin assignments are shown in Figure 3 with definitions summarized in Table 4, and the hardware signal characteristics described in Table 5.

FACSIMILE MODEM INTERFACE SIGNALS

R96DFXL and R144EFXL pin assignments are shown in Figure 4, and listed by pin number in Table 6. R96DFXL and R144EFXL hardware interface signals are listed by functional group in Table 7.

RFX96V12 and RFX144V12 pin assignments are shown in Figure 5, and listed by pin number in Table 8. RFX96V12 and RFX144V12 hardware interface signals are listed by functional group in Table 9.

The modem digital interface characteristics are listed in Table 10, and the analog interface characteristics in Table 11.

REFERENCE DOCUMENTATION

Document	Order No.
R96DFXL MONOFAX Modem Data Sheet	MD92
R144EFXL MONOFAX Modem Data Sheet	MD90
RFX96/144V12 MONOFAX Modem Data Sheet	MD107
MC24 Megacell CPU Programmer's Guide	415
9600 bps MONOFAX Modem Designer's Guide	820
9600 bps MONOFAX Modem Designer's Guide Addendum for R96DFXL	820A
R144EFXL MONOFAX Modem Designer's Guide	895
RFX96V12 and RFX14V12 MONOFAX Modem Designer's Guide	1011
Advanced FAXENGINE Family Integrated Facsimile Controller (IFC) Hardware Description	1013
Advanced FAXENGINE Evaluation System (FEES-MV) User's Manual	1014
Advanced FAXENGINE Firmware Description	1015
MC24 FAXENGINE ROM Emulator System (MC24 FERE) User's Manual	1016
Low Bit Rate Voice (LBRV) MEB User's Manual	1023

Table 2. Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32°F to 158°F)
Storage	–40°C to 80°C (–40°F to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Table 3. Power Requirements

Device	Voltage[1]	Typical Current @ 25°C	Maximum Current
IFC with Primary Power			
	+5 VDC +5%/-10%	65 mA	80 mA
IFC with Battery Power[2]			
IFC RTC[3]	+5 VDC	250 µA	500 µA
	+3 VDC	20 µA	50 µA
IFC DRAM	+5 VDC	250 µA	400 µA
Refresh	+3 VDC	150 µA	250 µA
MONOFAX Modems			
R96DFXL	+5 VDC ±5%	50 mA	55 mA
R144EFXL	+5 VDC ±5%	54 mA	60 mA
RFX96V12	+5 VDC ±5%	100 mA	119 mA
RFX144V12	+5 VDC ±5%	100 mA	119 mA

Notes:
1. Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 and 150 kHz must be less than 500 microvolts peak.
2. Battery power measurements made with a 32.768 kHz crystal oscillator frequency and a normal refresh rate.
3. RTC = Real Time Clock.

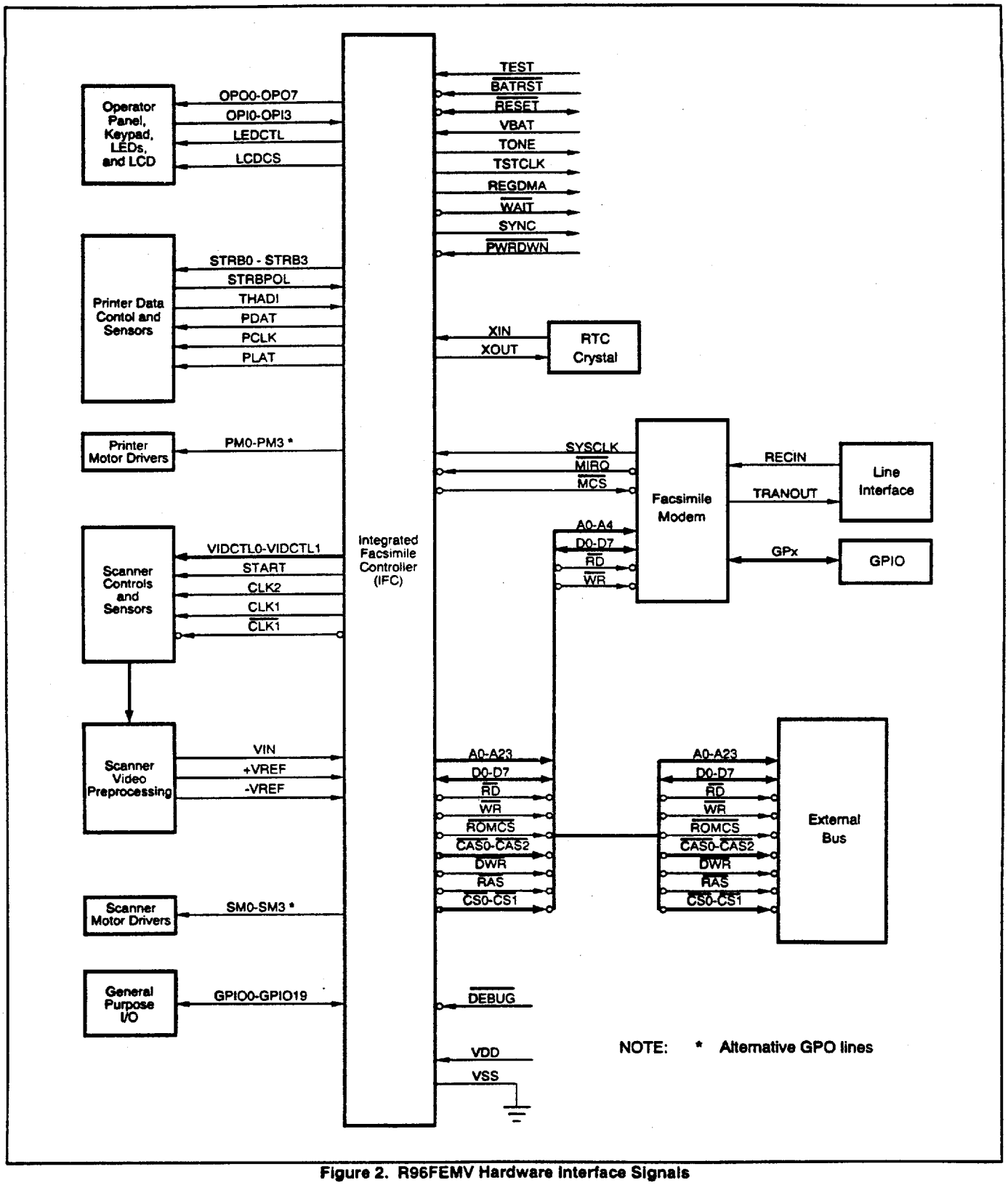


Figure 2. R96FEMV Hardware Interface Signals

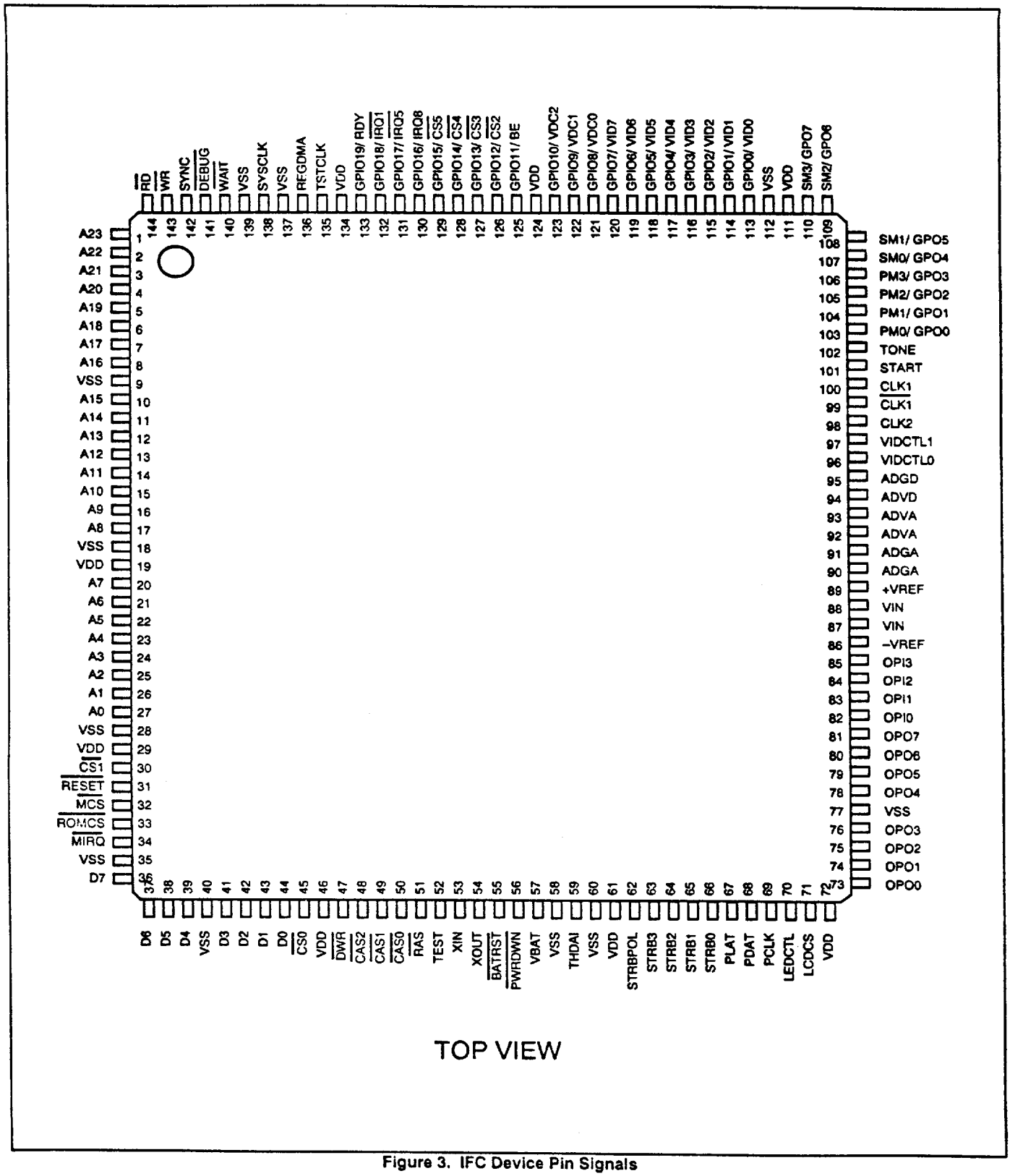


Figure 3. IFC Device Pin Signals

Table 4. IFC Pin Functions

Pin No.	Name	I/O	Description	Comments	Input Type	Output Type
System Bus Control IF						
1	A23	I/O	System Bus Address 23		T	3XT
2	A22	I/O	System Bus Address 22		T	3XT
3	A21	I/O	System Bus Address 21		T	3XT
4	A20	I/O	System Bus Address 20		T	3XT
5	A19	I/O	System Bus Address 19		T	3XT
6	A18	I/O	System Bus Address 18		T	3XT
7	A17	I/O	System Bus Address 17		T	3XT
8	A16	I/O	System Bus Address 16		T	3XT
9	VSS		Digital Ground			
10	A15	I/O	System Bus Address 15		T	3XT
11	A14	I/O	System Bus Address 14		T	3XT
12	A13	I/O	System Bus Address 13		T	3XT
13	A12	I/O	System Bus Address 12		T	3XT
14	A11	I/O	System Bus Address 11		T	3XT
15	A10	I/O	System Bus Address 10		T	3XT
16	A9	I/O	System Bus Address 9		T	3XT
17	A8	I/O	System Bus Address 8		T	3XT
18	VSS		Digital Ground			
19	VDD		Digital Power			
20	A7	I/O	System Bus Address 7		T	3XT
21	A6	I/O	System Bus Address 6		T	3XT
22	A5	I/O	System Bus Address 5		T	3XT
23	A4	I/O	System Bus Address 4		T	3XT
24	A3	I/O	System Bus Address 3		T	3XT
25	A2	I/O	System Bus Address 2		T	3XT
26	A1	I/O	System Bus Address 1		T	3XT
27	A0	I/O	System Bus Address 0		T	3XT
28	VSS		Digital Ground			
29	VDD		Digital Power			
30	CS1	O	I/O chip select		–	2XT
Prime Power Reset Logic and Test						
31	RESET	I/O	Reset FEMV	Internal Pullup, Open Drain Hysteresis In	HU	2XO
System Bus Control IF (Continued)						
32	MCS	O	Modem chip select		–	2XC
33	ROMCS	O	ROM chip select		–	2XT
CPU Control IF						
34	MIRQ	I	Modem interrupt	Hysteresis In, Internal Pullup	HU	–
System Bus Control IF (Continued)						
35	VSS		Digital Ground			
36	D7	I/O	System Data bus 7		T	3XT
37	D6	I/O	System Data bus 6		T	3XT
38	D5	I/O	System Data bus 5		T	3XT
39	D4	I/O	System Data bus 4		T	3XT
40	VSS		Digital Ground			
41	D3	I/O	System Data bus 3		T	3XT
42	D2	I/O	System Data bus 2		T	3XT
43	D1	I/O	System Data bus 1		T	3XT
44	D0	I/O	System Data bus 0		T	3XT
45	CS0	O	SRAM chip select		–	2XT
46	VDD		Digital Power			
47	DWR	O	DRAM Write Strobe		–	3XT
48	CAS2	O	DRAM Column Address Strobe 2		–	2XT
49	CAS1	O	DRAM Column Address Strobe 1		–	2XT
50	CAS0	O	DRAM Column Address Strobe 0		–	2XT
51	RAS	O	DRAM Row Address Strobe		–	3XT

Table 4. IFC Pin Functions (Cont'd)

Pin No.	Name	I/O	Description	Comments	Input Type	Output Type
Prime Power Reset Logic and Test (Continued)						
52	TEST	I	Test mode pin (low for normal operation)		C	–
Battery Power Control and Reset Logic						
53	XIN	I	RTC and DRAM refresh crystal input		OSC3	–
54	XOUT	O	RTC and DRAM refresh crystal output		–	OSC3
55	BATRST	I	Battery power reset input	Hysteresis In	H	–
56	PWRDWN	I	Indicates loss of prime power	Hysteresis In	H	–
57	VBAT		Battery Power			
58	VSS		Digital Ground			
Special Signals						
59	THADI	I	Analog Thermal A/D input		TA	–
Printer IF						
60	VSS		Digital Ground			
61	VDD		Digital Power			
62	STRBPOL	I	Controls active high or low status of strobes		C	–
63	STRB3	O	Strobe signal 3 for the Thermal Print Head (TPH)		–	1XP
64	STRB2	O	Strobe signal 2 for the TPH		–	1XP
65	STRB1	O	Strobe signal 1 for the TPH		–	1XP
66	STRB0	O	Strobe signal 0 for the TPH		–	1XP
67	PLAT	O	Latch signal for the TPH		–	3XP
68	PDAT	O	Serial printing data for the TPH		–	2XP
69	PCLK	O	TPH clock		–	3XC
Operator Panel IF						
70	LEDCTL	O	LED (OPO7-OPO0 output) control		–	5XC
71	LCDCS	O	LCD chip select		–	1XC
72	VDD		Digital Power			
73	OPO0	O	Keyboard / LED strobe 0		–	2XL
74	OPO1	O	Keyboard / LED strobe 1		–	2XL
75	OPO2	O	Keyboard / LED strobe 2		–	2XL
76	OPO3	O	Keyboard / LED strobe 3		–	2XL
77	VSS		Digital Ground			
78	OPO4	O	Keyboard / LED strobe 4		–	2XL
79	OPO5	O	Keyboard / LED strobe 5		–	2XL
80	OPO6	O	Keyboard / LED strobe 6		–	2XL
81	OPO7	O	Keyboard / LED strobe 7		–	2XL
82	OPI0	I	Keyboard return 0	Pullup, Hysteresis In	HU	–
83	OPI1	I	Keyboard return 1	Pullup, Hysteresis In	HU	–
84	OPI2	I	Keyboard return 2	Pullup, Hysteresis In	HU	–
85	OPI3	I	Keyboard return 3	Pullup, Hysteresis In	HU	–
Special Signals (Continued)						
86	-VREF	I	Negative Reference Voltage for Video A/D		-VR	–
87	VIN	I	Analog Video A/D input		VA	–
88	VIN	I	Analog Video A/D input		VA	–
89	+VREF	I	Positive Reference Voltage for Video A/D		+VR	–
90	ADGA		A/D Analog Ground		VADG	
91	ADGA		A/D Analog Ground		VADG	
92	ADVA		A/D Analog Power		VADV	
93	ADVA		A/D Analog Power		VADV	
94	ADVD		A/D Digital Power		VADV	
95	ADGD		A/D Digital Ground		VADG	
Scan IF						
96	VIDCTL0	O	Scanner signal preprocessing circuit control signal 0		–	2XC
97	VIDCTL1	O	Scanner signal preprocessing circuit control signal 1		–	2XC
98	CLK2	O	Scanner reset gate control, or CIS scanner clock		–	2XS
99	CLK1	O	Scanner inverted clock		–	2XS
100	CLK1	O	Scanner clock		–	2XS
101	START	O	Controls scanner shift gate		–	2XS

Table 4. IFC Pin Functions (Cont'd)

Pin No.	Name	I/O	Description	Comments	Input Type	Output Type
General Purpose I/O						
102	TONE	O	Single tone signal output		–	1XC
103	PM0/GPO0	O	Print motor cntl or GPO (programmable)		–	1XC
104	PM1/GPO1	O	Print motor cntl or GPO (programmable)		–	1XC
105	PM2/GPO2	O	Print motor cntl or GPO (programmable)		–	1XC
106	PM3/GPO3	O	Print motor cntl or GPO (programmable)		–	1XC
107	SM0/GPO4	O	Scan motor cntl or GPO (programmable)		–	1XC
108	SM1/GPO5	O	Scan motor cntl or GPO (programmable)		–	1XC
109	SM2/GPO6	O	Scan motor cntl or GPO (programmable)		–	1XC
110	SM3/GPO7	O	Scan motor cntl or GPO (programmable)		–	1XC
111	VDD		Digital Power			
112	VSS		Digital Ground			
113	GPIO0/ VID0	I/O	GPIO0 or video data 0 (programmable)	Hysteresis In	H	2XC
114	GPIO1/ VID1	I/O	GPIO1 or video data 1 (programmable)	Hysteresis In	H	2XC
115	GPIO2/ VID2	I/O	GPIO2 or video data 2 (programmable)	Hysteresis In	H	2XC
116	GPIO3/ VID3	I/O	GPIO3 or video data 3 (programmable)	Hysteresis In	H	2XC
117	GPIO4/ VID4	I/O	GPIO4 or video data 4 (programmable)	Hysteresis In	H	2XC
118	GPIO5/ VID5	I/O	GPIO5 or video data 5 (programmable)	Hysteresis In	H	2XC
119	GPIO6/ VID6	I/O	GPIO6 or video data 6 (programmable)	Hysteresis In	H	2XC
120	GPIO7/ VID7	I/O	GPIO7 or video data 7 (programmable)	Hysteresis In	H	2XC
121	GPIO8/ VDC0	I/O	GPIO8/ video data cntl 0 (programmable)	Hysteresis In	H	2XC
122	GPIO9/ VDC1	I/O	GPIO9/ video data cntl 1 (programmable)	Hysteresis In	H	2XC
123	GPIO10/ VDC2	I/O	GPIO10/ video data cntl 2 (programmable)	Hysteresis In	H	2XC
124	VDD		Digital Power			
125	GPIO11/$\overline{BE}$	I/O	GPIO11/ bus enable (programmable)	Hysteresis In	H	1XC
126	GPIO12/ $\overline{CS2}$	I/O	GPIO12/ I/O chip select 2 (programmable)	Hysteresis In	H	2XC
127	GPIO13/ $\overline{CS3}$	I/O	GPIO13/ I/O chip select 3 (programmable)	Hysteresis In	H	2XC
128	GPIO14/ $\overline{CS4}$	I/O	GPIO14/ I/O chip select 4 (programmable)	Hysteresis In	H	2XC
129	GPIO15/ $\overline{CS5}$	I/O	GPIO15/ I/O chip select 5 (programmable)	Hysteresis In	H	2XC
130	GPIO16/$\overline{IRQ8}$	I/O	GPIO16 or IRQ 8 input (active high)	Hysteresis In	H	1XC
131	GPIO17/ $\overline{IRQ5}$	I/O	GPIO17 or IRQ 5 input (active low)	Hysteresis In	H	1XC
132	GPIO18/ $\overline{IRQ1}$	I/O	GPIO18 or IRQ 1 input (active low)	Hysteresis In	H	1XC
133	GPIO19/RDY	I/O	GPIO19 or ready signal (programmable)	Hysteresis In	H	1XC
134	VDD		Digital Power			
CPU Control IF (Continued)						
135	TSTCLK	O	Test clock		–	3XC
System Bus Control IF (Continued)						
136	REGDMA	O	REGSEL cycle and DMA cycle		–	3XC
137	VSS		Digital Ground			
CPU Control IF (Continued)						
138	SYSCLK	I	System clock	Hysteresis In	H	–
139	VSS		Digital Ground			
System Bus Control IF (Continued)						
140	WAIT	O	Indicates TSTCLK cycle wait state		–	3XC
Prime Power Reset Logic and Test (Continued)						
141	DEBUG	I	External NMI input	Hysteresis In, Internal Pullup	HU	–
System Bus Control IF (Continued)						
142	$\overline{SYNC}$	O	Indicates CPU op code fetch cycle		–	2XC
143	$\overline{WR}$	O	Write strobe		–	3XT
144	$\overline{RD}$	O	Read strobe		–	3XT

Notes:
1. Name: Identifies the pin's active polarity:
   With overscore = Active low
   Without overscore =Active high or programmable polarity
2. I/O: Depicts the pin's input/output capability:
   I = Input only
   O = Output only
   I/O = Both Input and output

Table 5. IFC Hardware Signal Characteristics

Input Signal Characteristics

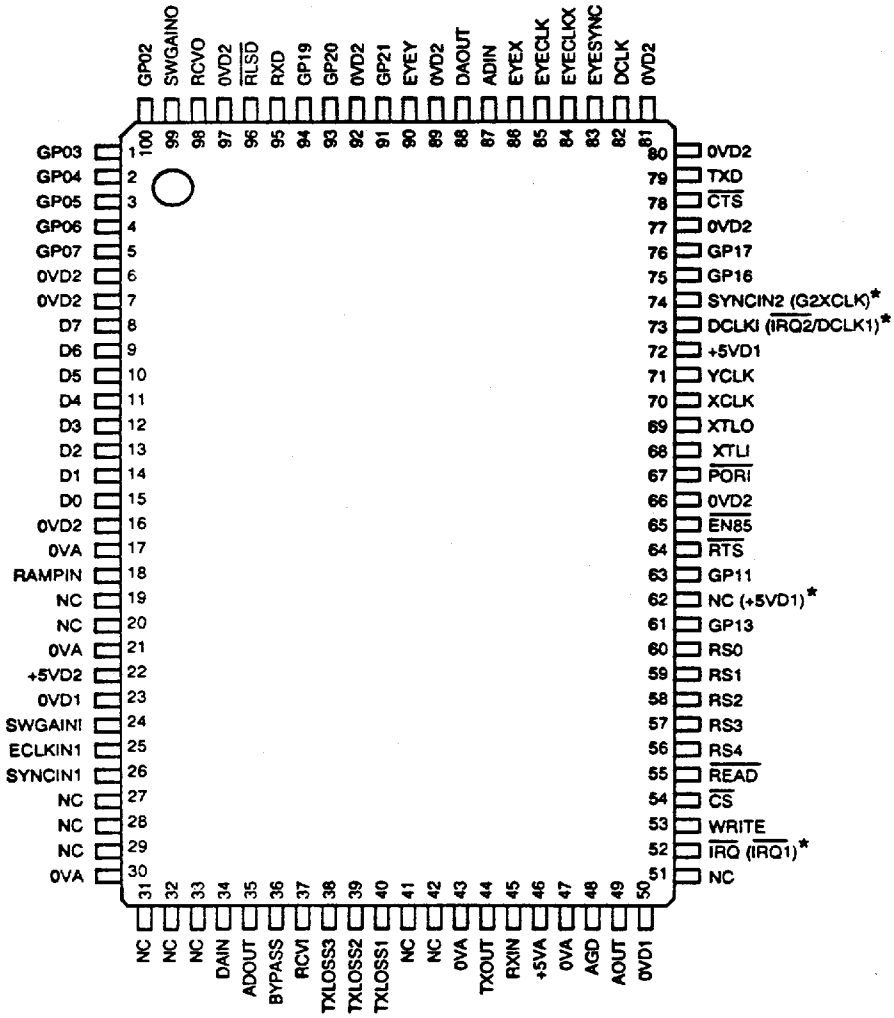
Input Type	Description	VIL (V max)	VIH (V min)	Hysterisis (V min)	Pullup Resistance (K ohm)
C	CMOS Input	0.3*VDD	0.7*VDD	–	–
CU	CMOS/Pullup	0.3*VDD	0.7*VDD	–	35–150
H	Hysteresis	0.25*VDD	0.7*VDD	0.9	–
HU	Hysteresis/Pullup	0.25*VDD	0.7*VDD	0.9	35–150
T	TTL Input	0.8	2.0	–	–
TU	TTL/Pullup	0.8	2.0	–	35–150
OSC3	CMOS Input	0.3*VDD	0.7*VDD	–	–

Absolute Input Range = –0.5 to VDD+0.5

Input Type	Description	Operating (V min)	Operating (V max)	Absolute Max (V min)	Absolute Max (V max)
TA	Thermal Head Analog Input	0.2*VDD	0.8*VDD	–0.5	VDD+0.5
VA	Video Analog In	-VR	+VR	-0.5	ADVA + 0.5
+VR	Video A/D +Vref	0.8	3.3	-0.5	ADVA + 0.5
-VR	Video A/D -Vref	-0.2	2.0	-0.5	ADVA + 0.5
VADV	Video A/D Power	VDD-0.1	VDD + 0.1	–	7.0
VADG	Video A/D GND	-0.1	0.1	-0.5	0.5
VDD	Digital Power	4.5	5.25	–0.25	7.0
GND	Digital Ground	0	0	0	0
VBAT	Battery Power	2.70	5.25	–0.25	7.0

Output Signal Characteristics

Output Type	Description	VOL (V max)	IOL (mA max)	VOH (V min)	IOH (mA max)	CL (pF max)
1XC	CMOS Output (1x)	0.4	1.6	VDD–1.5	1.6	50
1XP, 2XP	High Capacitance Driver	0.4	1.6	VDD–1.5	1.6	200
2XC	CMOS Output (2x)	0.4	3.5	VDD–1.5	3.5	50
2XT	TTL Output (2x)	0.4	4	2.4	4	50
2XS	CMOS Output (2x)	0.4	3.5	VDD–1.5	3.5	50
				1.5	15	50
2XL	LED Driver	0.7	10	VDD–1.5	3.5	100
2XO	CMOS Output, Open Drain	0.4	3.5	N/A	N/A	50
3XC	CMOS Output (3x)	0.4	6	VDD–1.5	6	50
3XP	High Capacitance Driver (3x)	0.4	6	VDD–1.5	6	700
3XT	TTL Output (3x)	0.4	6	2.4	6	50
5XC	CMOS Output (5x)	0.4	12	VDD–1.0	12	50
OSC3	Oscillator CMOS Output	–	–	–	–	–



TOP VIEW

Note: * Indicates a signal name in parentheses for the R144EFXL that differs from the signal name for that pin on the R96DFXL. All pins without this note are identically named.

Figure 4. R96DFXL/R144EFXL Facsimile Modem Pin Signals

Table 6. R96DFXL/R144EFXL Fax Modem Pin Signals

Pin No.	Signal Name	I/O Type
1	GP03	IA/OB
2	GP04	IA/OB
3	GP05	IA/OB
4	GP06	IA/OB
5	GP07	IA/OB
6	0VD2	GND
7	0VD2	GND
8	D7	IA/OB
9	D6	IA/OB
10	D5	IA/OB
11	D4	IA/OB
12	D3	IA/OB
13	D2	IA/OB
14	D1	IA/OB
15	D0	IA/OB
16	0VD2	GND
17	0VA	GND
18	RAMPIN	R
19	NC	
20	NC	
21	0VA	GND
22	+5VD2	PWR
23	0VD1	GND
24	SWGAINI	R
25	ECLKIN1	R
26	SYNCIN1	R
27	NC	
28	NC	
29	NC	
30	0VA	GND
31	NC	
32	NC	
33	NC	
34	DAIN	R
35	ADOUT	R
36	BYPASS	IC
37	RCVI	R
38	TXLOSS3	IC
39	TXLOSS2	IC
40	TXLOSS1	IC
41	NC	
42	NC	
43	0VA	GND
44	TXOUT	AA
45	RXIN	AB
46	+5VA	PWR
47	0VA	GND
48	AGD	R
49	AOUT	R
50	0VD1	GND
51	NC	
52	IRQ (IRQ1)	OC (Note 4)
53	WRITE-R/W	IA
54	CS	IA
55	READ-ϕ2	IA

Table 6. R96DFXL/R144EFXL Fax Modem Pin Signals (Cont'd)

Pin No.	Signal Name	I/O Type
56	RS4	IA
57	RS3	IA
58	RS2	IA
59	RS1	IA
60	RS0	IA
61	GP13	IA/OB
62	NC (+5VD1)	(Note 4)
63	GP11	IA/OB
64	RTS	IA
65	EN85	R
66	0VD2	GND
67	PORI	ID
68	XTLI	R
69	XTLO	R
70	XCLK	OD
71	YCLK	OD
72	+5VD1	PWR
73	DCLKI	R
	(IRQ2/DCLK1)	(Note 4)
74	SYNCIN2	R
	(G2xCLK)	(Note 4)
75	GP16	IA/OB
76	GP17	IA/OB
77	0VD2	GND
78	CTS	OA
79	TXD	IA
80	0VD2	GND
81	0VD2	GND
82	DCLK	OA
83	EYESYNC	OA
84	EYECLKX	OA
85	EYECLK	OA
86	EYEX	OA
87	ADIN	R
88	DAOUT	R
89	0VD2	GND
90	EYEY	OA
91	GP21	IA/OB
92	0VD2	GND
93	GP20	IA/OB
94	GP19	IA/OB
95	RXD	OA
96	RLSD	OA
97	0VD2	GND
98	RCVO	R
99	SWGAINO	R
100	GP02	IA/OB

Notes:

1. NC = No connection; leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 10.
   Analog signals: see Table 11;
3. R = Required modem interconnection; no connection to host equipment.
4. The name in parentheses applies to the R144EFXL only.

Table 7. R96DFXL/R144EFXL Hardware Interface Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
PORI	ID	Power-On-Reset Input
+5VD1	PWR	Connect to Digital +5V Power
+5VD2	PWR	Connect to Digital +5V Power
+5VA	PWR	Connect to Analog +5V Power
0VD1	GND	Connect to Digital Ground
0VD2	GND	Connect to Digital Ground
0VA	GND	Connect to Analog 0V Ground
AGD	R	+2.5 V Analog Ground
Microprocessor Bus Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
$\overline{CS}$	IA	Chip Select
$\overline{READ}$-ϕ2	IA	Read Enable (808X), ϕ2 Clock (65XX)
$\overline{WRITE}$-R/$\overline{W}$	IA	Write Enable (808X), R/$\overline{W}$ (65XX)
$\overline{IRQ}$, $\overline{IRQ1}$, $\overline{IRQ2}$	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
RXD	OA	Received Data
$\overline{RTS}$	IA	Request to Send
$\overline{CTS}$	OA	Clear to Send
$\overline{RLSD}$	OA	Received Line Signal Detected
DCLK	OA	Transmit and Receive Data Clock
G2XCLK	IA	Group 2 External Transmit and Receive Data Clock
Auxiliary Signals		
BYPASS	IC	Receiver Highpass Filter Bypass Enable
TXLOSS1	IC	2 dB of Analog Transmit Level Attenuation
TXLOSS2	IC	4 dB of Analog Transmit Level Attenuation
TXLOSS3	IC	8 dB of Analog Transmit Level Attenuation
XCLK	OD	12 MHz/19 MHz Output
YCLK	OD	6 MHz/9.5 MHz Output
$\overline{EN85}$	IA	Enable 8085 Bus
GPx	IA/OB	General Purpose Input/Output

Table 7. R96DFXL/R144EFXL Hardware Interface Signals (Cntd)

Name	Type[1]	Description
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
Eye Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock (576 kHz)
EYESYNC	OA	Serial Eye Pattern Strobe (9600 Hz)
Modem Interconnect		
DCLKI	R	Connect to DCLK
ECLKIN1	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
SWGAINI	R	Connect to SWGAINO
SWGAINO	R	Connect to SWGAINI
RAMPIN	R	Receiver Amplifier Input
AOUT	R	Smoothing Filter Output

Notes:

1. Digital signals are described in Table 10. Analog signals are described in Table 11.
2. R = Required overhead connection; no connection to host equipment.

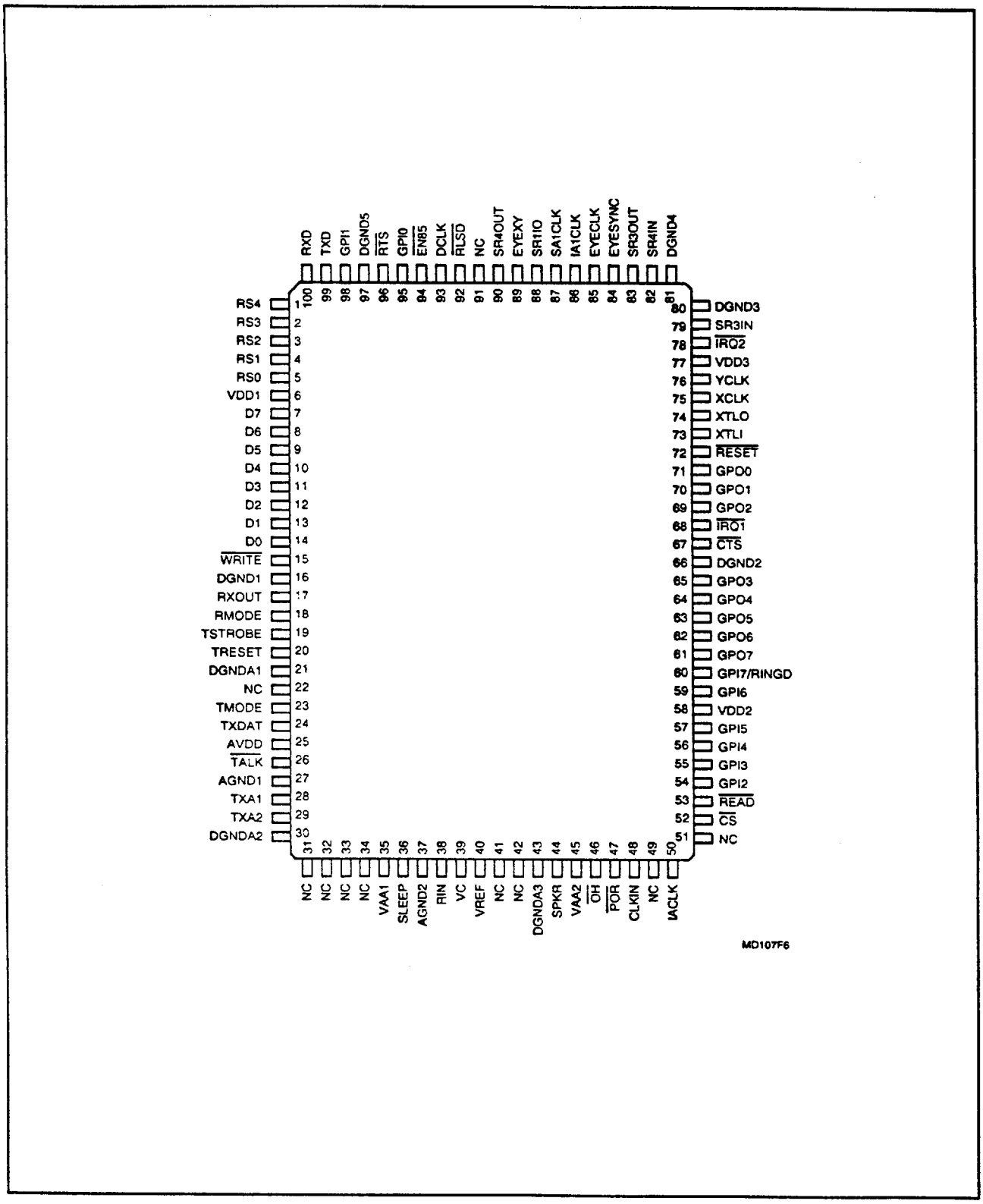


Figure 5. RFX96V12/RFX144V12 Pin Signals

Table 8. RFX96V12/RFX144V12 Fax Modem Pin Signals

Pin	Signal Label	Type	Interface
1	RS4	IA	Host Parallel Interface
2	RS3	IA	Host Parallel Interface
3	RS2	IA	Host Parallel Interface
4	RS1	IA	Host Parallel Interface
5	RS0	IA	Host Parallel Interface
6	VDD1	PWR	VCC
7	D7	IA/OB	Host Parallel Interface
8	D6	IA/OB	Host Parallel Interface
9	D5	IA/OB	Host Parallel Interface
10	D4	IA/OB	Host Parallel Interface
11	D3	IA/OB	Host Parallel Interface
12	D2	IA/OB	Host Parallel Interface
13	D1	IA/OB	Host Parallel Interface
14	D0	IA/OB	Host Parallel Interface
15	$\overline{\text{WRITE}}$	IA	Host Parallel Interface
16	DGND1	GND	DGND
17	RXOUT	MI	SR3IN (79)
18	RMODE	MI	TMODE (23)
19	TSTROBE	MI	IA1CLK (86)
20	TRESET	MI	SA1CLK (87)
21	DGNDA1	GND	AGND
22	NC		
23	TMODE	MI	RMODE (18)
24	TXDAT	MI	SR4OUT (90)
25	AVDD	PWR	VCC
26	$\overline{\text{TALK}}$	OD	Line Interface
27	AGND1	GND	AGND
28	TXA1	O(DD)	Analog Switch/Line Interface
29	TXA2	O(DD)	Analog Switch/Line Interface
30	DGNDA2	GND	AGND
31	NC		
32	NC		
33	NC		
34	NC		
35	VAA1	PWR	VCC
36	SLEEP	MI	Analog Sleep Control
37	AGND2	GND	AGND
38	RIN	I(DA)	Analog Switch/Line Interface
39	VC	MI	AGND through capacitors
40	VREF	MI	VC through capacitors
41	NC		
42	NC		
43	DGNDA3	GND	AGND
44	SPKR	O(DF)	Analog Switch/Speaker Circuit
45	VAA2	PWR	VCC
46	$\overline{\text{OH}}$	OD	Line Interface
47	$\overline{\text{POR}}$	MI	$\overline{\text{RESET}}$(72)
48	CLKIN	MI	IACLK (50)
49	NC		
50	IACLK	MI	CLKIN (48)
51	NC		
52	$\overline{\text{CS}}$	IA	Host Parallel Interface
53	$\overline{\text{READ}}$	IA	Host Parallel Interface

Table 8. RFX96V12/RFX144V12 Fax Modem Pin Signals (Cntd)

Pin	Signal Label	Type	Interface
54	GPI2	IA	General Purpose Input
55	GPI3	IA	General Purpose Input
56	GPI4	IA	General Purpose Input
57	GPI5	IA	General Purpose Input
58	VDD2	PWR	VCC
59	GPI6	IA	General Purpose Input
60	GPI7	IA	General Purpose Input[3]
61	GPO7	OB	General Purpose Output
62	GPO6	OB	General Purpose Output
63	GPO5	OB	General Purpose Output
64	GPO4	OB	General Purpose Output
65	GPO3	OB	General Purpose Output
66	DGND2	GND	DGND
67	$\overline{\text{CTS}}$	OA	DTE Serial Interface
68	$\overline{\text{IRQ1}}$	OC	Host Parallel Interface
69	GPO2	OB	General Purpose Output
70	GPO1	OB	General Purpose Output
71	GPO0	OB	General Purpose Output
72	$\overline{\text{RESET}}$	OA	Reset Circuit
73	XTLI	I	Crystal/Clock Circuit
74	XTLO	O	Crystal/Clock Circuit
75	XCLK	OD	Diagnostic Circuit
76	YCLK	OD	Diagnostic Circuit
77	VDD3	PWR	VCC
78	$\overline{\text{IRQ2}}$	OC	Host Parallel Interface
79	SR3IN	MI	RXOUT (17)
80	DGND3	GND	DGND
81	DGND4	GND	DGND
82	SR4IN	MI	NC (Reserved)
83	SR3OUT	MI	NC (Reserved)
84	EYESYNC	OA	Eye Pattern Circuit
85	EYECLK	OA	Eye Pattern Circuit
86	IA1CLK	MI	TSTROBE (19)
87	SA1CLK	MI	TRESET (20)
88	SR1IO	MI	TMODE (23) & RMODE (18)
89	EYEXY	OA	Eye Pattern Circuit
90	SR4OUT	MI	TXDAT (24)
91	NC		
92	$\overline{\text{RLSD}}$	OA	DTE Serial Interface
93	DCLK	OA	DTE Serial Interface
94	$\overline{\text{EN85}}$	IA	Auxiliary Circuit
95	GPI0	IA	General Purpose Input
96	$\overline{\text{RTS}}$	IA	DTE Serial Interface
97	DGND5	GND	DGND
98	GPI1	IA	General Purpose Input
99	TXD	IA	DTE Serial Interface
100	RXD	OA	DTE Serial Interface

Notes:
1. I/O types:
   MI = Modem interconnect.
   Digital input (IA, IB, etc.) and output (OA, OB, etc.).
   Analog input [I(DA)] and output [O(DD), O(DF), etc.].
2. NC = No external connection.
3. Normally connected to RINGD from DAA.

Table 9. RFX96V12/RFX144V12 Hardware I/F Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
RESET	ID	Reset Input
PORI	IA	Power-On-Reset Input
VDDn	PWR	Supply Voltage for DSP Circuits
AVDD	PWR	Supply Voltage for IA Analog Circuits
VAAn	PWR	Supply Voltage for IA Analog Circuits
DGNDn	GND	Ground for DSP Circuits
DGNDAn	GND	Ground for IA Digital Circuits
AGNDn	GND	Ground for IA Analog Circuits
Microprocessor Bus Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
CS	IA	Chip Select
READ-ϕ2	IA	Read Enable (808X), ϕ2 Clock (65XX)
WRITE-R/W	IA	Write Enable (808X), R/W (65XX)
IRQ, IRQ2	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
RXD	OA	Received Data
RTS	IA	Request to Send
CTS	OA	Clear to Send
RLSD	OA	Received Line Signal Detected
TDCLK	OA	Transmit Data Clock
RDCLK	IA	Receive Data Clock
Auxiliary Signals		
XCLK	OD	36.864 MHz Output
YCLK	OD	18.432 MHz Output
EN85	IA	Enable 8085 Bus
Diagnostic Indicator Interface		
INDOUTn	OA	Indicator Outputs

Table 9. RFX96V12/RFX144V12 Hardware I/F Signals (Cntd)

Name	Type[1]	Description
Line Interface		
RD	IA	Ring Frequency Detected Input
OH	OD	Off-Hook Relay Control Output
TALK	OD	Talk/Data Relay Control Output
LCS	IA	Loop Current Sense Input
Analog Switch/Line Interface		
TXAn	O(DF)	Transmit Analog Outputs
RIN	I(DA)	Receive Analog Input
Analog Switch/Speaker Interface		
SPKR	O(DF)	Speaker Analog Output
SELTXA	OA	Select TXA or SPKR
SELRXA	OA	Select RXA or MIC
General Purpose		
GP0n	I/O	General Purpose Input/Output (GPIO)
Eye Diagnostic Interface		
EYEXY	OA	Serial Eye Pattern X/Y Output
EYECLK	OA	Serial Eye Pattern Clock
EYESYNC	OA	Serial Eye Pattern Strobe
Reference Signals and Modem Interconnects		
VC	MI	Low Voltage Reference
VREF	MI	High Voltage Reference
POR	MI	Power-On-Reset - Connect to RESET
SR1IO	MI	Connect to RMODE and TMODE
TMODE	MI	Transmitter Mode - Connect to SR1IO
RMODE	MI	Receiver Mode - Connect to SR1I0
SRIN3	MI	Connect to RXOUT
RXOUT	MI	Receive Data Out - Connect to SR3IN
SR4OUT	MI	Connect to TXDAT
TXDAT	MI	Transmit Data In - Connect to SR4OUT
IACLK	MI	Connect to CLKIN
CLKIN	MI	Connect to IACLK
IA1CLK	MI	Connect to TRSTROBE
TRSTROBE	MI	Transmitter Strobe - Connect to IA1CLK
SA1CLK	MI	Connect to TRESET
TRESET	MI	Transmitter Reset - Connect to SA1CLK
SLEEP	MI	Connect to PWRDWN
PWRDWN	MI	Connect to SLEEP
SR4IN	MI	Reserved; No external connection
SR3OUT	MI	Reserved; No external connection
SELXTXA	MI	Select External TXA - Reserved; No external connection

Notes:

1. Digital signals are described in Table 10. Analog signals are described in Table 11.
2. R = Required overhead connection; no connection to host equipment.

Table 10. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	Vcc		
Type IC and ID		3.5	–	Vcc		
Input High Current	I_{IH}				µA	V_{CC} = 5.25 V, V_{IN} = 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}					Vdc
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.2 (VCC)		
Input Low Current	I_{IL}	–	–	–400	µA	V_{CC} = 5.25 V
Type IB and IC						
Input Leakage Current	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5 V, V_{CC} = 5.25 V
Types IA and ID						
Output High Voltage	V_{OH}				Vdc	
Types OA and OB		3.5	–	–		I_{LOAD} = – 100 µA
Type OE		2.4	–	–		I_{LOAD} = –40 µA
Output High Current	I_{OH}	–	–	–0.1	mA	
Type OD						
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OE		–		0.4		I_{LOAD} = 0.4 mA
Output Low Current	I_{OL}	–	–	100	µA	
Type OD						
Output Leakage Current	I_{LO}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID		–	5	–		
Type IB		–	20	–		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC and OE						Open drain
Type OD						Clock

Table 11. Analog Characteristics

Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		Input Voltage Range	2.5* ± 1.0 V @ 9600 Hz sample rate
			2.5* ± 0.85 V @ 8000 Hz sample rate
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		Output Voltage Range	2.5* ± 1.0 V @ 9600 Hz sample rate
			2.5* ± 1.25 V @ 8000 Hz sample rate
		D.C. Offset Deviation	< 200 mV
SPKR	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		Output Voltage Range	2.5* ± 1.6 V
		D.C. Offset Deviation	< 20 mV

Note: * 2.5 V is the nominal DC Offset.

FIRMWARE DESCRIPTION

The Advanced FAXENGINE includes a complete software package for the development of a customized facsimile machine. This software operates in a real-time multi-tasking environment. The code is parameterized to allow the developer to easily modify it to meet specific application needs. The modular structure, as shown in Figure 7, allows the developer to replace macros and primitives if further customization is desired.

The basic example/application code supports the following features:

- R96DFXL and R144EFXL modem control
- CCITT T.30 protocol
- DAA control
- CCITT T.4 MH/MR control
- Receive by polling
- Copy
- Scan and transmit
- Receive and print
- Voice/fax discrimination
- Superfine mode
- Operator panel control
- GPIO control

To further increase flexibility, many subroutines are supplied in a link library that allows the developer to easily replace or delete selected routines. Optional features supported by the application code are conditionally assembled. The library and conditional assembly minimize the amount of ROM required, and reduce total system cost. These optional features, which may be conditionally assembled, include:

- CCITT T.30 ECM
- CCITT T.6 MMR and alternate compression/decompression
  - CCITT T.6 MMR control
  - Scan to memory in MMR
  - Transmit from memory in MMR to MR or MH
  - Receive to memory in MMR from MR or MH
  - Transmit in MMR
  - Receive in MMR
- Page memory support
  - Scan to memory
  - Transmit from memory
  - Receive to memory
  - Print from memory
  - Broadcast transmission
  - Delayed transmission
  - Broadcast Polling
  - Delayed Polling
- ARAM mapping
- Digital answering machine (DAM) support
  - RFX96V12 and RFX144V12 modem control
  - Play, save, and delete messages
  - Skip forward and backward
  - Pause and stop
  - Record and play Out Going Message (OGM)
  - Record Incoming Message (ICM)
  - Detect DTMF during OGM
  - Voice prompts (date/time stamps)
  - Variable speed playback
  - Volume control
  - Remote access

By providing the foundation from which production code can be developed, this code helps reduce the developer's time to market. For additional information, see the Advanced FAXENGINE Firmware Description (Order No. 1015).

FAXENGINE MEMORY MAP

Figure 8 shows the Advanced FAXENGINE family memory map.

FAXENGINE INTERFACE CIRCUIT

Figure 9 shows the recommended interface circuits to connect the Advanced FAXENGINE family to the OEM electronics.

PACKAGING

Figure 10 provides the dimensions of the 100-pin PQFP, and Figure 11 provides the dimensions of the 144-pin TQFP.

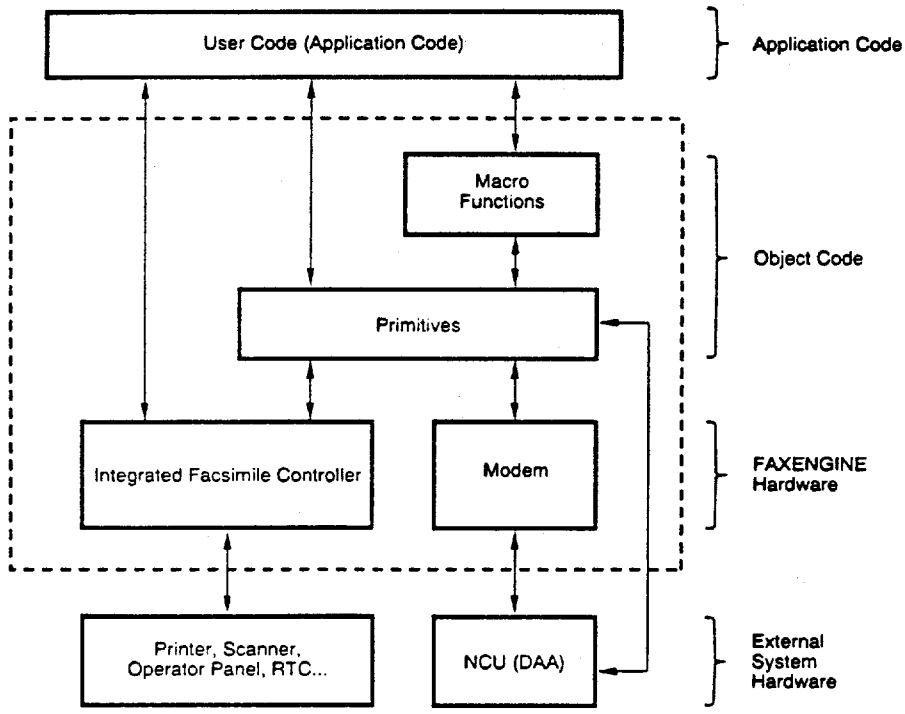


Figure 7. Firmware Interfaces

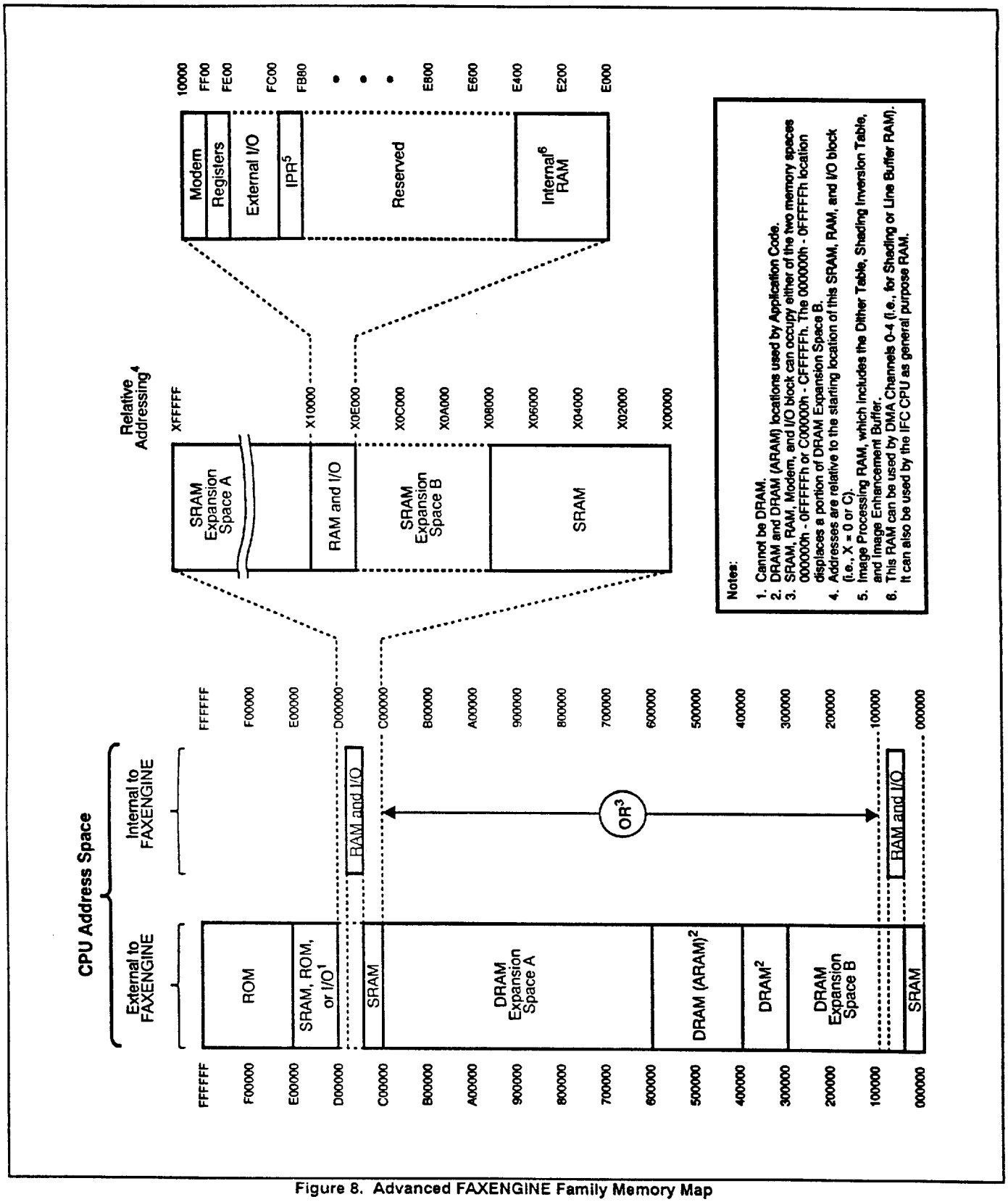


Figure 8. Advanced FAXENGINE Family Memory Map

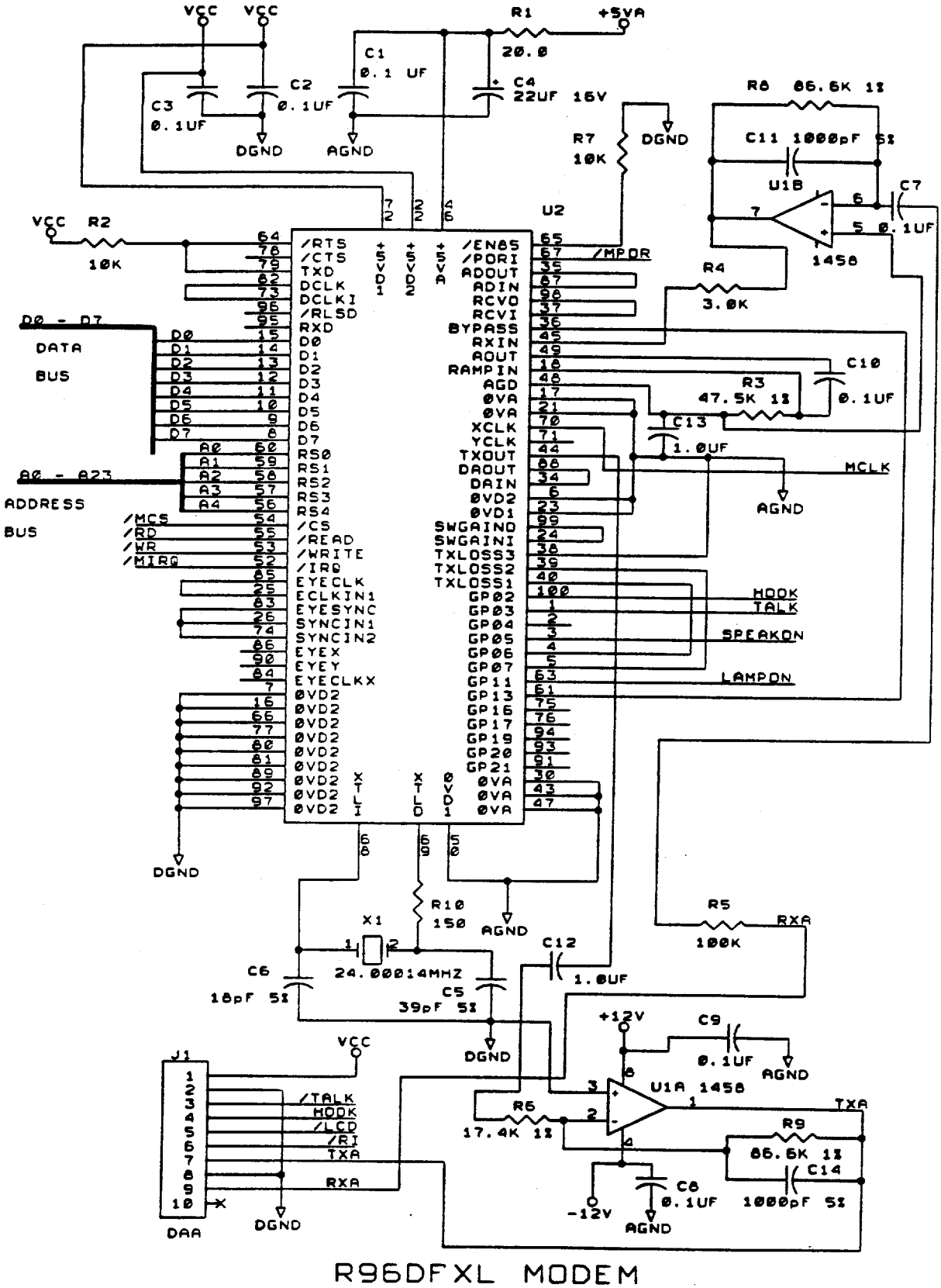


Figure 9. Advanced FAXENGINE Interface Schematic

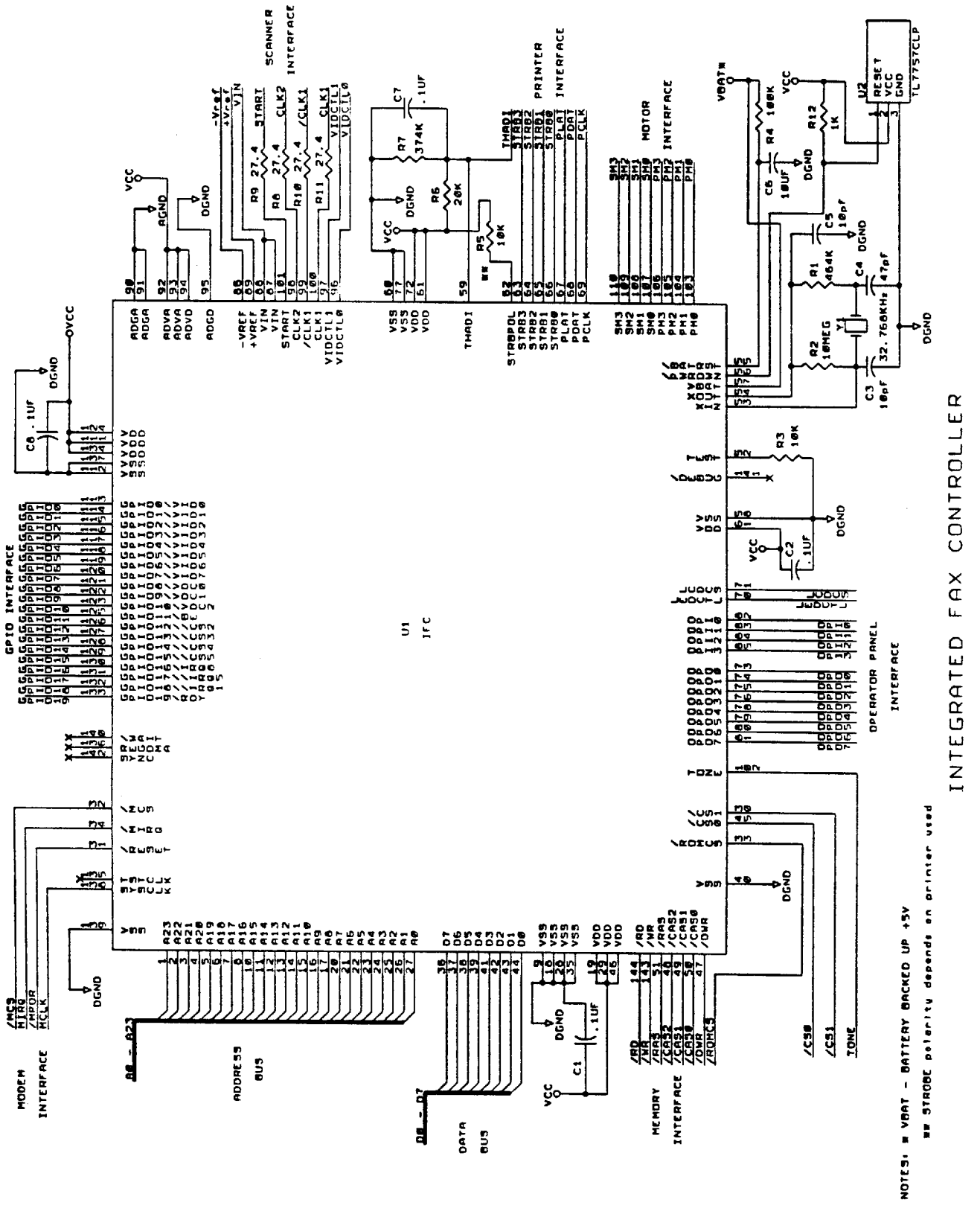
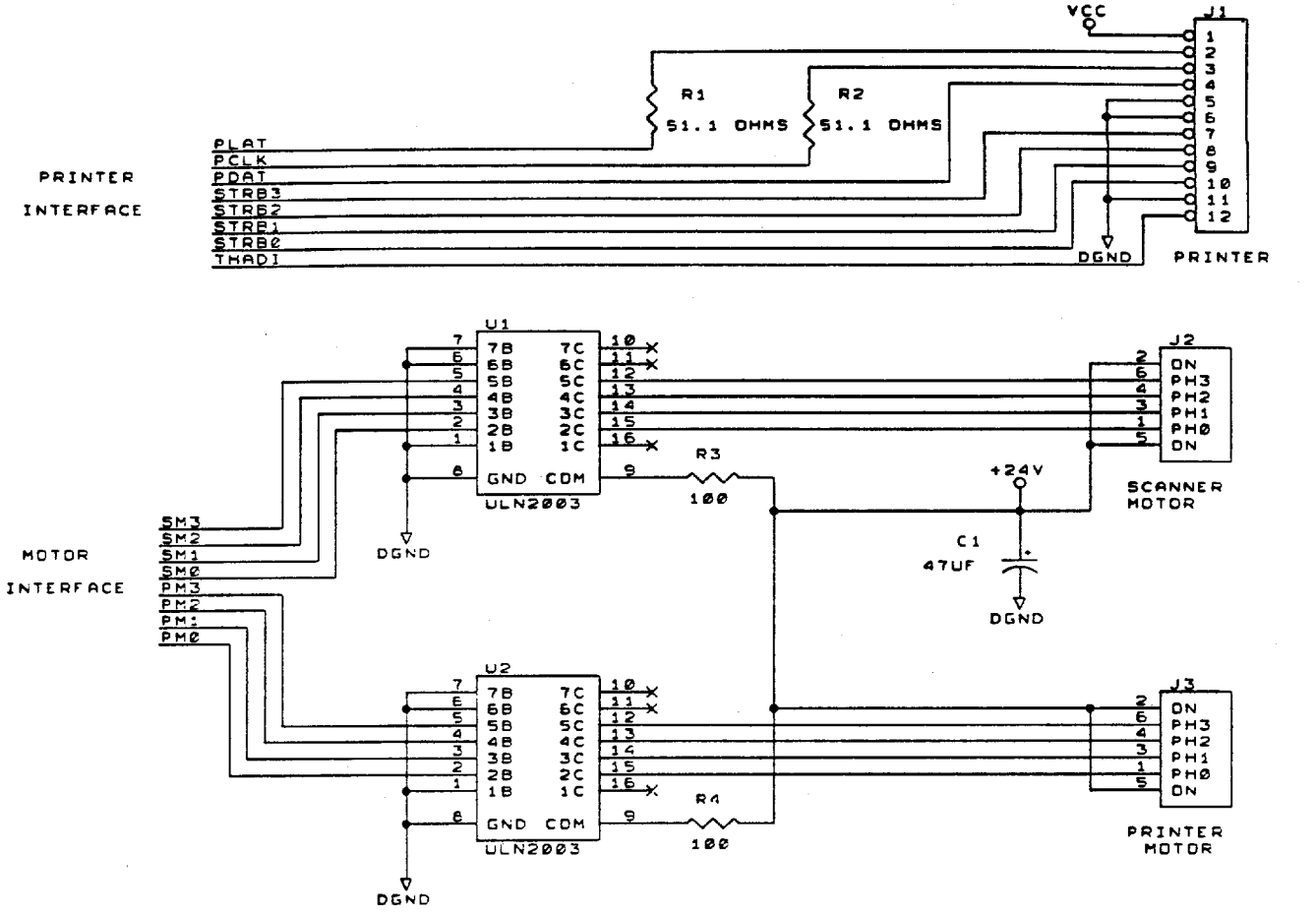
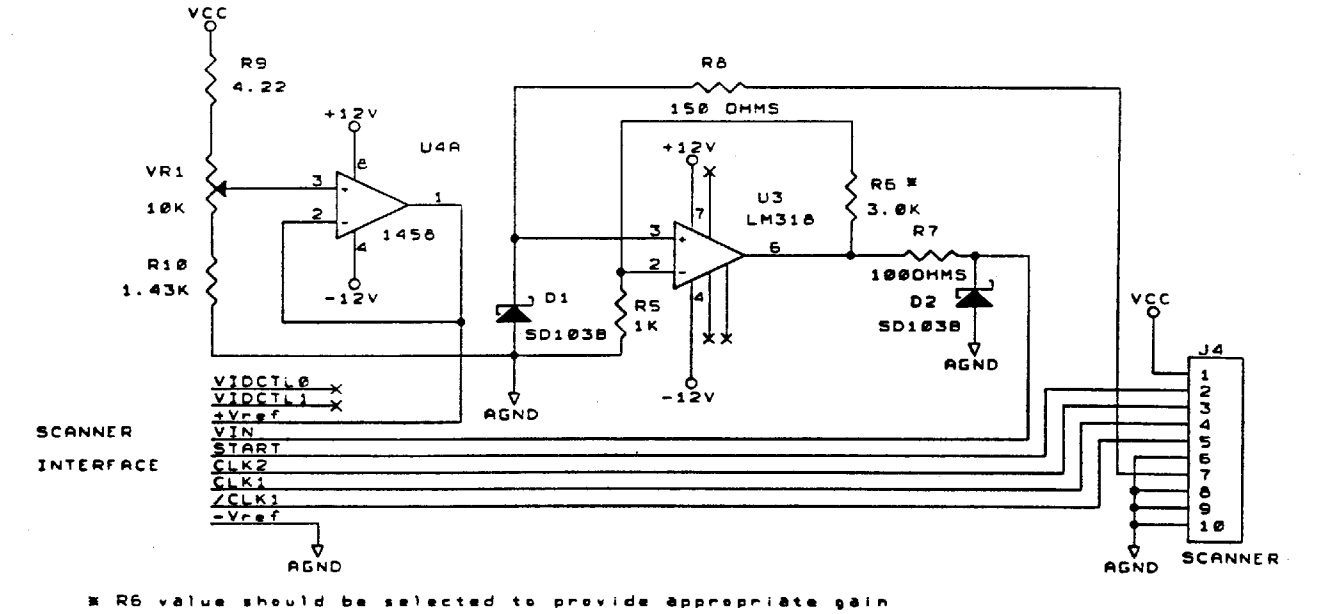


Figure 9. Advanced FAXENGINE Interface Schematic (Cntd)



PRINTER AND MOTOR CIRCUITRY



SCANNER AND VIDEO CIRCUITRY

Figure 9. Advanced FAXENGINE Interface Schematic (Cntd)

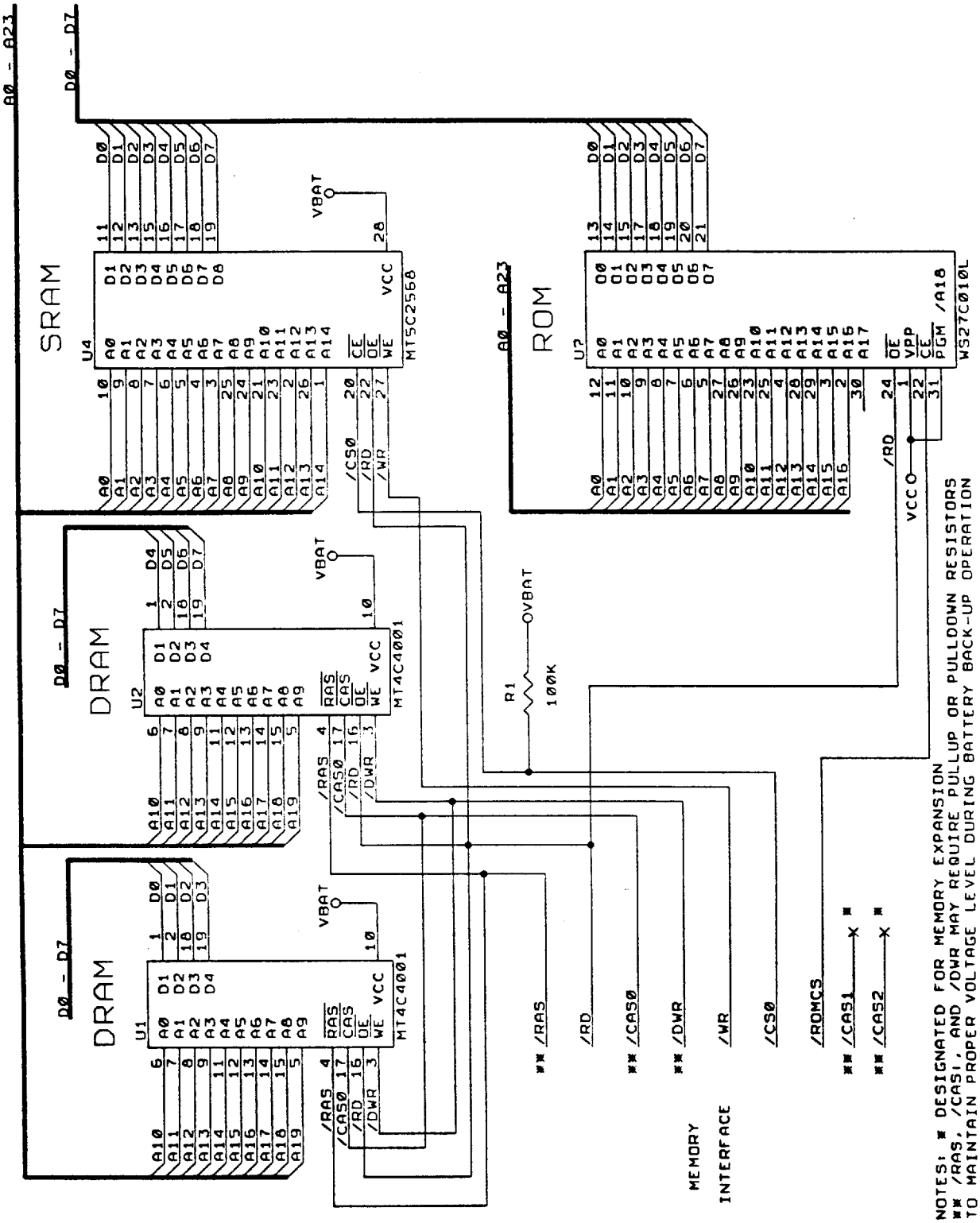


Figure 9. Advanced FAXENGINE Interface Schematic (Cntd)

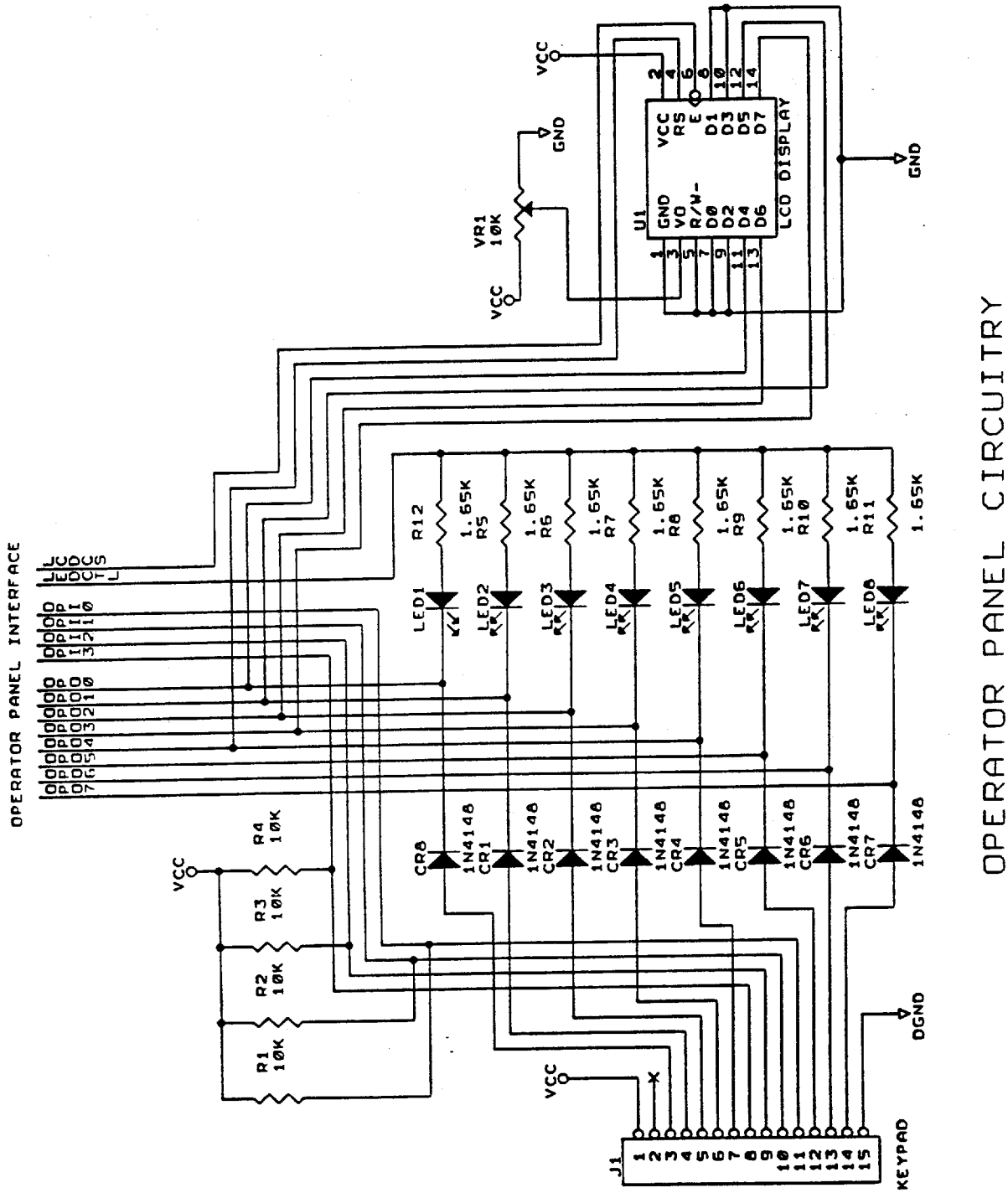
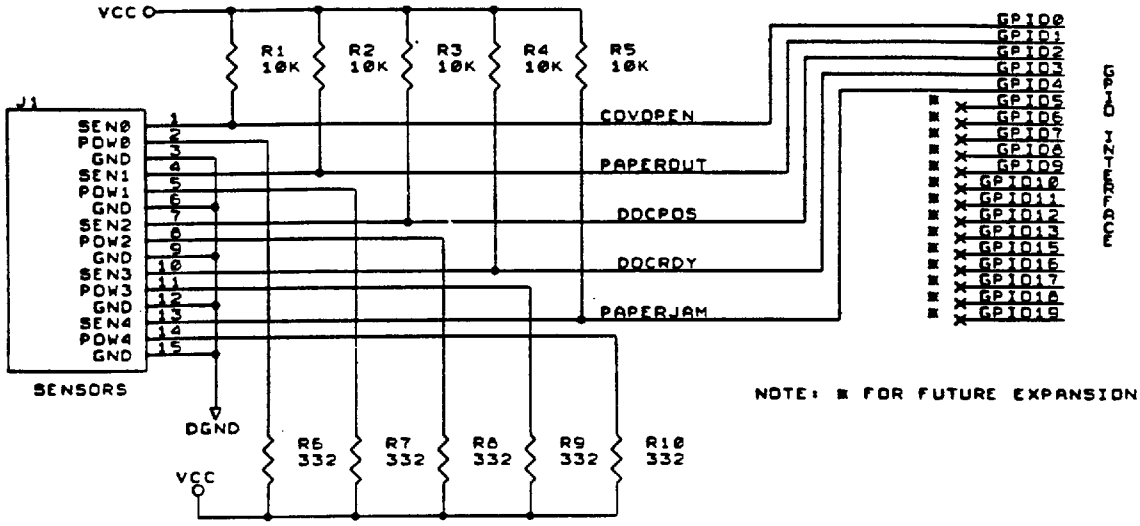
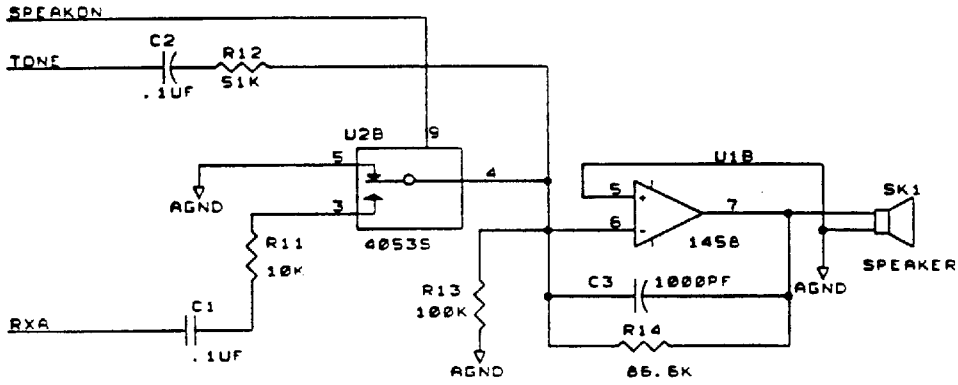


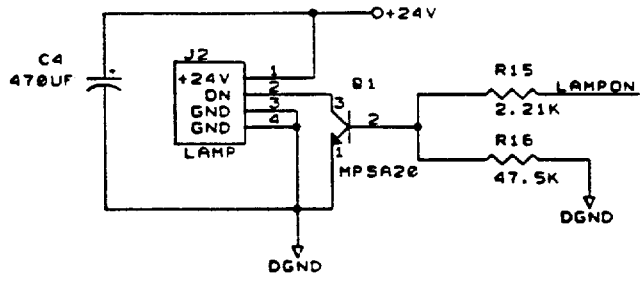
Figure 9. Advanced FAXENGINE Interface Schematic (Cntd)



SENSORS

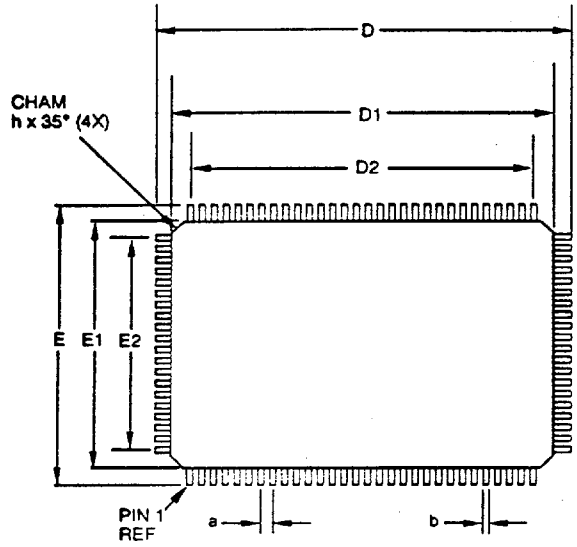


AUDIO CONTROL

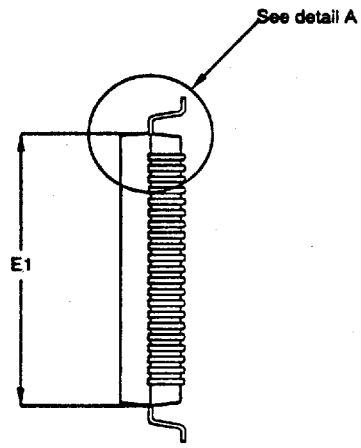


LAMP

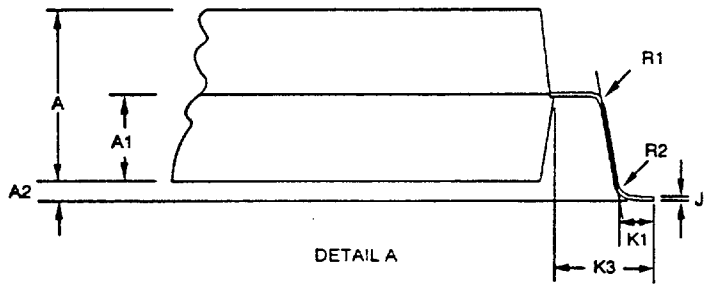
Figure 9. Advanced FAXENGINE Interface Schematic (Cntd)



TOP VIEW



SIDE VIEW

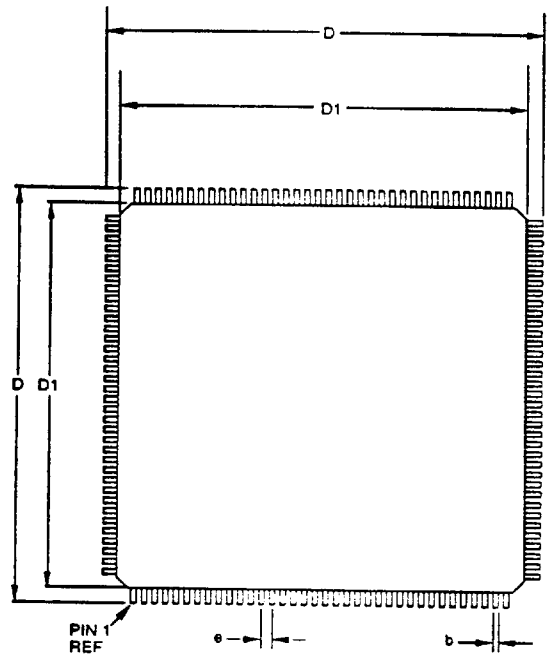


DETAIL A

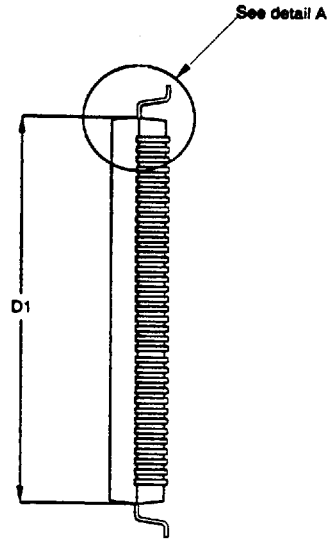
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.25 REF		0.0098	
D	23.05	23.35	0.907	0.919
D1	19.95	20.05	0.785	0.789
D2	18.85 REF		0.7421	
E	17.05	17.35	0.671	0.683
E1	13.95	14.05	0.549	0.553
E2	12.35 REF		0.4862	
K1	0.70	0.90	0.028	0.035
K3	1.60 REF		0.0630	
R1	0.23	—	0.009	—
R2	0.15	0.25	0.006	0.010
a	0.65 REF		0.0256	
b	0.30 REF		0.0118	
h	—	0.50	—	0.020
J	0.1524 REF		0.0060	
Ref: GP00-D234-5/92 (091393)				

Note: * Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

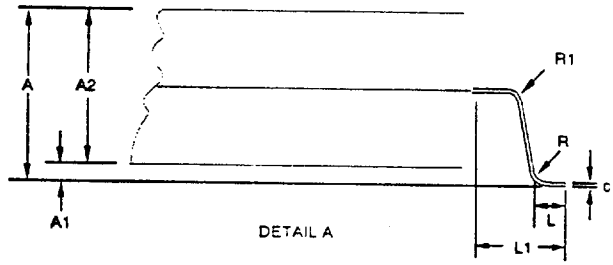
Figure 10. 100-Pin Plastic Quad Flat Package (PQFP)



TOP VIEW



SIDE VIEW



DETAIL A

Dim.	Millimeters Min.	Max.	Inches* Min.	Max.
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
D	22.0 REF		0.8661	
D1	20.0 REF		0.7874	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.0394	
R1	0.08	—	0.003	—
R	0.08	0.20	0.003	0.008
e	0.50 REF		0.0200	
b	0.17	0.27	0.007	0.010
c	0.09	0.20	0.004	0.008

Ref: S-R-PQFP-G (TQFP)-A-08/92-MD-136 (091393)

Note: * Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 11. 144-Pin Thin Quad Flat Package (TQFP)