P54/74FCT3480C/D—P54/74FCT3481C/D
3.3V DUAL ODD-PARITY, DUAL EVEN-PARITY GENERATOR/CHECKERS

FEATURES

- Function and Drive Compatible with the Fastest TTL Logic
- Inputs and Outputs Interface with TTL Logic Levels
- 3.3V ± 0.2V Power Supply and CMOS for Lowest Power Dissipation
- FCT3-D speed at 4.1ns max. (Com'l)
  FCT3-C speed at 4.8ns max. (Com'l)
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- 48 mA Sink Current (Com'l), 32 mA (Mil)
  15mA Source Current (Com'l), 12 mA (Mil)
- Multiple Center Power and Ground Pins
- Input Clamp Diodes to Limit Bus Reflections
- Two 8-Bit Parity Generator/Checkers Per Device
- Open Drain Low-Active Parity Error Widths
- Expandable for Larger Word Widths
- Manufactured in 0.4 micron PACE Technology™

DESCRIPTION

The 'FCT3480 and 'FCT3481 are high speed dual 8-bit parity generator/checkers. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a parity and a parity error output. The 'FCT3480 generates and checks odd parity, while the 'FCT481 generates and checks even parity. In the CHECK mode, the parity output for each generator in the 'FCT3480 ('FCT3481) is low whenever an odd (even) number of inputs is high; the common parity error output in the FCT3480 or the 'FCT3481 is low, indicating a error, if either of the generated parity outputs is high. In the GENERATE mode, the two input parity bits are disabled and each device functions as in the CHECK mode.

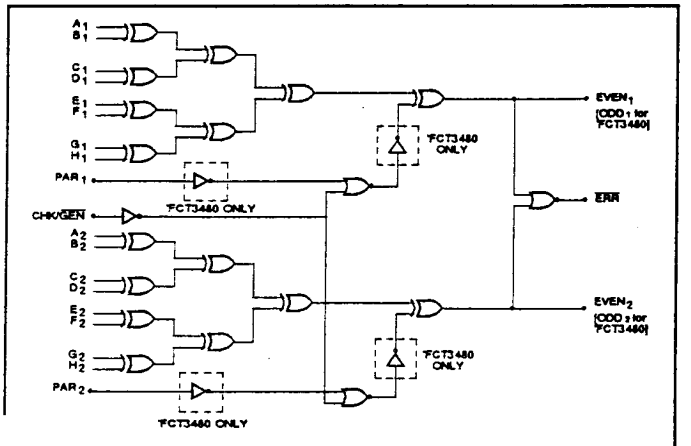
The parity error output is open-drain, designed for easy expansion of the word width by a simple wired-OR connection of several 'FCT3480 and 'FCT3481 type devices. Since additional logic is not needed, the parity generation and checking times remain the same as for each 'FCT480 device.

The 'FCT3480 and 'FCT3481 are manufactured using PACE II Technology™ which is Performance Advanced CMOS Engineered to use 0.4 micron effective channel lengths giving 250 picoseconds loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, and the extra power and extra ground pins, significantly improves switching noise characteristics that would otherwise occur in very high speed circuitry.

The 'FCT3480 and 'FCT3481 are available in 24-pin 300 mil DIP and SOIC packages providing excellent board level densities.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 3.3V.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Functional description only.
Not representative of propagation delays.

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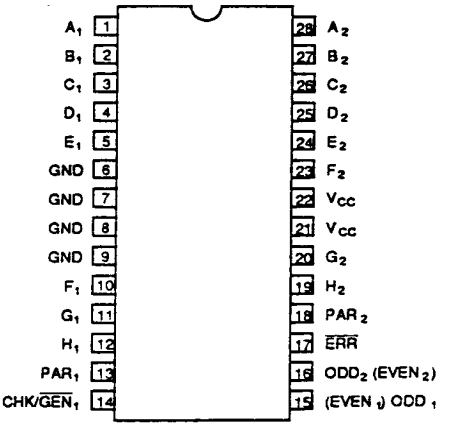

DIP (P4, D4), SOIC (S4)

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PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +5.0	V
I_{IN}	Input Current	–30 to +5.0	mA
I_{OUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS[3]

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+3.1V	+3.5V
Commercial		

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Note:

3. Unless otherwise restricted or extended by detail specifications.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{OZH}	OFF State I_{OUT} HIGH-level Output Current[3]				15	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	OFF State I_{OUT} LOW-level Output Current[3]				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

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Notes:

1. Typical limits are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.001	1.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, $V_{IN} = V_{CC} - 0.6V$[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.2	0.35	mA/MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	2.0	5.0	mA	V_{CC} = MAX, Outputs Open, One Bit Toggling at f_1 = 2.5MHz, 50% Duty Cycle, and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		2.5	7.0	mA	V_{CC} = MAX, Outputs Open, One Bit Toggling at f_1 = 2.5MHz, 50% Duty Cycle, and $V_{IN} = V_{CC} - 0.6V$ or V_{IN} = GND
		7.25	13.75	mA	V_{CC} = MAX, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, 50% Duty Cycle, and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		10.25	22.75	mA	V_{CC} = MAX, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, 50% Duty Cycle, and $V_{IN} = V_{CC} - 0.6V$ or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
2. Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + \Delta I_{CC} \cdot D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS (Minimum values for propagation delays are 1.5 ns, guaranteed by design)

Symbol	Parameter	'FCT3480C 'FCT3481C		'FCT3480D 'FCT3481D		Unit
		Mil.	Com'l.	Mil.	Com'l.	
t_{PLH} t_{PHL}	Propagation Delay A_n to ODD	5.4	4.8	4.8	4.1	ns
t_{PLH}[1] t_{PHL}	Propagation Delay A_n to $\overline{ERR}$	6.1	5.5	5.5	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay CHK/$\overline{GEN}$ to ODD	5.7	5.1	5.1	4.3	ns
t_{PLH}[1] t_{PHL}	Propagation Delay CHK/$\overline{GEN}$ to $\overline{ERR}$	5.5	4.9	4.9	4.2	ns

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Note:

1. t_{PLH} is measured up to $V_{OUT} = V_{OL} + 0.3V$

'FCT3481 TRUTH TABLE

Inputs					Outputs		
A_1 to H_1	A_2 to H_2	CHK/$\overline{GEN}_n$	$OPAR_1$	$OPAR_2$	ODD_1	ODD_2	PER_n
Number of A_1 to H_1 Inputs HIGH is EVEN	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H
	Number of Inputs HIGH A_2 to H_2 is ODD	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
Number of A_1 to H_1 Inputs HIGH is ODD	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
	Number of A_2 to H_2 Inputs HIGH is ODD	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L

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'FCT3480 TRUTH TABLE

Inputs					Outputs		
A_1 to H_1	A_2 to H_2	CHK/$\overline{GEN}_n$	$EPAR_1$	$EPAR_2$	$EVEN_1$	$EVEN_2$	PER_n
Number of A_1 to H_1 Inputs HIGH is EVEN	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L
	Number of Inputs HIGH A_2 to H_2 is ODD	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
Number of A_1 to H_1 Inputs HIGH is ODD	Number of A_2 to H_2 Inputs HIGH is EVEN	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
	Number of A_2 to H_2 Inputs HIGH is ODD	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H

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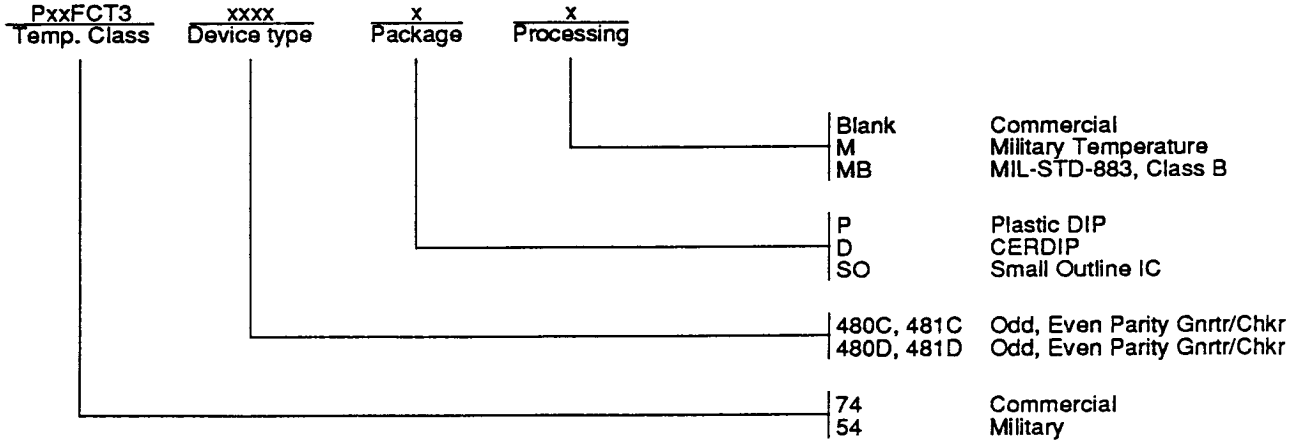
ORDERING INFORMATION



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