

## CD4514BM/CD4514BC, CD4515BM/CD4515BC 4-Bit Latched/4-to-16 Line Decoders

### General Description

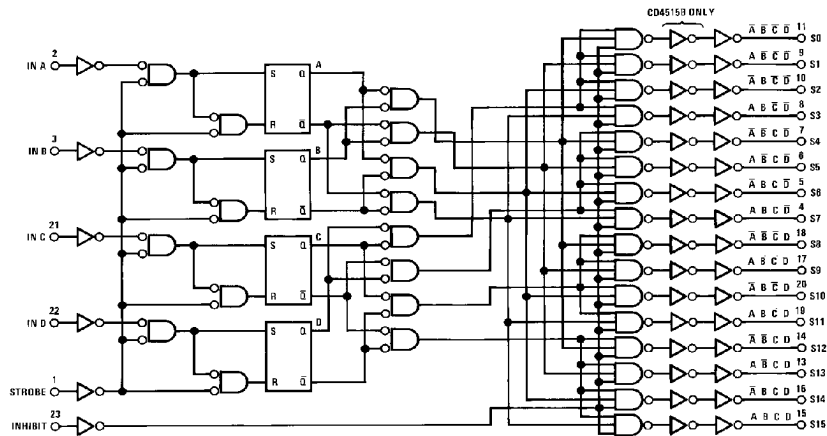
The CD4514B and CD4515B are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514B (output active high option) presents a logical "1" at the selected output, whereas the CD4515B presents a logical "0" at the selected output. The input latches are R-S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

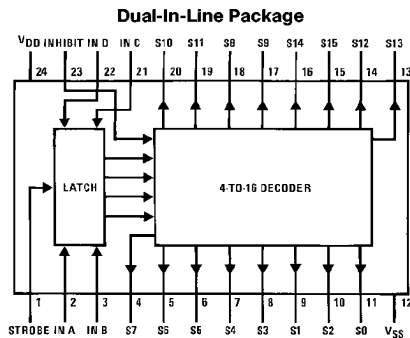
### Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V<sub>DD</sub> (typ.)
- Low power TTL compatibility fan out of 2 driving 74L
- Low quiescent power dissipation 0.025 μW/package @ 5.0 V<sub>DC</sub>
- Single supply operation
- Input impedance = 10<sup>12</sup>Ω typically
- Plug-in replacement for MC14514, MC14515

### Logic and Connection Diagrams



TL/F/5994-1



TL/F/5994-2

### Top View

Order Number CD4514B or CD4515B

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

### Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage ( $V_{DD}$ )	-0.5V to +18V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD}$ + 0.5V
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

### Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	3V to 15V
Input Voltage ( $V_{IN}$ )	0V to $V_{DD}$
Operating Temperature Range ( $T_A$ )	
CD4514BM, CD4515BM	-55°C to +125°C
CD4514BC, CD4515BC	-40°C to +85°C

### DC Electrical Characteristics CD4514BM, CD4515BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		5		0.005	5		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		10		0.010	10		300	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.015	20		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{IH} = V_{DD},  I_O  < 1 \mu A$				0			0.05	V
		$V_{DD} = 5V, V_{IL} = 0V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{IH} = V_{DD},  I_O  < 1 \mu A$								V
		$V_{DD} = 5V, V_{IL} = 0V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
$V_{IL}$	Low Level Input Voltage	$V_O = 0.5V$ or $4.5V$								V
		$V_{DD} = 5V,  I_O  < 1 \mu A$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
$V_{IH}$	High Level Input Voltage	$V_O = 0.5V$ or $4.5V$								V
		$V_{DD} = 5V,  I_O  < 1 \mu A$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
$I_{OL}$	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.90		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.80		2.40		mA
$I_{OH}$	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.90		mA
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.80		-2.40		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		$-10^{-5}$	-0.1		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1		1.0	$\mu A$

### DC Electrical Characteristics CD4514BC, CD4515BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.005	20		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		40		0.010	40		300	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		80		0.015	80		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{IL} = 0V, V_{IH} = V_{DD},  I_O  < 1 \mu A$				0			0.05	V
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{IL} = 0V, V_{IH} = V_{DD},  I_O  < 1 \mu A$								V
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V

## DC Electrical Characteristics CD4514BC, CD4515BC (Note 2) (Continued)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$V_{IL}$	Low Level Input Voltage	$ I_O  < 1 \mu A$ $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$ $V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$ $V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V V V
$V_{IH}$	High Level Input Voltage	$ I_O  < 1 \mu A$ $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$ $V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$ $V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0		V V V
$I_{OL}$	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.90 2.4		mA mA mA
$I_{OH}$	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.52 -1.3 -3.6		-0.44 -1.1 -3.0	-0.88 -2.25 -8.8		-0.36 -0.90 -2.4		mA mA mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.3 0.3		$-10^{-5}$ $10^{-5}$	-0.3 0.3		-1.0 1.0	$\mu A$ $\mu A$

## AC Electrical Characteristics\*

All types  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ,  $t_r = t_f = 20 \text{ ns}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{THL}, t_{TLH}$	Transition Times	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		100 50 40	200 100 80	ns ns ns
$t_{PLH}, t_{PHL}$	Propagation Delay Times	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		550 225 150	1100 450 300	ns ns ns
$t_{PLH}, t_{PHL}$	Inhibit Propagation Delay Times	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		400 150 100	800 300 200	ns ns ns
$t_{SU}$	Setup Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		125 50 38	250 100 75	ns ns ns
$t_{WH}$	Strobe Pulse Width	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		175 50 38	350 100 75	ns ns ns
$C_{PD}$	Power Dissipation Capacitance	Per Package (Note 5)		150		pF
$C_{IN}$	Input Capacitance	Any Input (Note 4)		5	7.5	pF

\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

**Note 4:** Capacitance is guaranteed by periodic testing.

**Note 5:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C and 74C Family Characteristics application note, AN-90.

## Truth Table

**Decode Truth Table (Strobe = 1)**

Inhibit	Data Inputs				Selected Output CD4514 = Logic "1" CD4515 = Logic "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't Care

## AC Test Circuit and Switching Time Waveforms

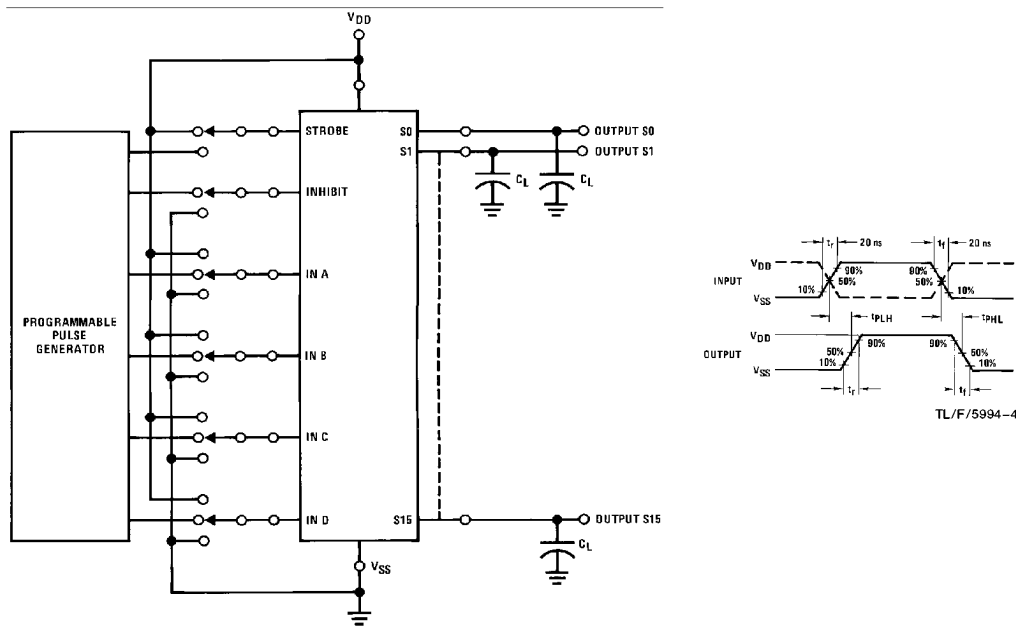


FIGURE 1

TL/F/5994-3

TL/F/5994-4

## Applications

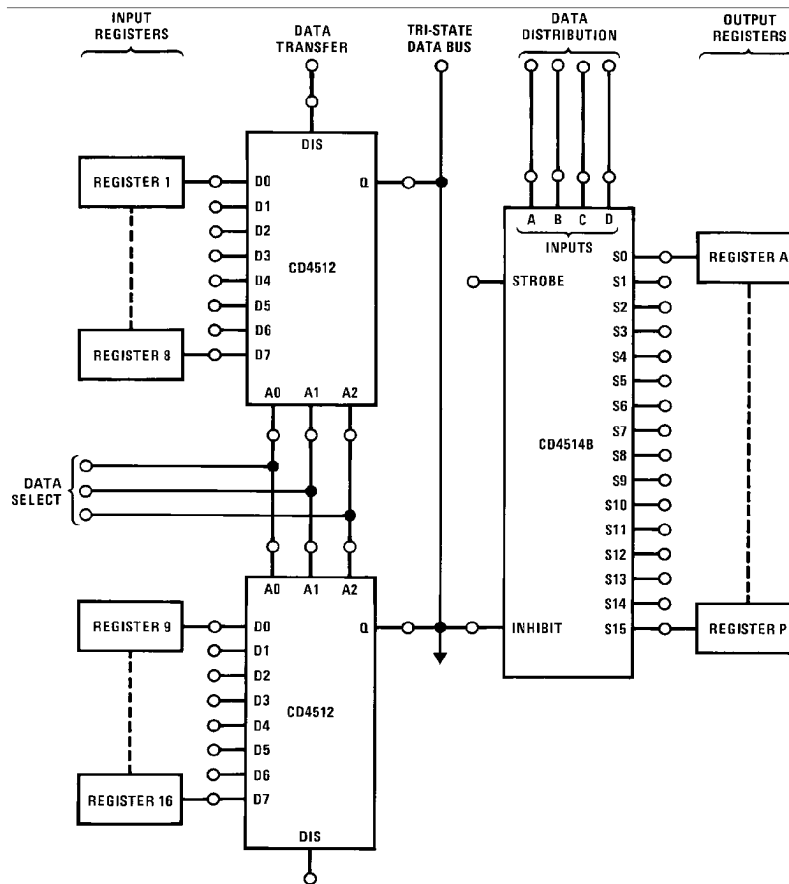
Two CD4512 8-channel data selectors are used here with the CD4514B 4-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a TRI-STATE® data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the 8 inputs on both CD4512 data selectors. One register is assigned to each input. The signals on A0, A1 and A2 choose 1-of-8 inputs for transfer out to the TRI-STATE data bus. A fourth signal, labelled Dis, disables one of the CD4512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1–16, the rate of transfer of the sequential information can also be varied. That is, if the CD4512 were addressed at a rate that is

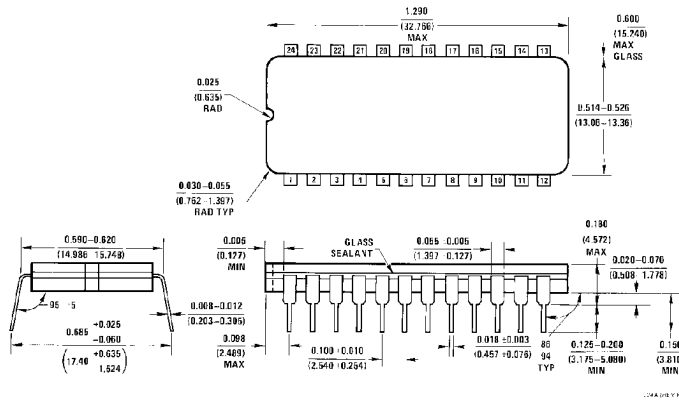
8 times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the TRI-STATE bus is redistributed by the CD4514B 4-bit latch/decoder. Using the 4-bit address, INA–IND, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A–P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

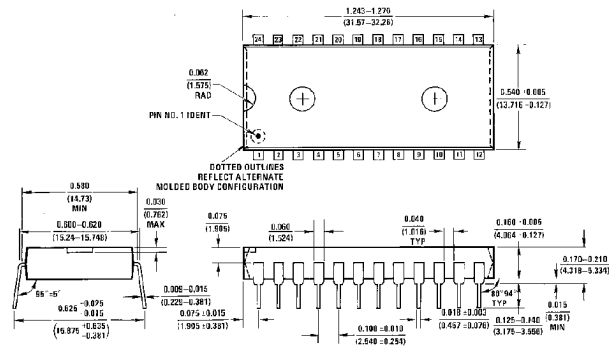


TL/F/5994-5

**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number CD4514BMJ, CD4514BCJ, CD4515BMJ or CD4515BCJ**  
**NS Package Number J24A**



**Molded Dual-In-Line Package (N)**  
**Order Number CD4514BMN, CD4514BCN, CD4515BMN or CD4515BCN**  
**NS Package Number N24A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: cnjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
 Tel: 81-043-299-2309  
 Fax: 81-043-299-2406

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.