HDMI Switch ICs

1 for input 1 output buffer (Sync with OE)

BU16025MUV

No.11063EAT06

ROHM Electronic Components — Pb Free
Directive Compliance — RoHS

●Description

BU16025MUV is HDMI Buffer IC for Source, Sink, and repeater equipment. Each TMDS input has internal 50ohm resistor. These resistors can be turned off by OE pin control. And BU16025MUV has selectable equalizer circuit and DDC active buffer to isolate capacitor between input and output.

●Features

1) Support 480i/p, 720p, and 1080i/p 12bit deep color and 2.70Gbps data rate
2) 5V Tolerance to all DDC and HPD_SINK Inputs
3) Integrated active DDC buffer
4) Integrated DDC data line delay mode to get hold margin
5) Integrated Switchable 50Ω Receiver Termination
6) Integrated Low TMDS output swing mode for High speed signal
7) High Impedance Outputs When Disabled
8) TMDS Inputs and output HBM ESD Protection Exceeds 8kV
9) Support AC coupling input (TMDS input common mode voltage is 3.3V)
10) Selectable Receiver Equalization
11) Integrated I^2C Identification Data for HDMI/DVI distinction (Display port translator mode)
12) 48-Pin VQFN Package
13) ROHS Compatible

●Applications

Digital TV, DVD player, set-top box, AV receiver, Digital projector, Desktop/Note book PC

●Absolute maximum ratings

Parameter	Ratings	Unit
Input Voltage	-0.3～+4.5	V
DDC, HPD_SINK input voltage	-0.3～+5.5	V
Differential pin input voltage	+2.5～+4.0	V
PRE, I2C_ONB, SELREF, OEB, EQ, DDC_TI, DDCEN, HDMID_EN, HPDINV input voltage	-0.3～+4.0	V
Power Dissipation rating	2123(*1)	mW
Storage temperature	-55～+125	℃

*1 ROHM standard substrate When it's used by than Ta=25℃, it's reduced by 21.2mW/℃

●Operating conditions

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Operating free-air temperature	T_A	0	-	70	℃
TMDS DIFFERENTIAL PINS (A/B)					
Input differential voltage range	V_{ID}	150	-	1560	mVp-p
Input common voltage range	V_{IC}	1.5	-	V_{CC}+0.01	V
Current control resistor	REXT	1.18	1.2	1.22	kΩ
TMDS output voltage range	AV_{CC}	3	3.3	3.6	V
Termination Resistor	R_T	45	50	55	Ω
Signal rate	-	-	-	2.70	Gbps
CONTROL PINS (PRE, I2C_ONB, OEB, SELREF, EQ, DDC_TI, DDCEN, HDMIID_EN, HPDINV)					
H level input voltage	V_{IH}	0.7×Vcc	-	V_{CC}	V
L level input voltage	V_{IL}	-0.3	-	0.3×Vcc	V
DDC I/O PINS (SCLx, SCLy, SDAx, SDAy)					
I2C data rate	$d_{R(I2C)}$	-	-	100	kHz
SDAx, SCLx					
H level input voltage	V_{IH}	2.1	-	5.5	V
L level input voltage	V_{IL}	-0.3	-	0.35	V
SDAy , SCLy					
H level input voltage	V_{IH}	2.1	-	5.5	V
L level input voltage	V_{IL}	-0.3	-	1.5	V
STATUS PINS (HPD_SINK)					
H level input voltage	V_{IH}	2.1	-	5.5	V
L level input voltage	V_{IL}	-0.3	-	0.8	V

●Electrical characteristics(Unless Otherwise noted Ta=25℃, Vcc=3.3V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Stand by Current (DDC_EN= "L")	Ist	-	-	10	µA	OEB = "Vcc", V_{IL}= "0V",V_{IH}="Vcc"
Stand by Current2 (DDC_EN= "H")	Ist2	-	1.8	3.0	mA	OEB = "Vcc", V_{IL}= "0V",V_{IH}="Vcc"
Circuit Current	Icc	-	68+32[*(1)]	84+32[*(1)]	mA	V_{IH} = Vcc,V_{IL} = Vcc-0.4V, REXT=1.2kΩ, R_T = 50Ω, AVcc = 3.3V,PRE=0V Am/Bm =2.25 Gbps HDMI data pattern, m = 2,3,4, A1/B1 = 225 MHz clock
Power Consumptions	P_D	-	-	381	mW	V_{IH} = Vcc,V_{IL} = Vcc-0.4V REXT=1.2kΩ, R_T = 50Ω, AVcc = 3.3V, PRE=0V Am/Bm = 2.25Gbps HDMI data pattern, m = 2,3,4, A1/B1 = 225 MHz clock
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
H level output voltage	V_{OH}	AVcc-10	-	AVcc+10	mV	AVcc = 3.3V, R_T = 50Ω ,PRE = 0V
L level output voltage	V_{OL}	AVcc-600	-	AVcc-400	mV	
Swing voltage	V_{SWING}	400	-	600	mV	
Swing voltage2 (Low TMDS output swing mode)	$V_{SWING 2}$	600	-	920	mVp-p	PRE = Vcc, Am/Bm =225 Mbps HDMI data pattern, m = 2,3,4, A1/B1 = 225 MHz clock
TMDS internal Resistor	R_{INT}	45	50	55	Ω	V_{IN} = 2.9V
Output leak current	Voff	-10	0	10	µA	AVcc = 3.3V, Vcc=0V
DDC Input and output						
SDAx, SCLx						
Input leak current	I_{IH1}	-10	-	10	µA	V_I = 5.5V
Input leak current	I_{IH2}	-10	-	10	µA	V_I = Vcc
H level output current	I_{OHT}	-10	-	10	µA	V_O = 5.5V
L level output current	I_{IL}	-10	-	10	µA	V_{IL} = GND
L level output voltage	V_{OLT}	0.43	-	0.57	V	RL = 4.7kΩ	SELREF = "L"
		0.52	-	0.87			SELREF = "H"
L level input voltage below output voltage	V_{OLT}-V_{IL}	-	100	-	mV		SELREF = "L"
		-	400	-			SELREF = "H"
SDAy , SCLy						
Input leak current	I_{IH1}	-10	-	10	µA	V_I = 5.5V
Input leak current	I_{IH2}	-10	-	10	µA	V_I = Vcc
H level output current	I_{OH}	-10	-	10	µA	V_O = 5.5V
L level output current	I_{OL}	-10	-	10	µA	V_{IL} = GND
L level output voltage	V_{OL}	-	-	0.2	V	I_{OUT} = 4mA
STATUS PINS (HPD)						
H level output voltage	V_{OH}	2.4	-	Vcc	V	I_{OH} = - 8mA
L level output voltage	V_{OL}	0	-	0.4	V	I_{OL} = 8mA
CONTROL PINS (PRE, OEB, DDCEN, HPDINV)						
H level input current	I_{IH}	-10	-	10	µA	V_{IH} = Vcc
L level input current	I_{IL}	-10	-	10	µA	V_{IL} = GND
CONTROL PINS (SELREF, EQ, DDC_TI)						
H level input current	I_{IH}	50	-	150	µA	V_{IH} = Vcc
L level input current	I_{IL}	-10	-	10	µA	V_{IL} = GND
CONTROL PINS (I2C_ONB, HDMIID_EN)						
H level input current	I_{IH}	-10	-	10	µA	V_{IH} = Vcc
L level input current	I_{IL}	-150	-	50	µA	V_{IL} = GND

(*1) 32mA is the current through TMDS internal resistor

●AC Characteristic (Unless Otherwise noted Ta=25℃, Vcc=3.3V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
TMDS Output Differential pin (Y/Z)						
Differential output rise time (20%-80%)	t_{R_tmds}	-	110	-	ps	AV$_{CC}$ = 3.3V, R$_T$ = 50Ω, PRE ="H"
Differential output rise time (20%-80%)	t_{F_tmds}	-	110	-	ps	
Differential intra pair skew (Fig9)	$t_{sk(D)}$	-	35	-	ps	
DDC I/O Pin　(SCLx, SCLy, SDAx, SDAy)						
Propagetion delay (L to H) SCLx to SCLy	t_{PLH1}	-	30	-	ns	R$_L$ = 4.7KΩ C$_L$ = 10pF DDC_TI = "H"
Propagetion delay (H to L) SCLx to SCLy	t_{PHL1}	-	10	-	ns	
Propagetion delay (L to H) SCLy to SCLx	t_{PLH2}	-	40	-	ns	
Propagetion delay (H to L) SCLy to SCLx	t_{PHL2}	-	20	-	ns	
Propagetion delay (L to H) SDAx to SDAy	t_{PLH3}	-	570	-	ns	R$_L$ = 4.7KΩ C$_L$ = 10pF DDC_TI = "H"
Propagetion delay (H to L) SDAx to SDAy	t_{PHL3}	-	570	-	ns	
Propagetion delay (L to H) SDAy to SDAx	t_{PLH4}	-	370	-	ns	
Propagetion delay (H to L) SDAyto SDAx	t_{PHL4}	-	370	-	ns	
Propagetion delay (L to H) SDAx/SCLx to SDAy/SCLy	t_{PLH5}	-	30	-	ns	R$_L$ = 4.7KΩ C$_L$ = 10pF DDC_TI = "L"
Propagetion delay (H to L) SDAx/SCLx to SDAy/SCLy	t_{PHL5}	-	10	-	ns	
Propagetion delay (L to H) SDAy/SCLy to SDAx/SCLx	t_{PLH6}	-	40	-	ns	
Propagetion delay (H to L) SDAy/SCLy to SDAx/SCLx	t_{PHL6}	-	20	-	ns	
SDAx/SCLx output rise time	t_{R1}	-	80	-	ns	R$_L$ = 4.7KΩ C$_L$ = 10pF
SDAx/SCLx output rise time	t_{F1}	-	5	-	ns	
SDAy/SCLy output rise time	t_{R2}	-	95	-	ns	
SDAy/SCLy output rise time	t_{F2}	-	5	-	ns	
STATUS PINS(HPD)						
Propagation delay time (L to H)	$t_{PLH(HPD)}$	-	100	-	ns	C$_L$=10pF
Propagation delay time (H to L)	$t_{PHL(HPD)}$	-	100	-	ns	C$_L$=10pF

●Electrical characteristic curves (Reference data)
Unless Otherwise noted Ta=25°C, Vcc=3.3V
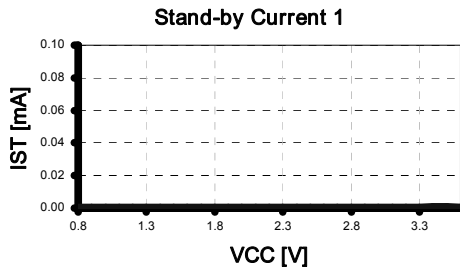

Fig.1   Stand-by Current 1(Ist)
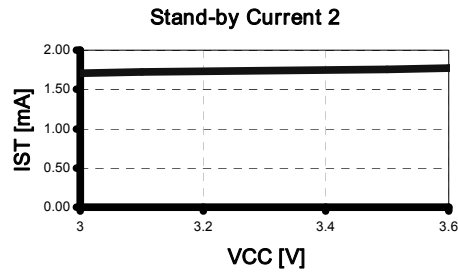OEB = "Vcc", DDC_EN= "0V"

Fig.2   Stand-by Current 2(Ist2)
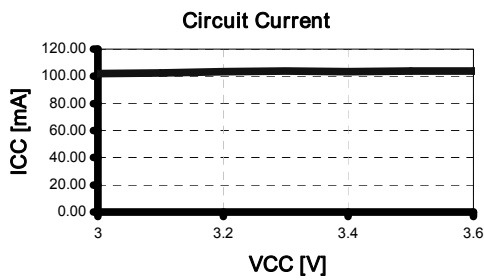OEB = "Vcc", DDC_EN= "Vcc"

Fig.3   Circuit Current(Vcc + AVcc) (Icc)
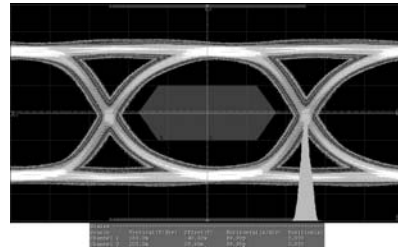OEB = "Vcc", DDC_EN= "0V"

Fig.4   Eye Diagram of BU16025MUV
2.25Gbps Data rate when PRE = "L",
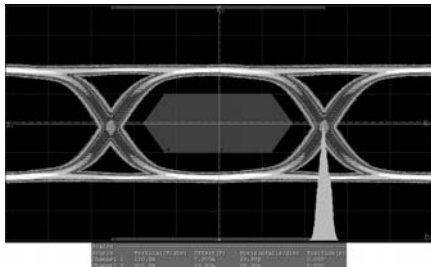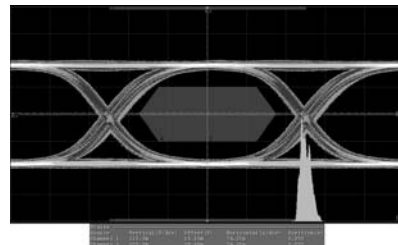Test Equipment DTG5334(tektronix),
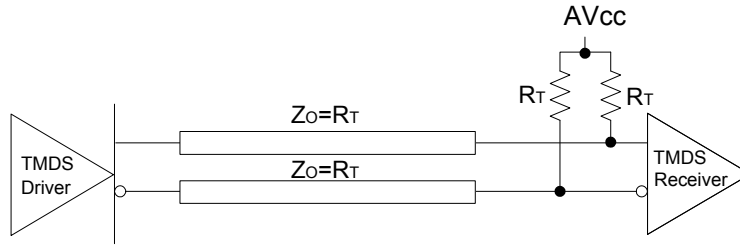DSA80000B(Agilent)

Fig.5   Eye Diagram of BU16025MUV
2.25Gbps Data rate when PRE = "H",
Test Equipment DTG5334(tektronix),
DSA80000B(Agilent)

Fig.6   Eye Diagram of BU16025MUV
2.7Gbps Data rate when PRE = "H",
Test Equipment DTG5334(tektronix),
DSA80000B(Agilent)

●Measurement symbol and circuit diagram

Fig 7   TMDS Output driver

$VID = VA - VB$ $Vswing = VY - VZ$

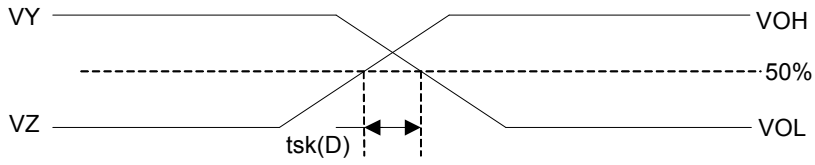Fig8   Test circuit and definition

Fig9   Definition of differential intra pair skew
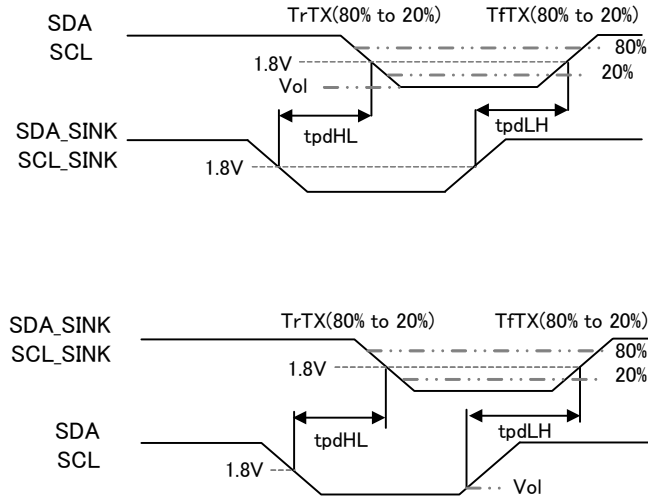

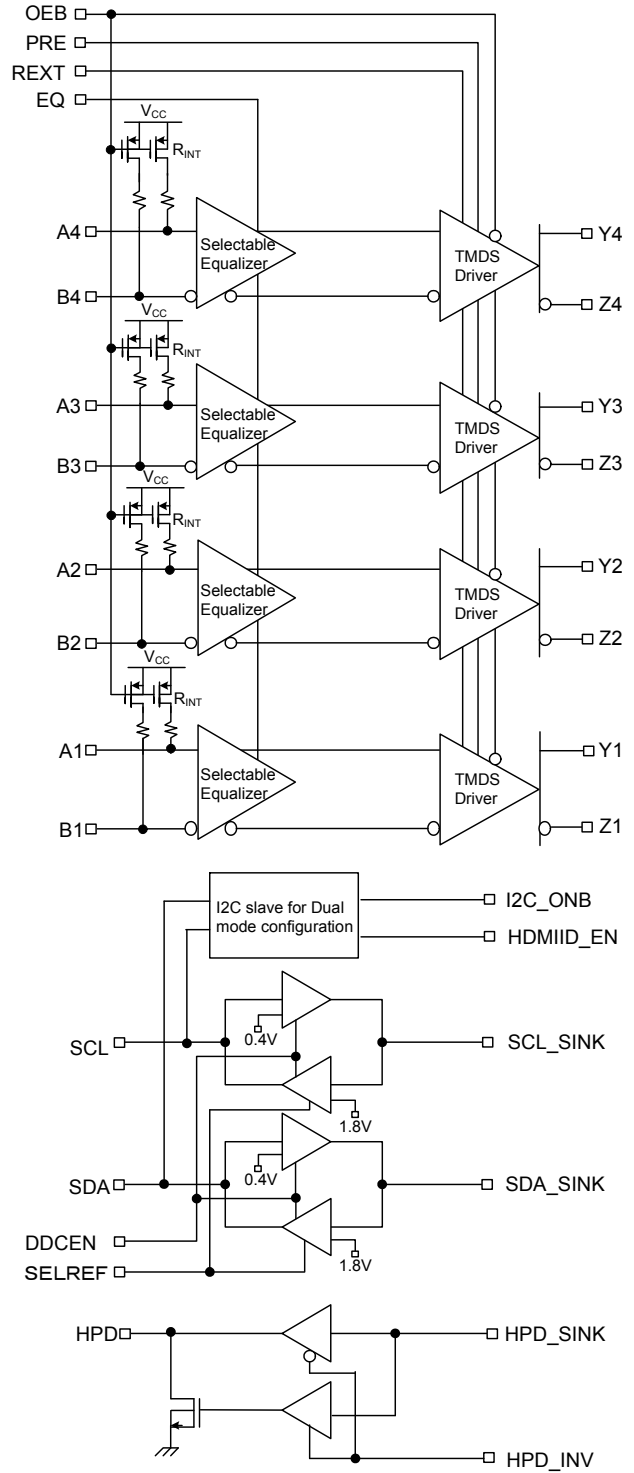Fig10   DDC timing definitions

●Block diagram and pin configuration

Fig.11   Block Diagram of BU16025MUV
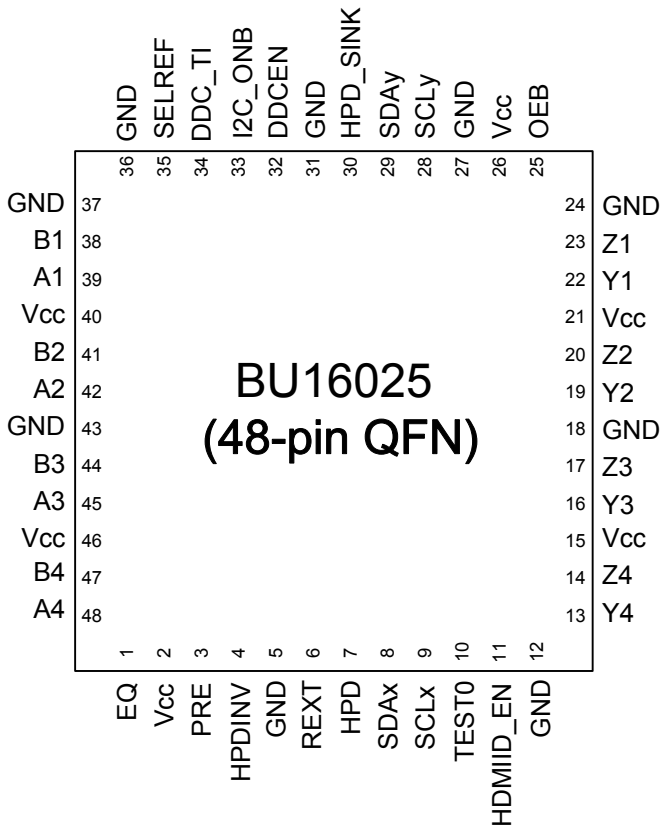
●Pin Explanation

Pin		I/O	Explanations
Name	Number		
B1, B2, B3, B4	38, 41, 44, 47	Input	TMDS Negative input
A1, A2, A3, A4	39, 42, 45, 48	Input	TMDS Positive input
Z1, Z2, Z3, Z4	23, 20, 17, 14	Output	TMDS Negative input
Y1, Y2, Y3, Y4	22, 19, 16, 13	Output	TMDS Positive input
EQ	1	Input	Equalizer gain setting(40kΩ internal pull down) "L" 5dB "H" 15dB
PRE	3	Input	TMDS Low output swing mode(Recommend High) Low : OFF High : ON
HPDINV	4	Input	HPD output select switch Low : non-invert High : Invert and open drain output
REXT	6	Input	TMDS Current control pin(via 1. 2kΩ to GND)
HPD	7	Output	Hot plug detect output [*1]
SDAx	8	Inout	DDC Data line(*2 Vol = 0.5V)
SCLx	9	Inout	DDC Clock line(*2 Vol = 0.5V)
TEST0	10	Input	Open or Gnd
HDMIID_EN	11	Input	HDMI ID Enable(40kΩ internal pull up) [*3] Low : 0xFF(DVI) High : ASCII (HDMI)
OEB	25	Input	TMDS line internal resistor and output enable switch Low : ON(Enable) High : High-Z
SCLy	28	Inout	DDC Clock line[*2]
SDAy	29	Inout	DDC Data line[*2]
HPD_SINK	30	Input	Hot plug detect input(10kΩ internal pull down)
DDCEN	32	Input	I^2C Repeater Enable Low : High-Z High : Enable
I2C_ONB	33	Input	Built-in I^2C Slave Enable Switch(90kΩ internal pull up) [*3] Low : ON High : OFF
DDC_TI	34	Input	DDC Data hold margin setting (40kΩ internal pull down) [*4] DDC_TI = "L" Delay from SDAx to SDAy = 570nsec, Delay from SCLx to SCLy = 20nsec Delay from SDAy to SDAx = 370nsec, Delay from SCLy to SCLx = 20nsec DDC_TI = "H" Delay from SDAx to SDAy = 20nsec, Delay from SCLx to SCLy = 20nsec Delay from SDAy to SDAx = 20ncec, Delay from SCLy to SCLx = 20nsec
SELREF	35	Input	SCLx/SDAx L level output voltage select (40kΩ internal pull down)
V$_{CC}$	2 ,15, 21, 26, 40, 46	-	Power
GND	5, 12, 18, 24, 27, 31, 36, 37, 43	-	Ground

(*1) HPD_OFF mode sets Hot plug detect output to High impedance. Except HPD_OFF mode, HPD is always active.
(*2) SDAx/SCLx, SDAy/SCLy have different L level input and output voltage. Please refer recommended operating condition in detail
(*3) HDMIID_EN, I2C_ONB don't need to be Enable except using internal I^2C slave.
(*4) Data hold time increases when DDC_TI= "L". But Data setup time and holdtime of Start condition decrease.

●Look up table of I2C_ONB and HDMIID_EN pin

Name	Pin setting				Output state			
	OEB	DDCEN	I2C_ONB	HDMI ID_EN	I^{2}C Buffer	Internal I^{2}C slave	HPD	TMDS Internal R
Normal mode (recommend)	L	L	H	H	OFF	OFF	active	ON
	L	H	H	H	active	OFF	active	ON
HPD_OFF mode	L	L	H	L	OFF	OFF	High Impedance	ON
	L	H	H	L	active	OFF	High Impedance	ON
TMDS_OFF mode	H	L	H	H	OFF	OFF	active	OFF
	H	H	H	H	active	OFF	active	OFF
HPD_TMDS_OFF mode	H	L	H	L	OFF	OFF	High Impedance	OFF
	H	H	H	L	active	OFF	High Impedance	OFF
Display Port Translator mode (HDMI)	-	H	L	H	active	(HDMI)	active	OFF
Display Port Translator mode (DVI)	-	H	L	L	active	(DVI) 0xFF	active	OFF
None	-	L	L	-	OFF	OFF	active	OFF

Display Port Translator mode
DisplayPort Translator mode are used to access internal I2C slave. I2C Slave register stores value like below. The ASCII code of this value is "DP-HDMI　ADAPTOR<EOT>
Please read from address 0x00 to 0x0F at the read cycle.

Slave adr : 7'b100_0000

I2C_ONB	HDMIID_EN	Acknowledge (from slave)	Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
L	H : HDMI Connect	Occur	Data	0x44	0x50	0x2D	0x48	0x44	0x4D	0x49	0x20	0x41	0x44	0x41	0x50	0x54	0x4F	0x52	0x04
	L : DVI Connect	Occur	Data	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
H	-	None	Data	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

When I2C_ONB=1, slave adr 7'b100_0000 is disabled

I²C Slave Read access to register block

step 1	0
I²C Start(Master)	S

S : Start Condition

step 2	7	6	5	4	3	2	1	0
I²C Device Address Write(Master)	1	0	0	0	0	0	0	0

Write

step 3	9
I²C Acknowledge(Slave)	A

A : Acknowledge

step 4	7	6	5	4	3	2	1	0
I²C Logic Address(Master)	0	0	0	0	0	0	0	0

step 5	9
I²C Acknowledge(Slave)	A

step 6	0
I²C Stop(Master)	P

P : Stop Condition

step 7	0
I²C Start(Master)	S

step 8	7	6	5	4	3	2	1	0
I²C General Address Read(Master)	1	0	0	0	0	0	0	1

Read

step 9	9
I²C Acknowledge(Slave)	A

step 10	7	6	5	4	3	2	1	0
I²C Read Data(Slave)	Data	Data	Data	Data	Data	Data	Data	Data

step 11	9
I²C Not-Acknowledge(Master)	X

X : A (Acknowledge) or ~A (Not-Acknowledge)

When X =A, Address pointer is incremented and repeat step10.
When X =~ A,   I²C slave reg stops and moves to step12.

step 12	0
I²C Stop(Master)	P

● I/O equivalence circuit
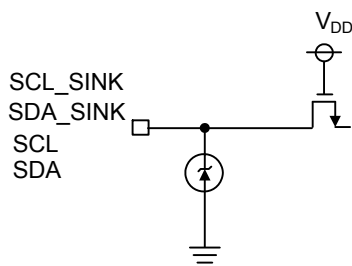
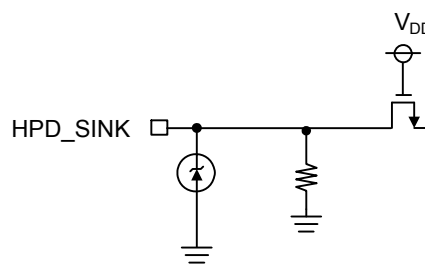TMDS Input Stage   Control Input Stage
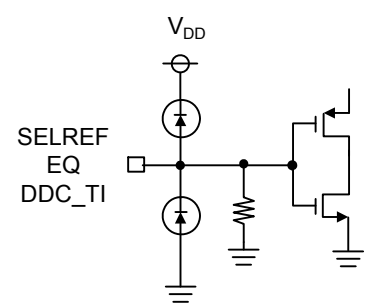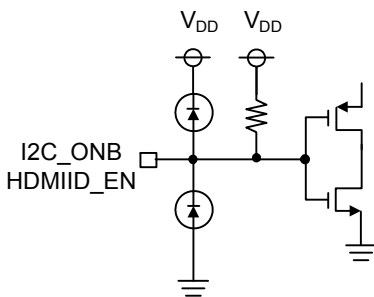

I²C Input/Output Stage   HPD_SINK Input Stage   Control Input Stage
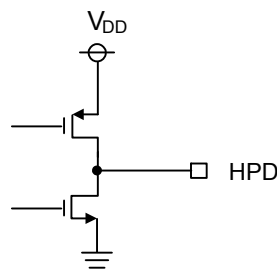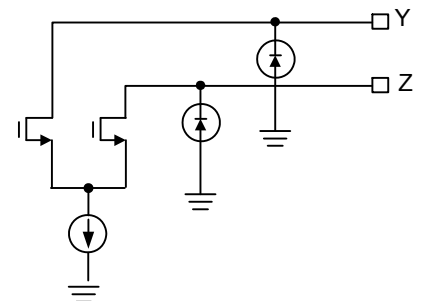

Control Input Stage   HPD Output Stage   TMDS Output Stage

●Notes for use

1) Internal Resistor about HPD_SINK
   For the reason HPD_SINK pin have internal resistor of 10kohm like below, don't put external resistor.
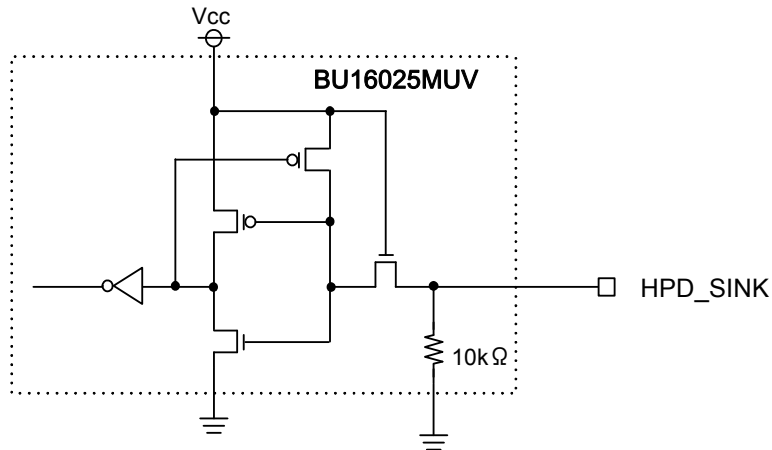

Fig12   HPD_SINK I/O schematic

2) About unused input pin
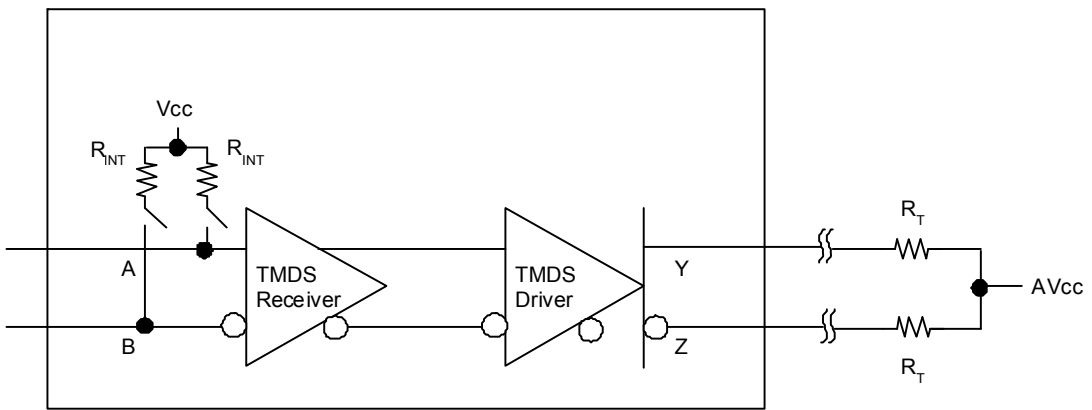   a. Unused inputs of TMDS recommend to OPEN

Fig 13   TMDS Input Recommendation

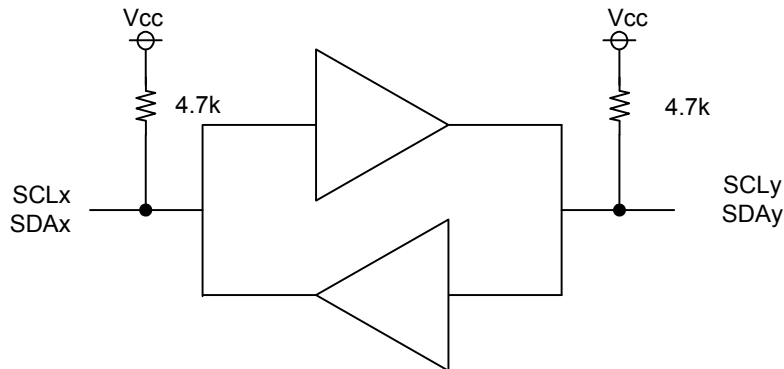   b. Unused inputs of DDC recommend to pull up.

Fig 14 Unused DDC Buffers of R side

   c. Unused input of HPD recommends to open

3) Serial connection of TMDS differential line

The serial connections of TMDS differential line like fig15 decrease the jitter tolerant characteristic. Especially when system needs 1080p (12bit) data rate, deterioration of Jitter tolerance is outstanding. This problem also depends on receiver IC characteristic. When 1080p (12bit) is required , Rohm doesn't recommend cascade connect application.
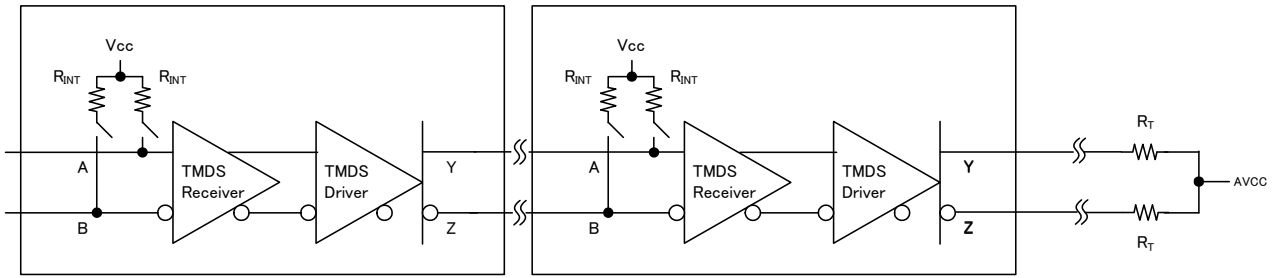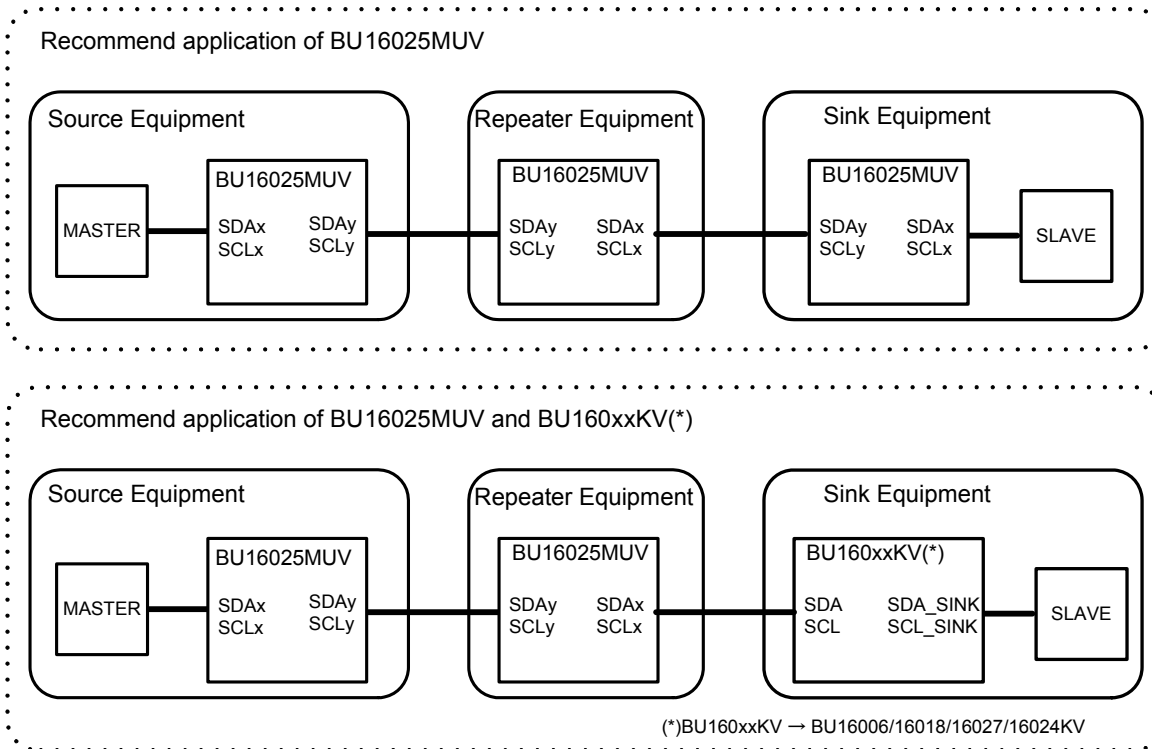

Fig 15   cascade connection notice

4) DDC line connections

DDC buffer of SDA x /SCLx and SDAy/SCLy have different low threshold level. Connect like below

Fig 16   DDC connection notice

5) AC Coupling

This IC can also communicate using AC coupling capacitor with TMDS line. But even connecting AC coupling capacitor, AC current may flow if input common mode voltage between two devices is different. This AC current may damage the lower common mode voltage devices like PCIe or DisplayPort.

6) TMDS output offset voltage

Offset voltage may appear to TMDS output when there is no signal to TMDS input differential line. OE should be set to "H" to avoid it.
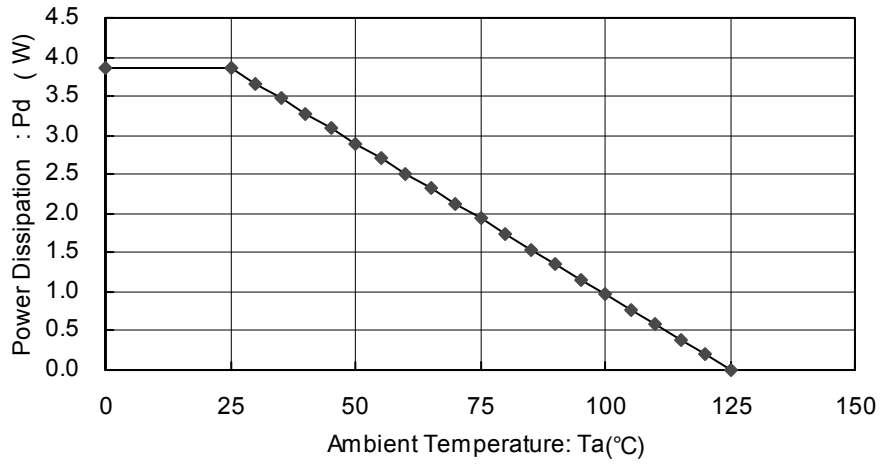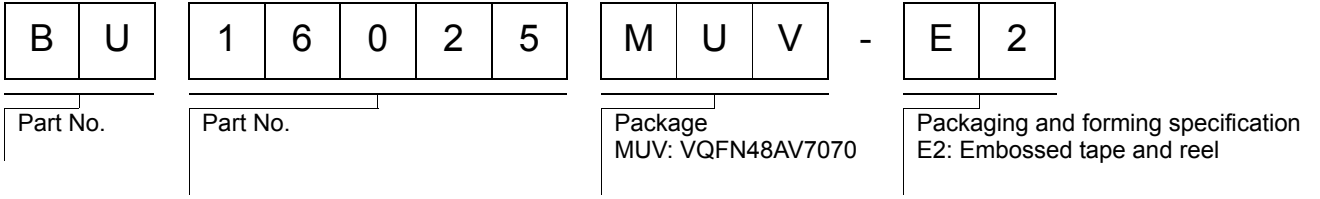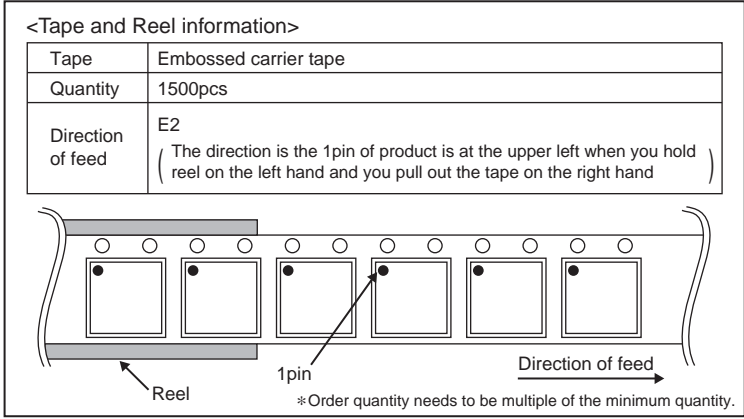
●Thermal Derating Curve

Rohm standard 4layer board

Fig.17   Thermal Derating Curve

●Ordering part number

| B | U | | 1 | 6 | 0 | 2 | 5 | | M | U | V | - | E | 2 |

Part No.   Part No.

Package
MUV: VQFN48AV7070

Packaging and forming specification
E2: Embossed tape and reel

VQFN048AV7070

7.0±0.1

7.0±0.1

1PIN MARK

1.0MAX

0.08 S

C0.2

4.7±0.1

48 1 12

4.7±0.1

37 13

0.4±0.1

36 25

24

0.75 0.5 0.25 +0.05 −0.04

0.02 +0.03 −0.02 (0.22)

(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel

1pin

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

Notes

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