

HDMI Switch ICs

3 for input 1 output switch with Termination sense correspondence (Sync with HPD_SINK)



BU16018KV

No.09063EDT02

●Description

BU16018KV is 3 for input 1 output HDMI/DVI switch LSI. Each port supports 2.25Gbps. (HDMI 1.3a).

This device control is simple. It requires only 3.3V source and a few GPIO controls.

Terminated resistors(50Ω) are integrated at each input port. When channel is not selected, termination resistors are turned off. TMDS inputs are high impedance.

This device is integrated equalization function and DDC buffer function, so It can adapt long cable.

●Features

- 1) Supports 2.25 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolution to 12-bit color depth
- 2) Compatible with HDMI 1.3a
- 3) Each port supports HDMI or DVI inputs
- 4) 5V tolerance to all DDC and HPD_SINK inputs
- 5) Integrated DDC buffer
- 6) Integrated switchable 50Ω receiver termination
- 7) Integrated equalizer circuit to adapt long cable
- 8) High impedance outputs when disabled
- 9) HBM ESD Protection exceeds 10kV
- 10) 3.3V supply operation
- 11) VQFP80 package
- 12) ROHS compatible

●Applications

Digital TV, DVD Player, Set-Top-Box, Audio Video Receiver, Digital Projector, DVI or HDMI Switch Box

●Line up matrix

Part No.	Power Supply (V)	ESD (KV)	Input (ch)	Output (ch)	Data rate (Gbps)	Hot Plug Control	Termination Sense Correspondence	Switching Method	DDC Buffer	Equalizer	De emphasis	Package	RoHS
BU16020KV	3 to 3.6	10	HDMI 4ch	HDMI 1ch	2.7	Yes	Yes	GPIO/I ² C	Yes	Yes (adaptive)	Yes	VQFP100	Yes
BU16018KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes	VQFP80	Yes
BU16027KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16006KV	3 to 3.6	10	HDMI 2ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16024KV	3 to 3.6	10	HDMI 1ch	HDMI 1ch	2.25	Yes	Yes	-	Yes	Yes	Yes	VQFP48C	Yes

●BLOCK DIAGRAM

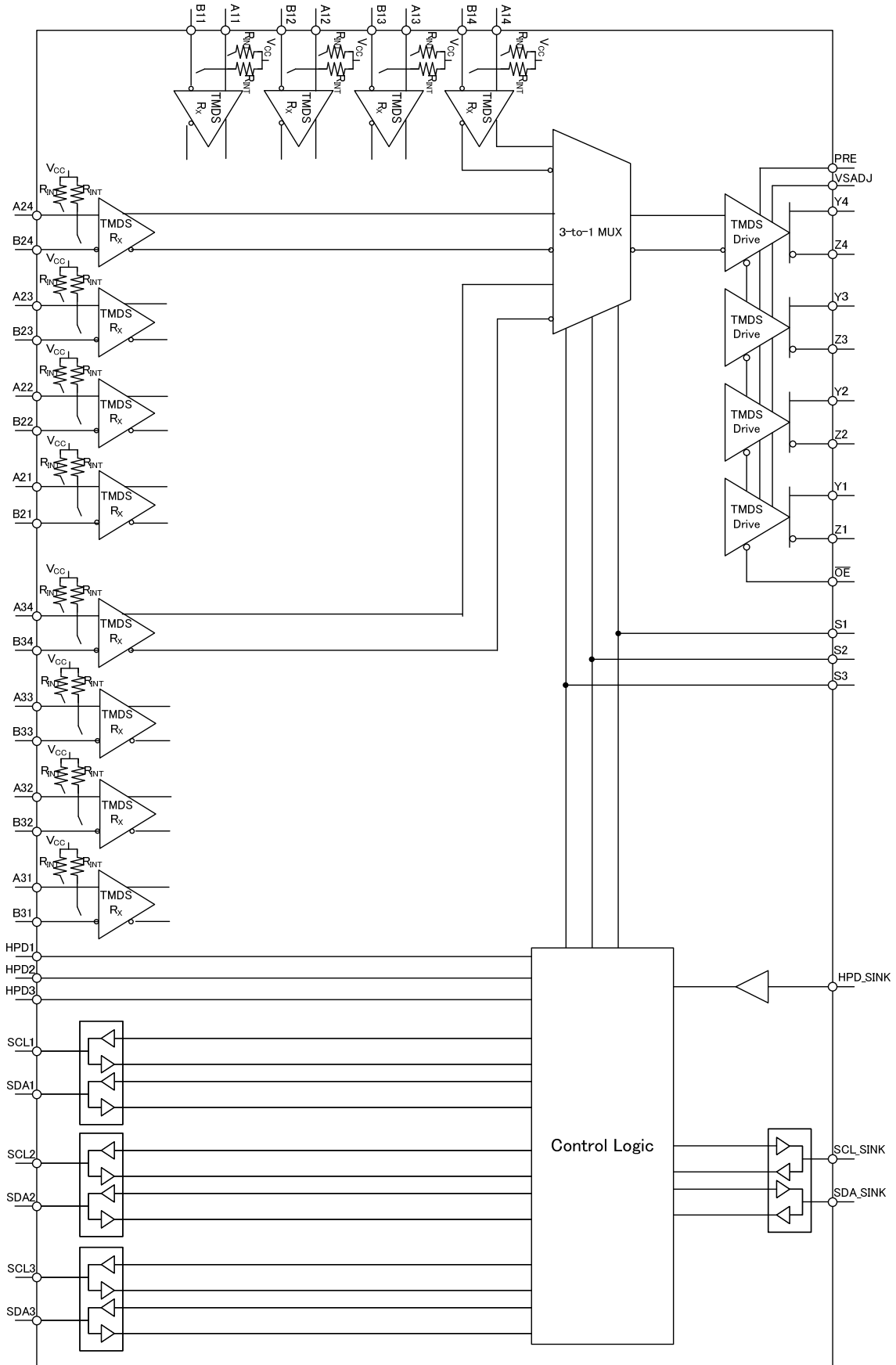


Figure 2-1 Block Diagram

● PIN EXPLANATION

1). PIN ASSIGNMENT

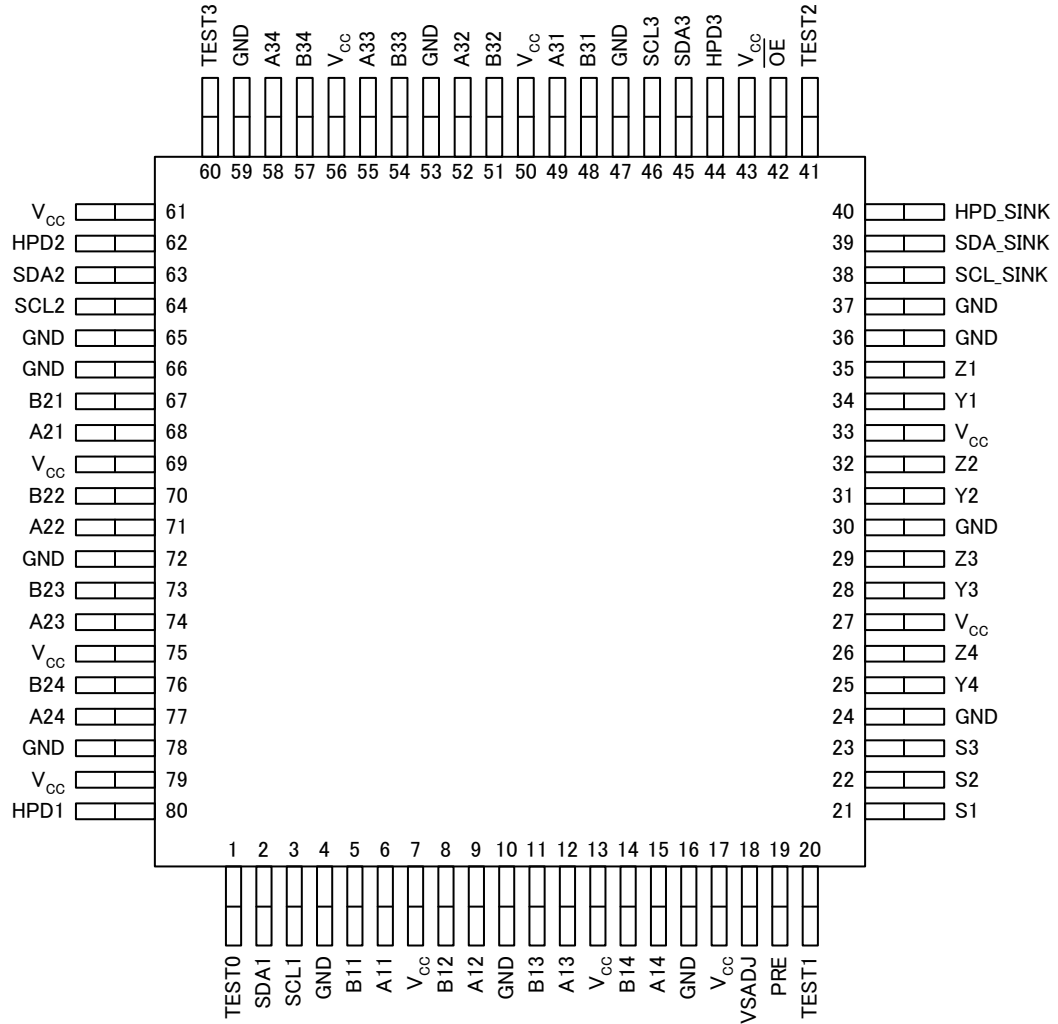


Figure 3-1 Pin Location

2). PIN LIST

TERMINAL		I/O	DESCRIPTION
NAME	No.		
A11, A12, A13, A14	6, 9, 12, 15	I	Port 1 TMDS positive inputs
A21, A22, A23, A24	68, 71, 74, 77	I	Port 2 TMDS positive inputs
A31, A32, A33, A34	49, 52, 55, 58	I	Port 3 TMDS positive inputs
B11, B12, B13, B14	5, 8, 11, 14	I	Port 1 TMDS negative inputs
B21, B22, B23, B24	67, 70, 73, 76	I	Port 2 TMDS negative inputs
B31, B32, B33, B34	48, 51, 54, 57	I	Port 3 TMDS negative inputs
GND	4, 10, 16, 24, 30, 36, 37, 47, 53, 59, 65, 66, 72, 78		Ground
HPD1	80	O	Port 1 hot plug detector output
HPD2	62	O	Port 2 hot plug detector output
HPD3	44	O	Port 3 hot plug detector output
HPD_SINK	40	I	Sink side hot plug detector input High : 5-V power signal asserted from source to sink and EDID is ready Low : No 5-V power signal asserted from source to sink or EDID is not ready
TEST0,1,2,3	1, 20, 41, 60		Open or GND connect (recommend)
OE	42	I	Output enable, active low
PRE	19	I	Output de-emphasis adjustment High : ON, Low : OFF
SCL1	3	I/O	Port 1 DDC bus clock line
SCL2	64	I/O	Port 2 DDC bus clock line
SCL3	46	I/O	Port 3 DDC bus clock line
SCL_SINK	38	I/O	Sink side DDC bus clock line
SDA1	2	I/O	Port 1 DDC bus data line
SDA2	63	I/O	Port 2 DDC bus data line
SDA3	45	I/O	Port 3 DDC bus data line
SDA_SINK	39	I/O	Sink side DDC bus data line
S1, S2, S3	21, 22, 23	I	Source selector input
V _{cc}	7, 13, 17, 27, 33, 43, 50, 56, 61, 69, 75, 79		Power supply
VSADJ	18	I	TMDS compliant voltage swing control. Connect to GND via 4.64KΩ
Y1, Y2, Y3, Y4	34, 31, 28, 25	O	TMDS positive outputs
Z1, Z2, Z3, Z4	35, 32, 29, 26	O	TMDS negative outputs

●EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

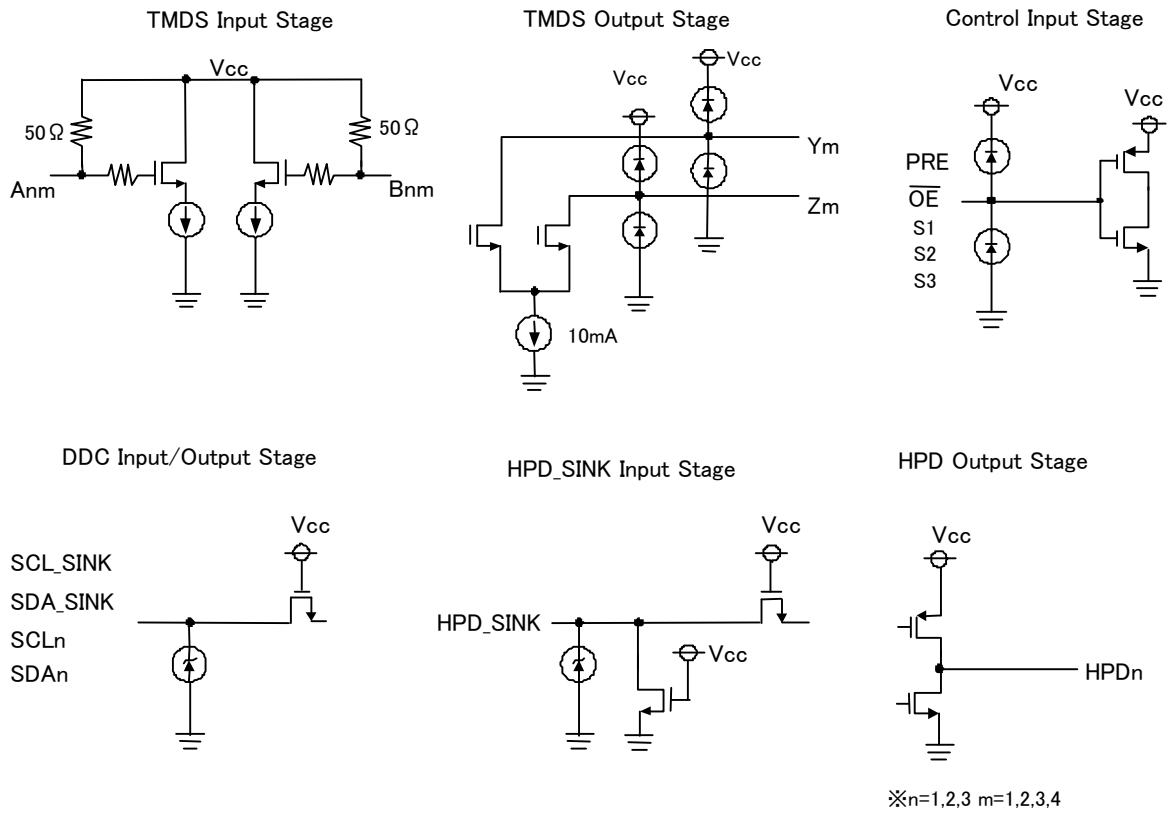


Figure 4-1 I/O pin schematic diagram

● SOURCE SELECTION LOOKUP TABLE

CONTROL PINS				I/O SELECTED	HOT PLUG DETECT STATUS			
HPD_SINK	S1	S2	S3	Y/Z	SCL_SINK SDA_SINK	HPD1	HPD2	HPD3
H	H	X	X	A1/B1 Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	H	L	L
H	L	H	X	A2/B2 Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	H	L
H	L	L	H	A3/B3 Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	H
H	L	L	L	None (Z) All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	H	H	H
L	H	X	X	Disallowed (indeterminate)State All terminations are disconnected	SCL1 SDA1	L	L	L
L	L	H	X	Disallowed (indeterminate)State All terminations are disconnected	SCL2 SDA2	L	L	L
L	L	L	H	Disallowed (indeterminate)State All terminations are disconnected	SCL3 SDA3	L	L	L
L	L	L	L	None (Z) All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	L	L	L

(1) H: Logic high; L: Logic low; X: Don't care; Z: High impedance

● ELECTRICAL SPECIFICATIONS

1.) ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

ITEM	MIN.	TYP.	MAX.	UNIT
Power supply voltage (V _{CC})	-0.3	-	4.0	V
DDC,HPD_SINK input voltage	-0.3	-	6.0	V
Differential input voltage	2.5	-	4.0	V
PRE, S1, S2, S3, OE input voltage	-0.3	-	4.0	V
Power dissipation	-	-	1200 ※1	mW
Storage temperature range	-55	-	125	°C

※70mm×70mm×1.6mm glass epoxy board mount. (Reverse Cu occupation rate: 15mm×15mm)

When it's used by than Ta=25°C, it's reduced by 12mW/°C.

2.) RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply voltage	3.0	3.3	3.6	V
T _A	Operating free-air temperature	0	-	70	°C
TMDS DIFFERENTIAL PINS (A/B)					
V _{ID}	Receiver peak-to-peak differential input voltage	150	-	1560	mVp-p
V _{IC}	Input common mode voltage	V _{CC} -0.6	-	V _{CC} +0.01	V
R _{V_SADJ}	Resistor for TMDS compliant voltage swing range	4.6	4.64	4.68	KΩ
A _{V_{CC}}	TMDS output termination voltage	3.0	3.3	3.6	V
R _T	Termination resistance	45	50	55	Ω
Signaling rate		0	-	2.25	Gbps
CONTROL PINS (S1,S2)					
V _{IH}	LVTTL High-level input voltage	2	-	V _{CC}	V
V _{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
STATUS(HPD_SINK)					
V _{IH}	LVTTL High-level input voltage	2.4	-	5.5	V
V _{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
DDC PINS (SCL_SINK, SDA_SINK, SDA[3:1], SCL[3:1])					
V _{I(DDC)}	Input voltage	GND	-	5.5	V

3.) ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
I _{CC}	Supply current	V _{IH} = V _{CC} , V _{IL} = V _{CC} -0.4V, R _{VSADJ} = 4.64kΩ R _T = 50Ω, AV _{CC} = 3.3V Anm/Bnm = 2.25Gbps HDMI data pattern n = 1 or 2 or 3, m = 2, 3, 4 An1/Bn1 = 225 MHz clock	-	120	150	mA
P _D	Power dissipation	V _{IH} = V _{CC} , V _{IL} = V _{CC} -0.4V, R _{VSADJ} = 4.64kΩ R _T = 50Ω, AV _{CC} = 3.3V Anm/Bnm = 2.25Gbps HDMI data pattern, n = 1 or 2 or 3, m = 2, 3, 4 An1/Bn1 = 225 MHz clock	-	450	600	mW
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V _{OH}	Single-ended high-level output voltage	AV _{CC} = 3.3V, R _T = 50Ω, PRE = 0V	AV _{CC} -10	-	AV _{CC} +10	mV
V _{OL}	Single-ended low-level output voltage		AV _{CC} -600	-	AV _{CC} -400	mV
V _{SWING}	Single-ended low-level swing voltage		400	-	600	mV
V _{OD(O)}	Overshoot of output differential voltage		-	6%	15%	2xV _{swing}
V _{OD(U)}	Undershoot of output differential voltage		-	12%	25%	2xV _{swing}
V _{ODE(SS)}	Steady state output differential voltage with de-emphasis	PRE = V _{CC} Anm/Bnm = 250 Mbps HDMI data pattern, n = 1 or 2 or 3, m = 2, 3, 4 An1/Bn1 = 25 MHz clock	600	-	920	mVp-p
R _{INT}	Input termination resistance	V _{IN} = 2.9V	45	50	55	Ω
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-	5	-	mV

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
DDC Input and output						
Tx : SCL_SINK , SDA_SINK						
$I_{IKT\ ①}$	Input leak current	$V_I = 5.5V$	-10	-	10	μA
$I_{IKT\ ②}$	Input leak current	$V_I = V_{CC}$	-10	-	10	μA
I_{OHT}	High-level output current	$V_O = 3.6V$	-10	-	10	μA
I_{ILT}	Low-level input current	$V_{IL} = GND$	-10	-	10	μA
V_{OLT}	Low-level output voltage	$RL = 4.7k\Omega$	0.43	0.5	0.57	V
$V_{OLT} - V_{IL}$	Low-level input voltage below output low-level voltage		20	100	190	mV
V_{OLT}	Low-level output voltage	$RL = 4.7k\Omega$	0.43	0.5	0.57	V
$V_{OLT} - V_{IL}$	Low-level input voltage below output low-level voltage		20	100	190	mV
Rx : SCLn , SDA n (n = 1, 2, 3)						
$I_{IKR\ ①}$	Input leak current	$V_I = 5.5V$	-10	-	10	μA
$I_{IKR\ ②}$	Input leak current	$V_I = V_{CC}$	-10	-	10	μA
I_{OHR}	High-level output current	$V_O = 3.6V$	-10	-	10	μA
I_{ILR}	Low-level input current	$V_{IL} = GND$	-10	-	10	μA
V_{OLR}	Low-level output voltage	$I_{OUT} = 4mA$	-	-	0.2	V
CONTROL PINS (PRE, S1, S2, S3, OE)						
I_{IH}	High-level digital input current	$V_{IH} = V_{CC}$	-10	-	10	μA
I_{IL}	Low-level digital input current	$V_{IL} = GND$	-10	-	10	μA
STATUS PINS (HPD_SINK)						
I_{IH}	High-level digital input current	$V_{IH} = 5.5V$	10	50	100	μA
		$V_{IH} = V_{CC}$	5	30	80	μA
I_{IL}	Low-level digital input current	$V_{IL} = GND$	-10	-	10	μA
STATUS PINS (HPD1, 2, 3)						
$V_{OH(TTL)}$	TTL High-level output voltage	$I_{OH} = -8mA$	2.4	-	V_{CC}	V
$V_{OL(TTL)}$	TTL Low-level output voltage	$I_{OL} = 8mA$	0	-	0.4	V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
TMDS DIFFERENTIAL PINS (Y/Z)						
t _{PLH}	Propagation delay time low-high-level output	See Figure 5-2, AV _{CC} = 3.3V, R _T = 50 Ω, PRE=0V	-	480	-	ps
t _{PHL}	Propagation delay time high-low level output		-	500	-	ps
t _r	Differential output signal rise time (20%-80%)		-	160	-	ps
t _f	Differential output signal fall time (20%-80%)		-	160	-	ps
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})		-	20	-	ps
t _{sk(D)}	Intra-pair differential skew, see Figure 5-3.		-	35	-	ps
t _{sk(o)}	Inter-pair channel-to-channel output skew ⁽²⁾		-	50	-	ps
t _{sk(pp)}	Part to part skew ⁽³⁾		-	400	-	ps
t _{sx}	Select to switch output		-	8	-	ns
t _{dis}	Disable time		-	5	-	ns
t _{en}	Enable time	-	7	-	ns	
DDC I/O PINS (SCL_n, SCL_SINK, SDA_n, SDA_SINK) (n = 1, 2, 3)						
t _{pdLHTR(DDC)}	Propagation delay time, low-to-high-level output Tx to Rx	R _L = 4.7KΩ C _L = 100pF	-	650	-	ns
t _{pdHLTR(DDC)}	Propagation delay time, high-to-low-level output Tx to Rx		-	200	-	ns
t _{pdLHRT(DDC)}	Propagation delay time, low-to-high-level output Rx to Tx	R _L = 1.67KΩ C _L = 400pF	-	500	-	ns
t _{pdHLRT(DDC)}	Propagation delay time, high-to-low-level output Rx to Tx		-	350	-	ns
t _{r TX(DDC)}	Tx output Rise time	R _L = 4.7KΩ C _L = 100pF	-	800	-	ns
t _{f TX(DDC)}	Tx output Fall time		-	150	-	ns
t _{r RX(DDC)}	Rx output Rise time	R _L = 1.67KΩ C _L = 400pF	-	950	-	ns
t _{f RX(DDC)}	Rx output Fall time		-	50	-	ns
t _{sx(DDC)}	Switch time from SCL _n to SCL_SINK	C _L =10pF	-	800	-	ns
C _{IO}	Input/output capacitance	V _I =0V		15		pF

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
STATUS PINS(HPD1, 2, 3)						
$t_{pdLH(HPD)}$	Propagation delay time, low-to-high-level output from HPD_SINK to HPDn(n=1,2,3)	$C_L=10pF$	-	5	-	ns
$t_{pdHL(HPD)}$	Propagation delay time, high-to-low-level output from HPD_SINK to HPDn(n=1,2,3)	$C_L=10pF$	-	5	-	ns
$t_{sx(HPD)}$	Switch time from port select to the latest valid status of HPD	$C_L=10pF$	-	8	-	ns

Note:

1. All typical values are at 25°C and with a 3.3V supply.
2. $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel of a devices when inputs are tied together.
3. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel two devices, or between channel 1 of two devices, when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.

● MEASUREMENT SYMBOL AND CIRCUIT

PARAMETER MEASUREMENT INFORMATION

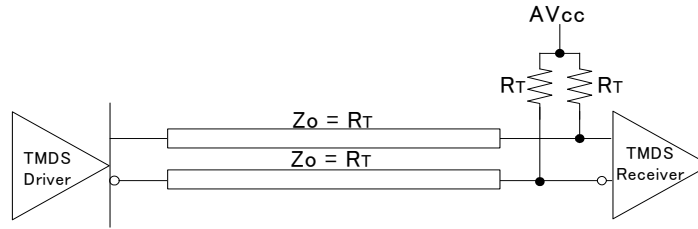


Figure 5-1 Termination for TMSD Output Driver

PARAMETER MEASUREMENT INFORMATION (continued)

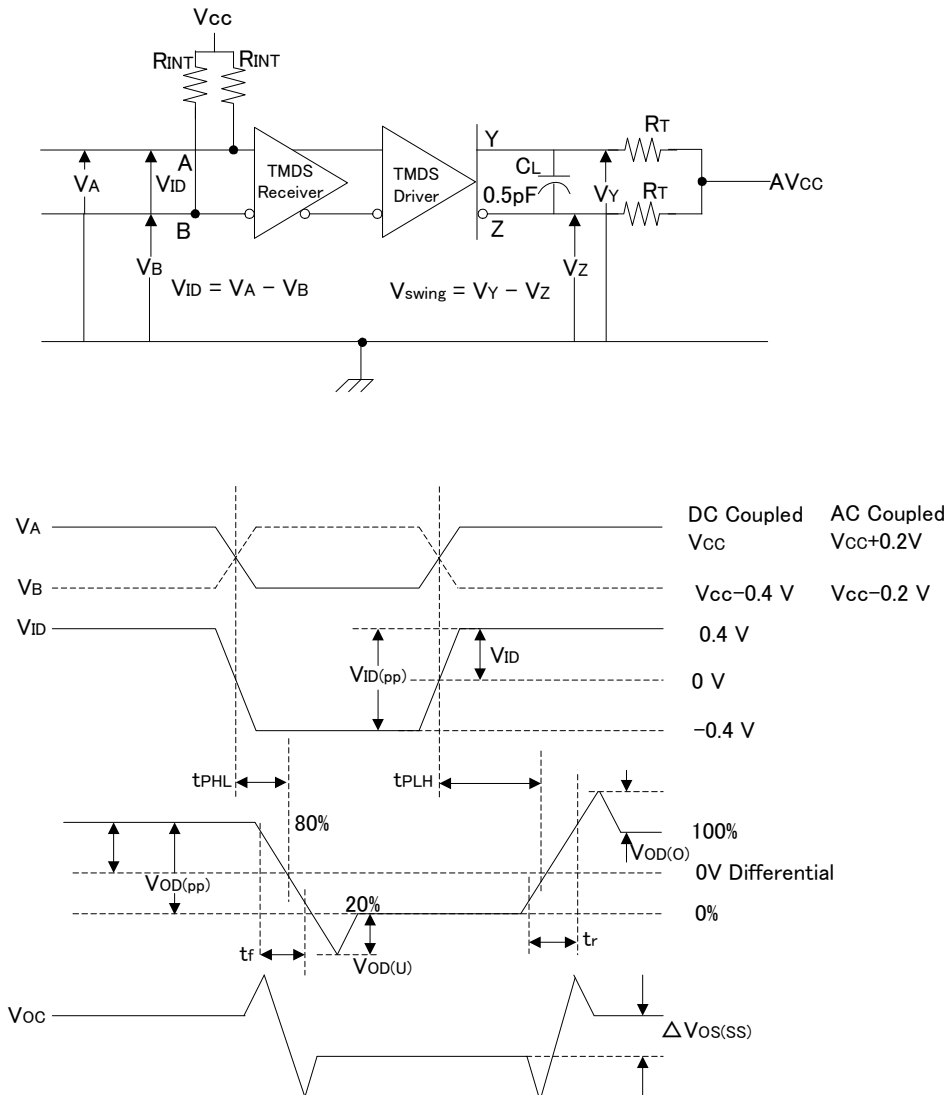


Figure 5-2 Timing Test Circuit and Definitions

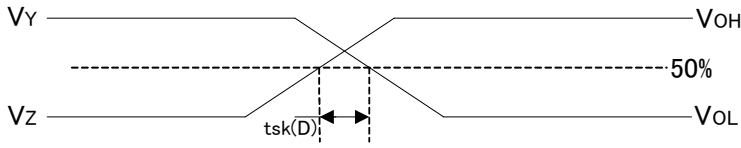


Figure 5-3 Definition of Intra-Pair Differential Skew

PARAMETER MEASUREMENT INFORMATION (continued)

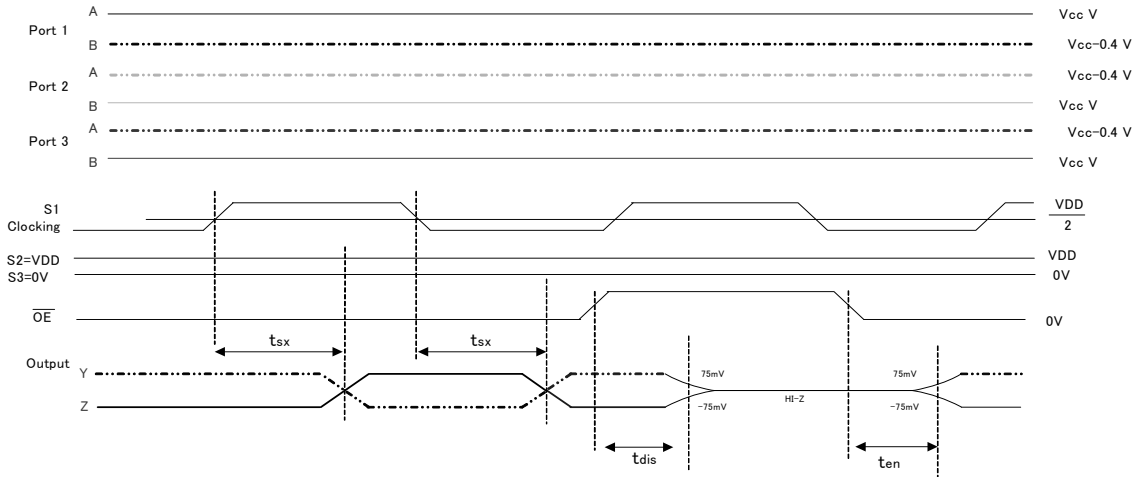


Figure 5-4 TMDs Outputs Control Timing Definitions

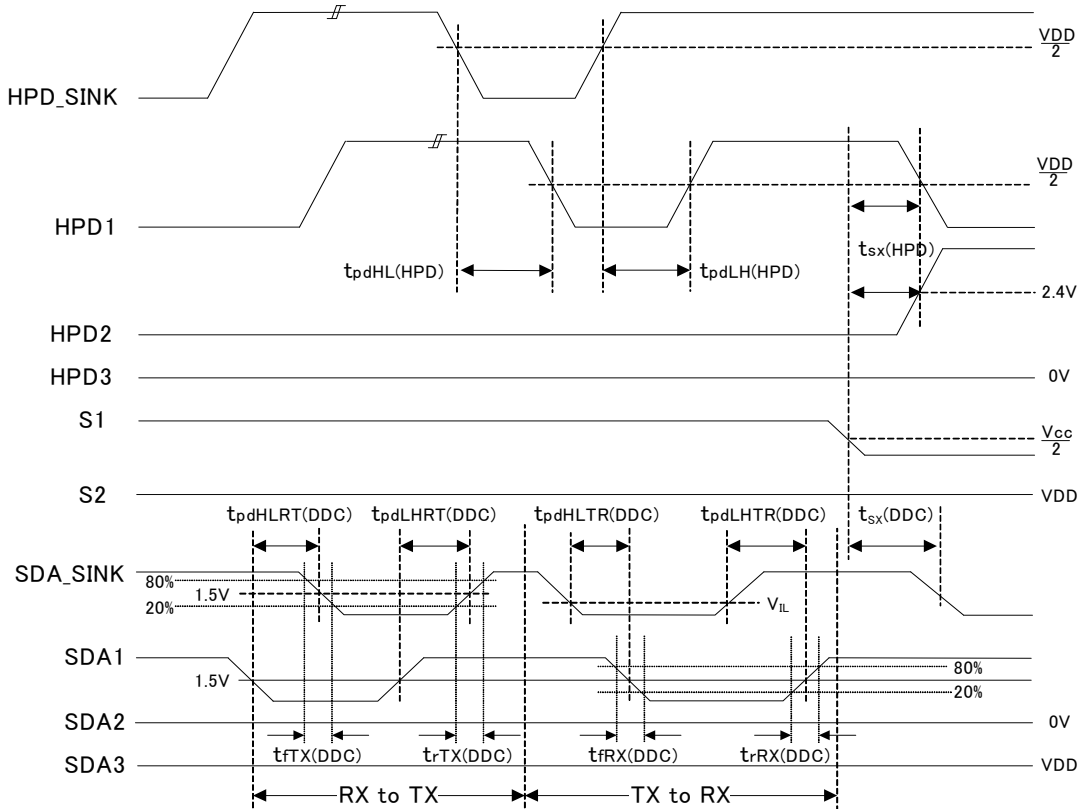


Figure 5-5 DDC and HPD Timing Definitions

1). Y and Z terminal ESD diode notice.

Y and Z terminals are connected ESD diode.

When $VCC + 0.4 < AVCC$.

BU16018KV flow leak current from AVCC to VCC.

In order to pass the compliance test.

You must use mandatory application, refer Figure 6-1 for "Repeater" or "output Buffer" application.

If you use "Repeater" or "output Buffer"

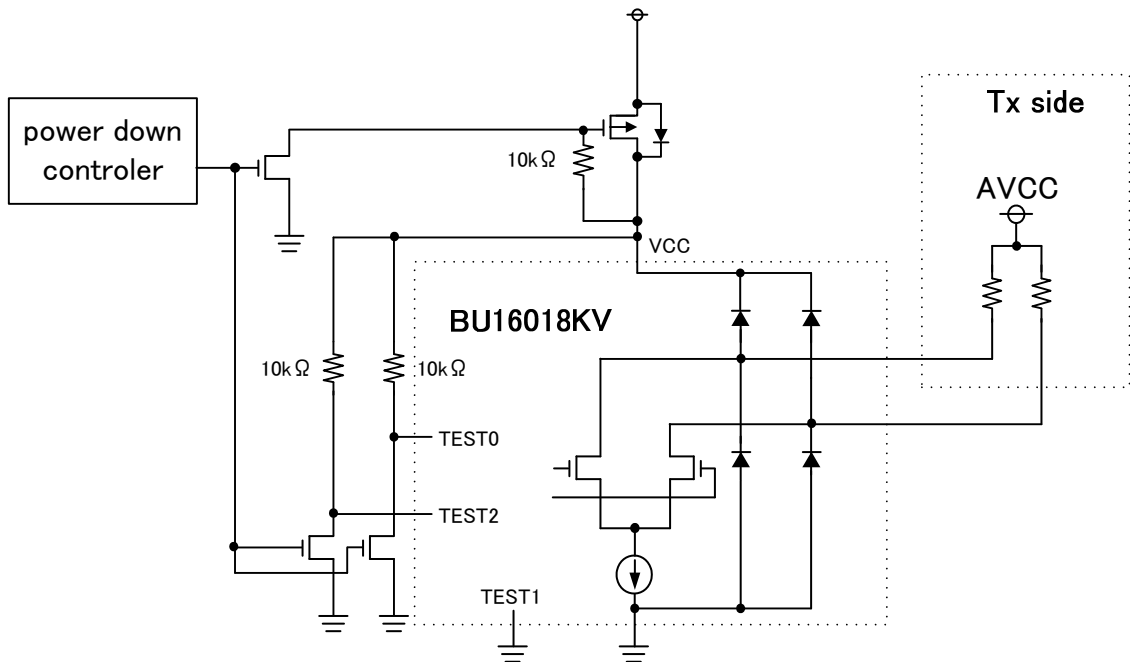


Figure 6-1 Leak current control

2). HPD_SINK Pull down resistance.

HPD_SINK is a 5V tolerant structure shown in Figure 6-2.

It needs some drive current to pull down HPD_SINK "H" to "L"(max10uA@HPD_SINK=2V).

So to pull down HPD_SINK, please use 10kΩ(or under 10kΩ) resistor.

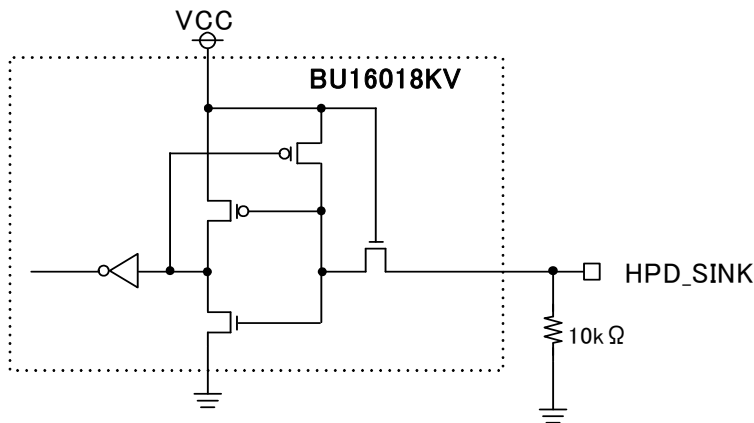


Figure 6-2 HPD_SINK I/O schematic

3). About don't use terminal.
 Unused TMD5 input channel can be opened.

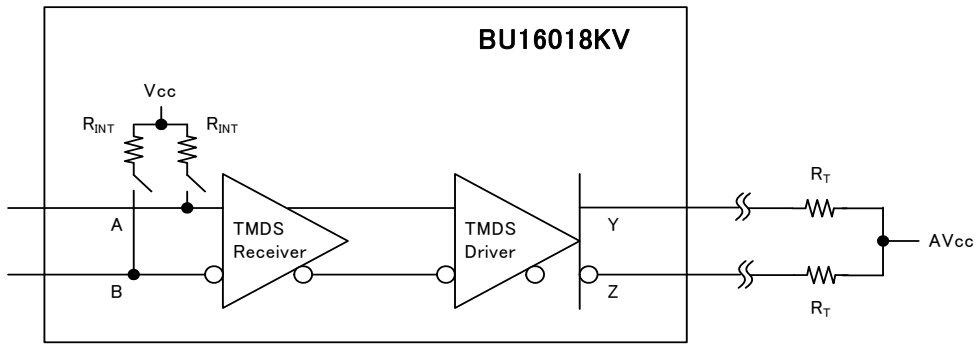


Figure 6-3 TMD5 Input Fail-Safe Recommendation

Unused DDC Buffers of R side pulled up to Vdd

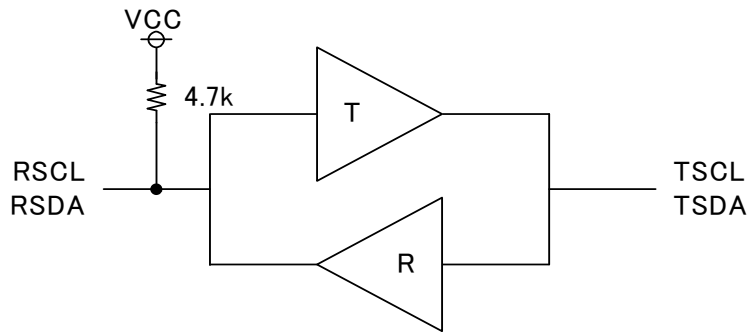


Figure 6-4 DDC Buffers in BU16018KV

Open unused HPDn.

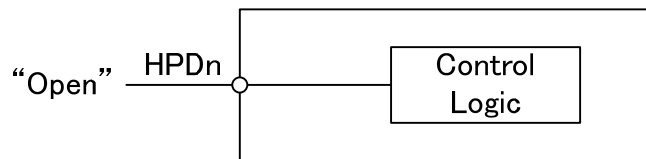


Figure 6-5 Open unused HPDn

4). About serial connect notice.

When HDMI sw output connect to other HDMI sw input like following application.

There is possibility that. 1080p(12bit) image isn't displayed. It's depend on receiver IC characteristic.
 When system is required 1080p (12bit), Rohm doesn't recommend serial connect application.

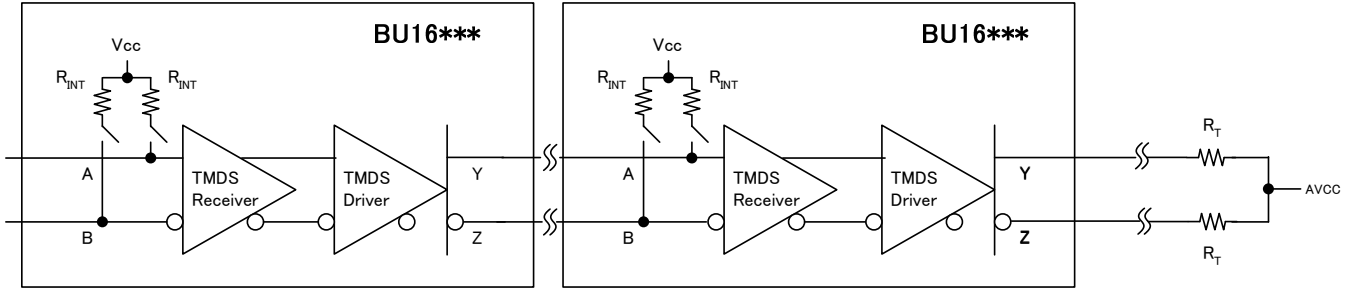


Figure 6-6 serial connect notice

5). Offset voltage appearance.

If differential input is opened, offset voltage appear at differential output OE is set to low to avoid it.

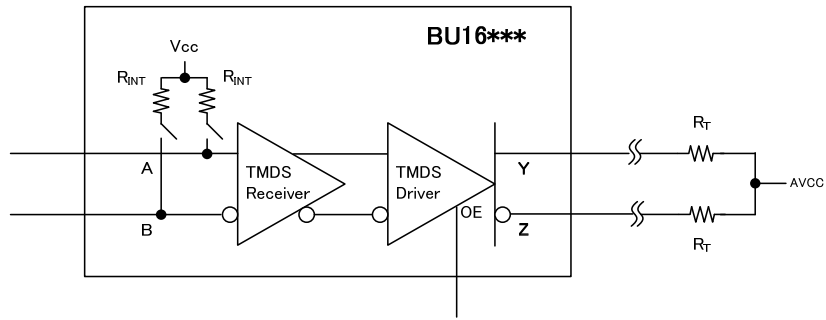


Figure 6-7 Offset voltage avoid

6). Limitation of Master and slave direction.

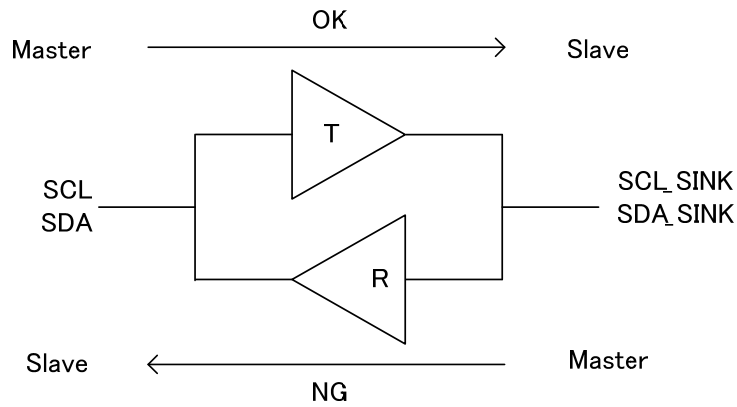


Figure 6-8 Limitation of Master and slave direction

● Ordering part number



ROHM model name



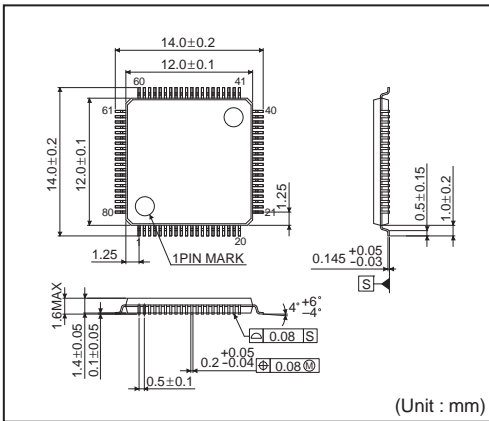
Package type
VQFP80



Packaging and forming specification
E2 =Reel-shaped emboss taping

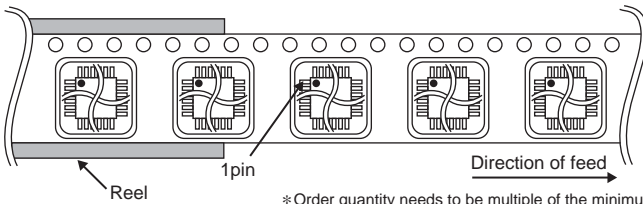
● Package specification

VQFP80



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold) reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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