NEC

MOS INTEGRATED CIRCUIT

μPD77113A, 77114

16-BIT FIXED-POINT DIGITAL SIGNAL PROCESSORS

DESCRIPTION

The μPD77113A and 77114 are 16-bit fixed-point digital signal processors (DSPs).

Compared with the μPD77016 family, these DSPs have improved power consumption and are ideal for battery-powered mobile terminals such as PDAs and cellular phones.

Both mask ROM and RAM models are available.

For details of the functions of these DSPs, refer to the following User's Manuals:

μPD77111 Family User's Manual : U14623E
μPD77016 Family User's Manual - Instructions : U13116E

FEATURES

- Instruction cycle (operating clock)
  μPD77113A : 13.3 ns MIN (75 MHz MAX)
  μPD77114 : 13.3 ns MIN (75 MHz MAX)
- Memory
- Internal instruction memory
  μPD77113A : RAM 3.5K words × 32 bits
  Mask ROM 48K words × 32 bits
  μPD77114 : RAM 3.5K words × 32 bits
  Mask ROM 48K words × 32 bits
- Data memory
  μPD77113A : RAM 16K words × 16 bits × 2 banks
  Mask ROM 32K words × 16 bits × 2 banks
  μPD77114 : RAM 16K words × 16 bits × 2 banks
  Mask ROM 32K words × 16 bits × 2 banks
  External memory space 8K words × 16 bits × 2 banks

ORDERING INFORMATION

	Part Number	Package
★	μPD77113AF1-xxx-CN1	80-pin plastic fine-pitch BGA (9 × 9)
	μPD77114GC-xxx-9EU	100-pin plastic TQFP (fine pitch) (14 × 14)

Remark xxx indicates ROM code suffix.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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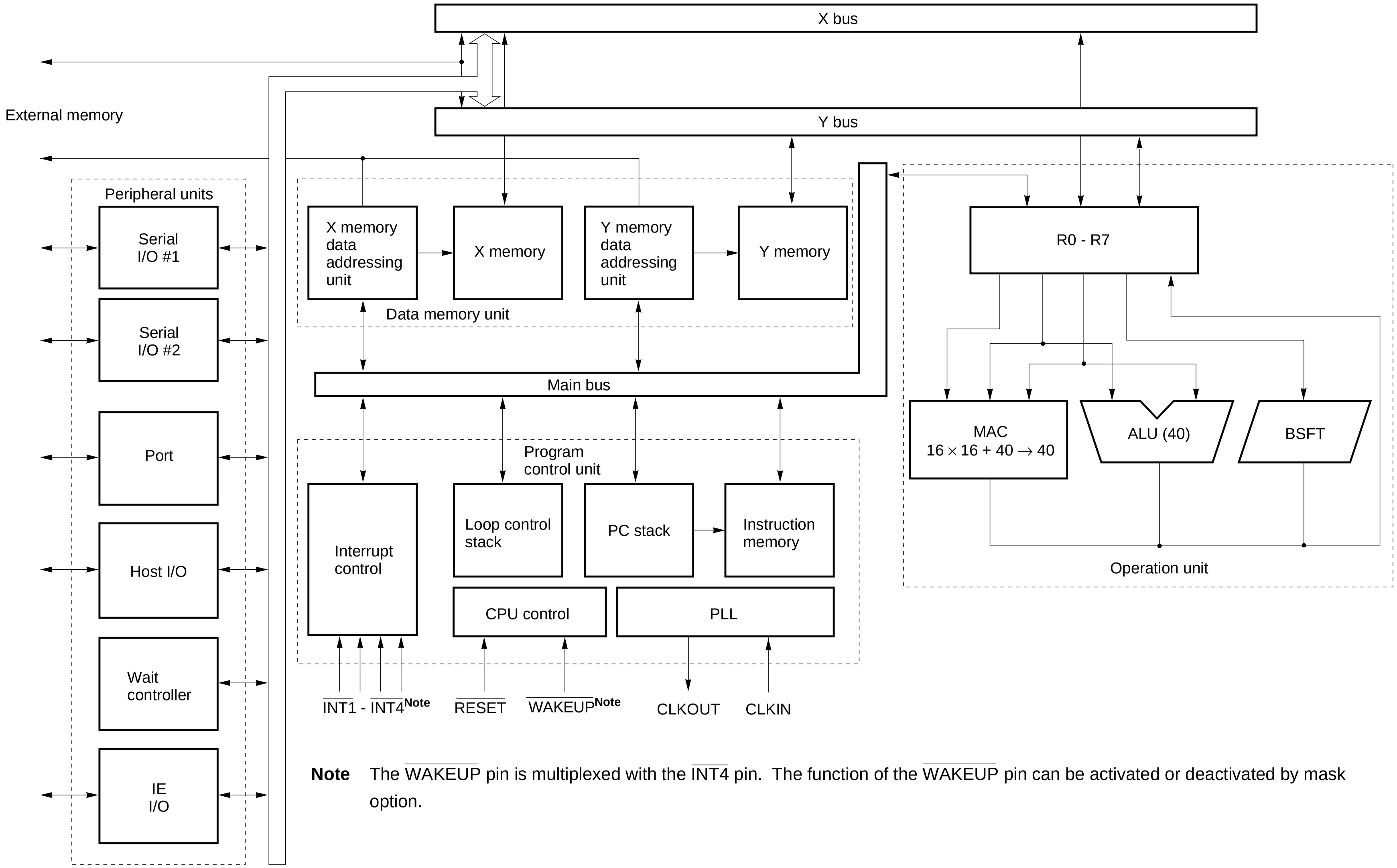
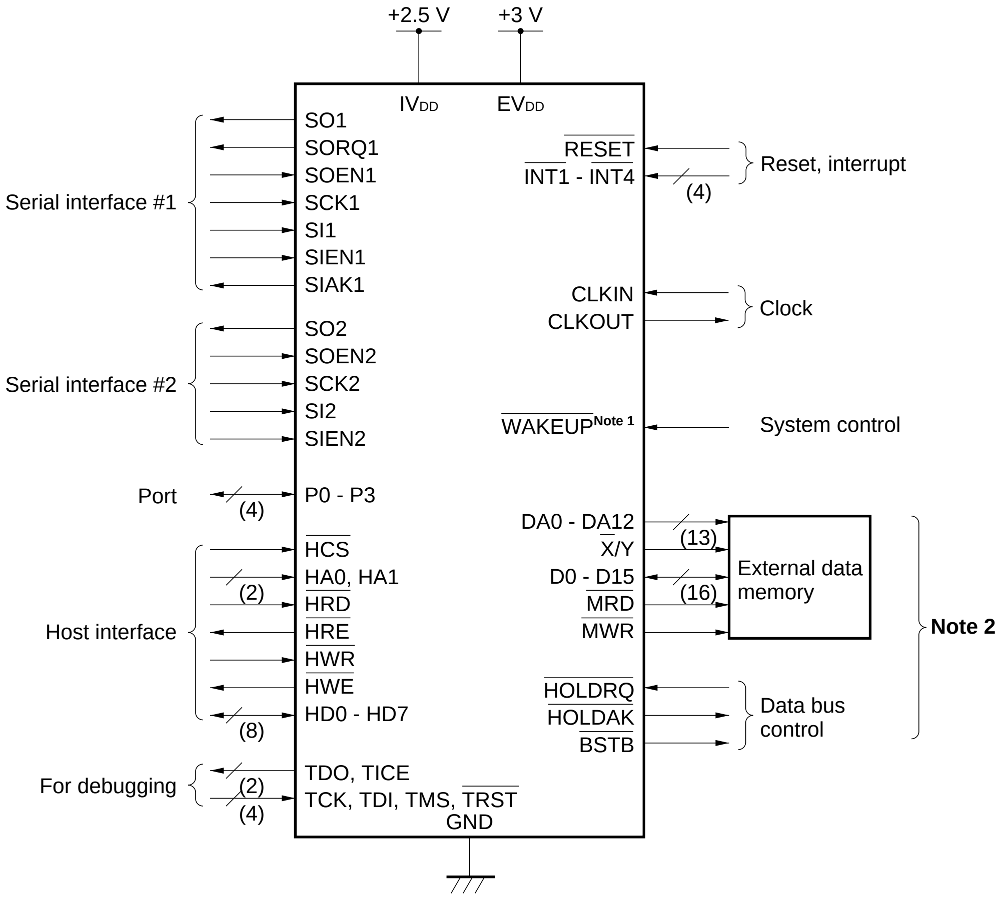
The mark ★ shows major revised points.

BLOCK DIAGRAM



Note The $\overline{\text{WAKEUP}}$ pin is multiplexed with the $\overline{\text{INT4}}$ pin. The function of the $\overline{\text{WAKEUP}}$ pin can be activated or deactivated by mask option.

PIN CONFIGURATION



Notes 1. The function of this pin can be activated or deactivated by mask option.

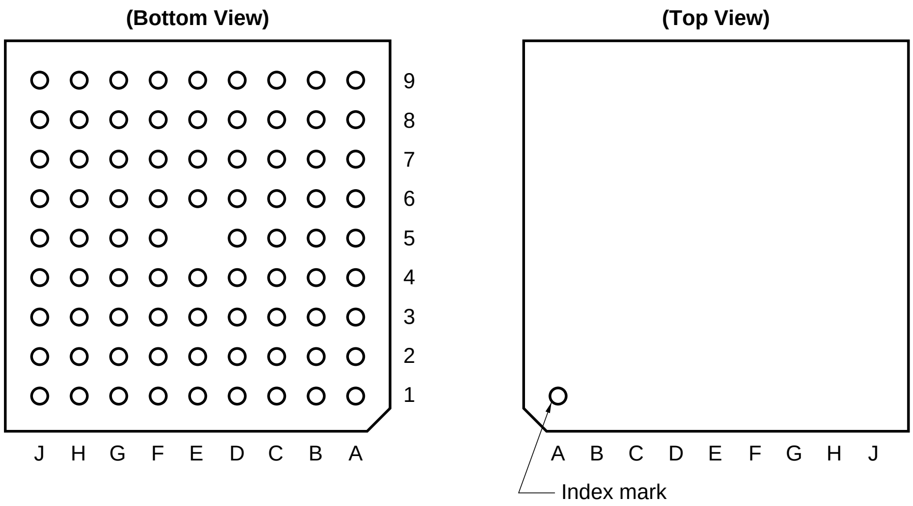
2. An external data memory interface is not provided on the μPD77113A.

★ DSP FUNCTION LIST

<table>
<tr><th colspan="2">Item</th><th>μPD77016</th><th>μPD77018A</th><th>μPD77019</th><th>μPD77019-013</th><th>μPD77110</th><th>μPD77111</th><th>μPD77112</th><th>μPD77113A</th><th>μPD77114</th></tr>
<tr><td rowspan="6">Memory space (words × bits)</td><td>Internal instruction RAM</td><td>1.5K × 32</td><td>256 × 32</td><td colspan="2">4K × 32</td><td>35.5K × 32</td><td colspan="2">1K × 32</td><td colspan="2">3.5K × 32</td></tr>
<tr><td>Internal instruction ROM</td><td>None</td><td colspan="2">24K × 32</td><td colspan="2">None</td><td colspan="2">31.75K × 32</td><td colspan="2">48K × 32</td></tr>
<tr><td>Data RAM (X/Y memory)</td><td>2K × 16 each</td><td colspan="3">3K × 16 each</td><td>24K × 16 each</td><td colspan="2">3K × 16 each</td><td colspan="2">16K × 16 each</td></tr>
<tr><td>Data ROM (X/Y memory)</td><td>None</td><td colspan="2">12K × 16 each</td><td colspan="2">None</td><td colspan="2">16K × 16 each</td><td colspan="2">32K × 16 each</td></tr>
<tr><td>External instruction memory</td><td>48K × 32</td><td colspan="8">None</td></tr>
<tr><td>External data memory (X/Y memory)</td><td>48K × 16 each</td><td colspan="3">16K × 16 each</td><td>32K × 16 each</td><td>None</td><td>16K × 16 each</td><td>None</td><td>8K × 16 each</td></tr>
<tr><td colspan="2">Instruction cycle (at maximum speed)</td><td>30 ns (33 MHz)</td><td colspan="3">16.6 ns (60 MHz)</td><td>15.3 ns (65 MHz)</td><td colspan="4">13.3 ns (75 MHz)</td></tr>
<tr><td colspan="2">Multiple</td><td>–</td><td colspan="2">×1, 2, 3, 4, 8 (mask option)</td><td>Fixed to ×4</td><td>Integer of ×1 to 8 (external pin)</td><td colspan="4">Integer of ×1 to 16 (mask option)</td></tr>
<tr><td colspan="2">Serial interface (two channels)</td><td>Channels 1 and 2 have same function.</td><td colspan="8">Channel 1 has same function as μPD77016. Channel 2 does not have SORQ2 and SIAK2 pins (for connection of codec).</td></tr>
<tr><td colspan="2">Supply voltage</td><td>5 V</td><td colspan="3">3 V</td><td colspan="5">DSP core: 2.5 V
I/O pins : 3 V</td></tr>
<tr><td colspan="2">Package</td><td>160-pin QFP</td><td>100-pin TQFP
116-pin BGA</td><td colspan="3">100-pin TQFP</td><td>80-pin TQFP
80-pin FBGA</td><td>100-pin TQFP</td><td>80-pin FBGA</td><td>100-pin TQFP</td></tr>
</table>

PIN CONFIGURATION

80-pin plastic fine-pitch BGA (9 × 9)
μPD77113AF1-xxx-CN1

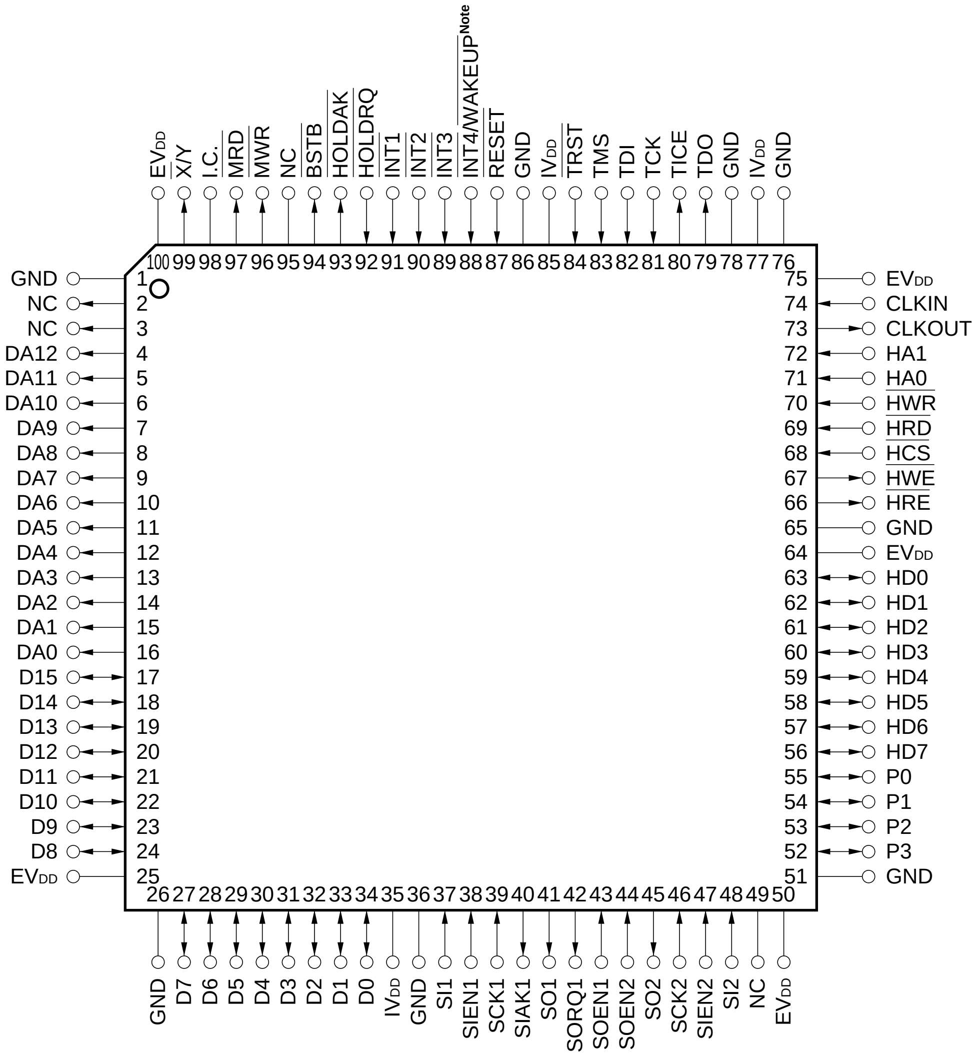


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	–	C3	NU	E6	$\overline{\text{HCS}}$	G8	P1
A2	NU	C4	$\overline{\text{RESET}}$	E7	GND	G9	GND
A3	EV_{DD}	C5	TDI	E8	HD1	H1	NU
A4	$\overline{\text{INT3}}$	C6	TDO	E9	HD2	H2	NU
A5	GND	C7	CLKIN	F1	NU	H3	SCK1
A6	TMS	C8	HA0	F2	NU	H4	SOEN2
A7	GND	C9	EV_{DD}	F3	SOEN1	H5	SIEN2
A8	$\overline{\text{TRST}}$	D1	EV_{DD}	F4	GND	H6	P3
A9	–	D2	NU	F5	HD0	H7	P0
B1	NU	D3	$\overline{\text{INT2}}$	F6	SI2	H8	HD7
B2	NU	D4	NU	F7	HD3	H9	NU
B3	$\overline{\text{INT1}}$	D5	TCK	F8	HD6	J1	–
B4	$\overline{\text{INT4}}$/$\overline{\text{WAKEUP}}$ Note	D6	GND	F9	HD5	J2	NU
B5	IV_{DD}	D7	$\overline{\text{HWR}}$	G1	EV_{DD}	J3	SI1
B6	TICE	D8	$\overline{\text{HRD}}$	G2	GND	J4	SORQ1
B7	IV_{DD}	D9	EV_{DD}	G3	SIEN1	J5	SO2
B8	HA1	E1	NU	G4	SO1	J6	SCK2
B9	CLKOUT	E2	GND	G5	IV_{DD}	J7	EV_{DD}
C1	GND	E3	SIAK1	G6	HD4	J8	NU
C2	NU	E4	NU	G7	P2	J9	–

Note The function of the $\overline{\text{WAKEUP}}$ pin can be activated or deactivated by a mask option.

100-pin plastic TQFP (fine-pitch) (14 × 14) (Top View)

μPD77114GC-xxx-9EU



Note The functions can be activated or deactivated by a mask option.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	26	GND	51	GND	76	GND
2	NC	27	D7	52	P3	77	IV_{DD}
3	NC	28	D6	53	P2	78	GND
4	DA12	29	D5	54	P1	79	TDO
5	DA11	30	D4	55	P0	80	TICE
6	DA10	31	D3	56	HD7	81	TCK
7	DA9	32	D2	57	HD6	82	TD1
8	DA8	33	D1	58	HD5	83	TMS
9	DA7	34	D0	59	HD4	84	$\overline{\text{TRST}}$
10	DA6	35	IV_{DD}	60	HD3	85	IV_{DD}
11	DA5	36	GND	61	HD2	86	GND
12	DA4	37	SI1	62	HD1	87	$\overline{\text{RESET}}$
13	DA3	38	SIEN1	63	HD0	88	$\overline{\text{INT4}}$/$\overline{\text{WAKEUP}}$[Note]
14	DA2	39	SCK1	64	EV_{DD}	89	$\overline{\text{INT3}}$
15	DA1	40	SIAK1	65	GND	90	$\overline{\text{INT2}}$
16	DA0	41	SO1	66	$\overline{\text{HRE}}$	91	$\overline{\text{INT1}}$
17	D15	42	SORQ1	67	$\overline{\text{HWE}}$	92	$\overline{\text{HOLDRQ}}$
18	D14	43	SOEN1	68	$\overline{\text{HCS}}$	93	$\overline{\text{HOLDAK}}$
19	D13	44	SOEN2	69	$\overline{\text{HRD}}$	94	$\overline{\text{BSTB}}$
20	D12	45	SO2	70	$\overline{\text{HWR}}$	95	NC
21	D11	46	SCK2	71	HA0	96	$\overline{\text{MWR}}$
22	D10	47	SIEN2	72	HA1	97	$\overline{\text{MRD}}$
23	D9	48	SI2	73	CLKOUT	98	I.C.
24	D8	49	NC	74	CLKIN	99	$\overline{\text{X}}$/Y
25	EV_{DD}	50	EV_{DD}	75	EV_{DD}	100	EV_{DD}

Note The function of the $\overline{\text{WAKEUP}}$ pin can be activated or deactivated by a mask option.

PIN NAME

$\overline{\text{BSTB}}$	: Bus Strobe
CLKIN	: Clock Input
CLKOUT	: Clock Output
D0 - D15	: 16-bit Data Bus
DA0 - DA12	: External Data Memory Address Bus
EV_{DD}	: Power Supply for I/O Pins
GND	: Ground
HA0, HA1	: Host Data Access
$\overline{\text{HCS}}$	: Host Chip Select
HD0 - HD7	: Host Data Bus
$\overline{\text{HOLDAK}}$	: Hold Acknowledge
$\overline{\text{HOLDRQ}}$	: Hold Request
$\overline{\text{HRD}}$	: Host Read
$\overline{\text{HRE}}$	: Host Read Enable
$\overline{\text{HWE}}$	: Host Write Enable
$\overline{\text{HWR}}$	: Host Write
I.C.	: Internally Connected
$\overline{\text{INT1}}$ - $\overline{\text{INT4}}$	: Interrupt
IV_{DD}	: Power Supply for DSP Core
$\overline{\text{MRD}}$	: Memory Read Output
$\overline{\text{MWR}}$	: Memory Write Output
NC	: Non-Connection
NU	: Not Used
P0 - P3	: Port
$\overline{\text{RESET}}$	: Reset
SCK1, SCK2	: Serial Clock Input
SI1, SI2	: Serial Data Input
SIAK1	: Serial Input Acknowledge
SIEN1, SIEN2	: Serial Input Enable
SO1, SO2	: Serial Data Output
SOEN1, SOEN2	: Serial Output Enable
SORQ1	: Serial Output Request
TCK	: Test Clock Input
TDI	: Test Data Input
TDO	: Test Data Output
TICE	: Test In-Circuit Emulator
TMS	: Test Mode Select
$\overline{\text{TRST}}$	: Test Reset
$\overline{\text{WAKEUP}}$	: Wakeup from STOP Mode
$\overline{\text{X}}$/Y	: X/Y Memory Select

CONTENTS

1. PIN FUNCTION

Because the pin numbers differ depending on the package, refer to the diagram of the package to be used.

1.1 Pin Function Description

• Power supply

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
IV_{DD}	35, 77, 85	B5, B7, G5	–	Power to DSP core (+2.5 V)	–
EV_{DD}	25, 50, 64, 75, 100	A3, C9, D1, D9, G1, J7	–	Power to I/O pins (+3 V)	–
GND	1, 26, 36, 51, 65, 76, 78, 86	A5, A7, C1, D6, E2, E7, F4, G2, G9	–	Ground	–

★ **Remark** Please supply voltage to the IV_{DD} and EV_{DD} pins simultaneously.

• System control

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
CLKIN	74	C7	Input	System clock input	–
CLKOUT	73	B9	Output	Internal system clock output	–
$\overline{\text{RESET}}$	87	C4	Input	Internal system reset signal input	
$\overline{\text{WAKEUP}}$	88	B4	Input	Stop mode release signal input. • When this pin is asserted active, the stop mode is released. The function of this pin can be activated or deactivated by a mask option.	$\overline{\text{INT4}}$

• Interrupt

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
$\overline{\text{INT1}}$ - $\overline{\text{INT3}}$	91 - 89	B3, D3, A4	Input	External maskable interrupt input. • Detected at the falling edge.	–
$\overline{\text{INT4}}$	88	B4	Input		$\overline{\text{WAKEUP}}$

- **External data memory interface (μPD77114 only)**

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
$\overline{X}$/Y	99	–	Output (3S)	Memory select signal output. 0: Uses X memory. 1: Uses Y memory.	–
DA0 - DA12	16 - 4	–	Output (3S)	Address bus of external data memory. • Accesses the external memory. • Continuously outputs the external memory address accessed last when the external memory is not being accessed. Kept low (0x000) if the external memory is never accessed after reset.	–
D0 - D15	34 - 27, 24 - 17	–	I/O (3S)	16-bit data bus. • Accesses the external memory.	–
$\overline{\text{MRD}}$	97	–	Output (3S)	Read output • External memory read	–
$\overline{\text{MWR}}$	96	–	Output (3S)	Write output • External memory write	–
$\overline{\text{HOLDRQ}}$	92	–	Input	Hold request signal • Input a low level to this pin when the external device uses the external data memory bus of the μPD77114.	–
$\overline{\text{BSTB}}$	94	–	Output	Bus strobe signal • This pin goes low when the μPD77114 uses the external data memory bus.	–
$\overline{\text{HOLDAK}}$	93	–	Output	Hold acknowledge signal • This pin goes low when the external device is enabled to use the external data memory bus of the μPD77114.	–

Remark Pins marked “3S” under the heading “I/O” go into a high-impedance state in the following conditions:
$\overline{X}$/Y, DA0-DA12, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$: When the bus is released ($\overline{\text{HOLDAK}}$ = low level)
D0-D15: When the external data memory is not being accessed and when the bus is released ($\overline{\text{HOLDAK}}$ = low level)

- **Serial interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
SCK1	39	H3	Input	Serial 1 clock input	–
SORQ1	42	J4	Output	Serial output 1 request	–
SOEN1	43	F3	Input	Serial output 1 enable	–
SO1	41	G4	Output (3S)	Serial data output 1	–
SIEN1	38	G3	Input	Serial input 1 enable	–
SI1	37	J3	Input	Serial data input 1	–
SIAK1	40	E3	Output	Serial input 1 acknowledge	–
SCK2	46	J6	Input	Serial 2 clock input	–
SOEN2	44	H4	Input	Serial output 2 enable	–
SO2	45	J5	Output (3S)	Serial data output 2	–
SIEN2	47	H5	Input	Serial input 2 enable	–
SI2	48	F6	Input	Serial data input 2	–

Remark The pins marked “3S” under the heading “I/O” go into a high-impedance state on completion of data transfer and input of the hardware reset ($\overline{\text{RESET}}$) signal.

- **Host interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
HA1	72	B8	Input	Specifies the register to be accessed by HD7 through HD0. • 1: Accesses the host interface status register (HST). • 0: Accesses the host transmit data register (HDT (out)) when read ($\overline{\text{HRD}}$ = 0), and host receive data register (HDT (in)) when written ($\overline{\text{HWR}}$ = 0).	–
HA0	71	C8	Input	Specifies the register to be accessed by HD7 through HD0. • 1: Accesses bits 15 through 8 of HST, HDT (in), and HDT (out). • 0: Accesses bits 7 through 0 of HST, HDT (in), and HDT (out).	–
$\overline{\text{HCS}}$	68	E6	Input	Chip select input	–
$\overline{\text{HRD}}$	69	D8	Input	Host read input	–
$\overline{\text{HWR}}$	70	D7	Input	Host write input	–
$\overline{\text{HRE}}$	66	–	Output	Host read enable output	–
$\overline{\text{HWE}}$	67	–	Output	Host write enable output	–
HD0 - HD7	63 - 56	F5, E8, E9, F7, G6, F9, F8, H8	I/O (3S)	8-bit host data bus	–

Remark The pins marked “3S” under the heading “I/O” go into a high-impedance state when the host interface is not being accessed.

- **I/O ports**

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
P0	55	H7	I/O	General-purpose I/O port	–
P1	54	G8	I/O		–
P2	53	G7	I/O		–
P3	52	H6	I/O		–

• **Debugging interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
TDO	79	C6	Output	For debugging	–
TICE	80	B6	Output		–
TCK	81	D5	Input		–
TDI	82	C5	Input		–
TMS	83	A6	Input		–
$\overline{\text{TRST}}$	84	A8	Input		–

• **Others**

Pin Name	Pin No.		I/O	Function	Shared by:
	100-pin TQFP	80-pin BGA			
I.C.	98	–	–	Internally connected. Leave this pin unconnected.	–
NU	–	A2, B1, B2, C2, C3, D2, D4, E1, E4, F1, F2, H1, H2, H9, J2, J8	–	No function pins. Connect to EV_{DD} via pull-up resistor, or connect to GND via pull-down resistor.	–
NC	2, 3, 49, 95	–	–	No-connect pins. Leave these pins unconnected.	–
–	–	A1, A9, J1, J9	–	Pins to strengthen soldering. Connect these pins to the board as necessary.	–

Caution If any signal is input to these pins or if an attempt is made to read these pins, the normal operation of the μPD77113A and 77114 is not guaranteed.

1.2 Connection of Unused Pins

1.2.1 Connection of Function Pins

When mounting, connect unused pins as follows:

Pin	I/O	Recommended Connection
$\overline{\text{INT1}}$ - $\overline{\text{INT4}}$	Input	Connect to EV_{DD}.
$\overline{\text{X}}$/Y	Output	Leave unconnected.
DA0 - DA12	Output	
D0 - D15[Note 1]	I/O	Connect to EV_{DD} via pull-up resistor, or connect to GND via pull-down resistor.
$\overline{\text{MRD}}$, $\overline{\text{MWR}}$	Output	Leave unconnected.
$\overline{\text{HOLDRQ}}$	Input	Leave unconnected. (internally pulled up).
$\overline{\text{BSTB}}$, $\overline{\text{HOLDAK}}$	Output	Leave unconnected.
SCK1, SCK2	Input	Connect to EV_{DD} or GND.
SI1, SI2	Input	
SIEN1, SIEN2	Input	Connect to GND.
SOEN1, SOEN2	Input	
SORQ1	Output	Leave unconnected.
SO1, SO2	Output	
SIAK1	Output	
HA0, HA1	Input	Connect to EV_{DD} or GND.
$\overline{\text{HCS}}$, $\overline{\text{HRD}}$, $\overline{\text{HWR}}$	Input	Connect to EV_{DD}.
$\overline{\text{HRE}}$, $\overline{\text{HWE}}$	Output	Leave unconnected.
HD0 - HD7[Note 2]	I/O	Connect to EV_{DD} via pull-up resistor, or connect to GND via pull-down resistor.
P0 - P3	I/O	
TCK	Input	Connect to GND via pull-down resistor.
TDO, TICE	Output	Leave unconnected.
TMS, TDI	Input	Leave unconnected. (internally pulled up).
$\overline{\text{TRST}}$	Input	Leave unconnected. (internally pulled down).
CLKOUT	Output	Leave unconnected.

Notes 1. These pins may be left unconnected if the external data memory is not accessed in the program. However, connect these pins as recommended in the halt and stop modes when the power consumption must be lowered.

2. These pins may be left unconnected if $\overline{\text{HCS}}$, $\overline{\text{HRD}}$, and $\overline{\text{HWR}}$ are fixed to the high level.
However, connect these pins as recommended in the halt and stop modes when the power consumption must be lowered.

1.2.2 Connection of no-function pins

Pin	I/O	Recommended Connection
I.C.	–	Leave unconnected.
NU	–	Connect to EV_{DD} via pull-up resistor, or connect to GND via pull-down resistor.
NC	–	Leave unconnected.

2. FUNCTION OUTLINE

2.1 Program Control Unit

This unit is used to execute instructions, and control branching, loops, interrupts, the clock, and the standby mode of the DSP.

2.1.1 CPU control

A three-stage pipeline architecture is employed and almost all the instructions, except some instructions such as branch instructions, are executed in one system clock.

2.1.2 Interrupt control

Interrupt requests input from external pins ($\overline{\text{INT1}}$ through $\overline{\text{INT4}}$) or generated by the internal peripherals (serial interface and host interface) are serviced. The interrupt of each interrupt source can be enabled or disabled. Multiple interrupts are also supported.

2.1.3 Loop control task

A loop function without any hardware overhead is provided. A loop stack with four levels is provided to support multiple loops.

2.1.4 PC stack

A 15-level PC stack that stores the program counter supports multiple interrupts and subroutine calls.

2.1.5 PLL

A PLL is provided as a clock generator that can multiply or divide an external clock input to supply an operating clock to the DSP. A multiple of ×1 to ×16 or a division ratio of 1/1 to 1/16 can be set by a mask option.

Two standby modes are available for lowering the power consumption while the DSP is not in use.

- HALT mode : Set by execution of the HALT instruction. The current consumption drops to several mA. The normal operation mode is recovered by an interrupt or hardware reset.
- STOP mode: Set by execution of the STOP instruction. The current consumption drops to several 10 μA. The normal operation mode is recovered by hardware reset or $\overline{\text{WAKEUP}}$ pin[Note].

Note If the WAKEUP function is activated by mask option

2.1.6 Instruction memory

The capacity and type of the memory differ depending on the model of the DSP.

64 words of the instruction RAM are allocated to interrupt vectors.

A boot-up ROM that boots up the instruction RAM is provided, and the instruction RAM can be initialized or rewritten by self boot (boot from the internal data ROM or external data space) or host boot (boot via host interface).

The μPD77113A and 77114 have 3.5K-word instruction RAM and 48K-word instruction ROM.

2.2 Arithmetic Unit

This unit performs multiplication, addition, logical operations, and shift, and consists of a 40-bit multiply accumulator, 40-bit data ALU, 40-bit barrel shifter, and eight 40-bit general-purpose registers.

2.2.1 General-purpose registers (R0 through R7)

These eight 40-bit registers are used to input/output data for arithmetic operations, and load or store data from/to data memory.

A general-purpose register (R0 to R7) is made up of three parts: R0L through R7L (bits 15 through 0), R0H through R7H (bits 31 through 16), and R0E through R7E (bits 39 through 32). Depending on the type of operation, RnL, RnH, and RnE are used as one register or in different combinations.

2.2.2 Multiply accumulator (MAC)

The MAC multiplies two 16-bit values, and adds or subtracts the multiplication result from one 40-bit value, and outputs a 40-bit value.

The MAC is provided with a shifter (MSFT: MAC ShiFTer) at the stage preceding the input stage. This shifter can arithmetically shift the 40-bit value to be added to or subtracted from the multiplication result 1 or 16 bits to the right .

2.2.3 Arithmetic logic unit (ALU)

This unit inputs one or two 40-bit values, executes an arithmetic or logical operation, and outputs a 40-bit value.

2.2.4 Barrel shifter (BSFT: Barrel ShiFTer)

The barrel shifter inputs a 40-bit value, shifts it to the left or right by any number of bits, and outputs a 40-bit value. The data may be arithmetically shifted to the right shifted to the right, in which case the data is sign-extended, or logically shifted to the right, in which case 0 is inserted from the MSB.

2.3 Data Memory Unit

The data memory unit consists of two banks of data memory and two data addressing units.

2.3.1 Data memory

The capacity and type of the memory differ depending on the model of the DSP. All DSPs have two banks of data memory (X data memory and Y data memory). A 64-word peripheral area is assigned in the data memory space.

The μPD77113A and 77114 have 16K words × 2 banks data RAM and 32K words × 2 banks data ROM.

In addition, the μPD77114 has an external data memory interface so that the external memory can be expanded to 8K words × 2 banks.

2.3.2 Data addressing unit

An independent data addressing unit is provided for each of the X data memory and Y data memory spaces.

Each data addressing unit has four data pointers (DPn), four index registers (DNn), one modulo register (DMX or DMY), and an address ALU.

2.4 Peripheral Units

A serial interface, host interface, general-purpose I/O port, and wait cycle register are provided. All these internal peripherals are mapped to the X data memory and Y data memory spaces, and are accessed from program as memory-mapped I/Os.

2.4.1 Serial interface (SIO)

Two serial interfaces are provided. These serial interfaces have the following features:

- Serial clock : Supplied from external source to each interface. The same clock is used for input and output on the interface.
- Frame length: 8 or 16 bits, and MSB or LSB first selectable for each interface and input or output
- Handshake : Handshaking with external devices is implemented with a dedicated status signal. With the internal units, polling, wait, or interrupt are used.

2.4.2 Host interface (HIO)

This is an 8-bit parallel port that inputs data from or outputs data to an external host CPU or DMA controller. In the DSP, a 16-bit register is mapped to memory for input data, output data, and status. Handshaking with an external device is implemented by using a dedicated status signal. Handshaking with internal units is achieved by means of polling, wait, or interrupts.

2.4.3 General-purpose I/O port (PIO)

This is a 4-bit I/O port that can be set in the input or output mode in 1-bit units.

2.4.4 Wait cycle register

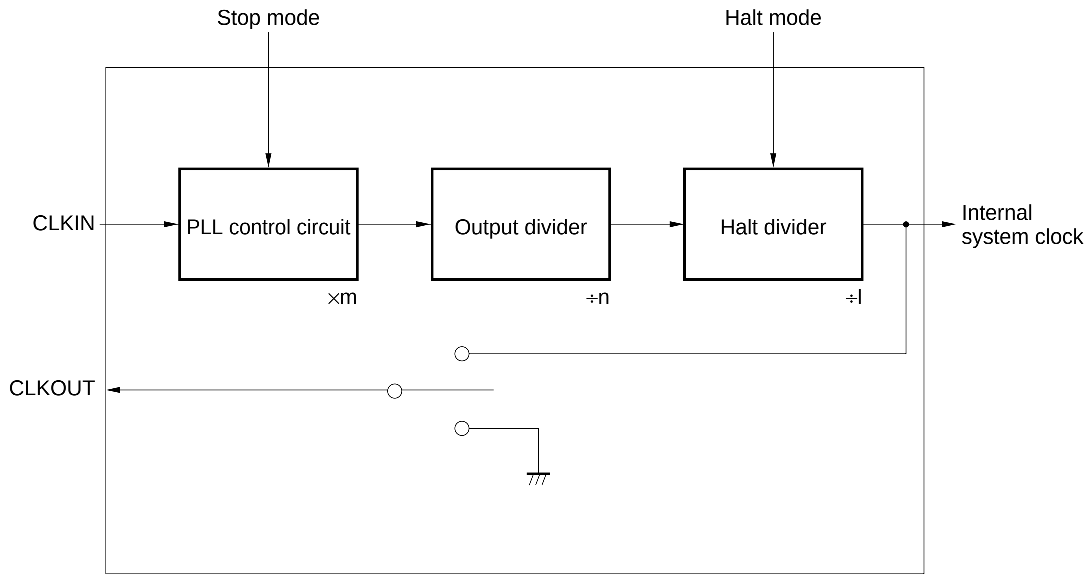
The number of wait cycles to be inserted when the external data memory area is accessed can be specified in advance by using a register (DWTR)[Note]. The number of wait cycles that can be set is 1, 3, or 7.

Note This function is not available on the μPD77113A because this DSP does not have an external data area.

3. CLOCK GENERATOR

The clock generator generates an internal system clock based on the external clock input from the CLKIN pin and supplies the generated clock to the internal units of the DSP.

For details of how to set the PLL multiple, refer to **4.2 Initializing PLL**, and **8.1 Clock Control Options**.



4. RESET FUNCTION

When a low level of a specified width is input to the $\overline{\text{RESET}}$ pin, the device is initialized.

4.1 Hardware Reset

If the $\overline{\text{RESET}}$ pin is asserted active (low level) for a specified period, the internal circuitry of the DSP is initialized. If the $\overline{\text{RESET}}$ pin is then deasserted inactive (high level), boot processing of the instruction RAM is performed according to the status of the port pins (P0 and P1). After boot processing, processing is executed starting from the instruction at address 0x200 of instruction memory (reset entry). In addition, a self-check is performed by the internal data RAM at the same time as the boot processing. This check takes about 20 ms (at 50 MHz operation, the length of this period is in inverse proportion to the operating frequency.)

On power application, the $\overline{\text{RESET}}$ pin must be asserted active (low level) after 4 input clocks have been input with the $\overline{\text{RESET}}$ pin in the inactive status (high level), after the supply voltage has reached the level of the operating voltage. In other words, no power-ON reset function is available. On power application, the PLL must be initialized.

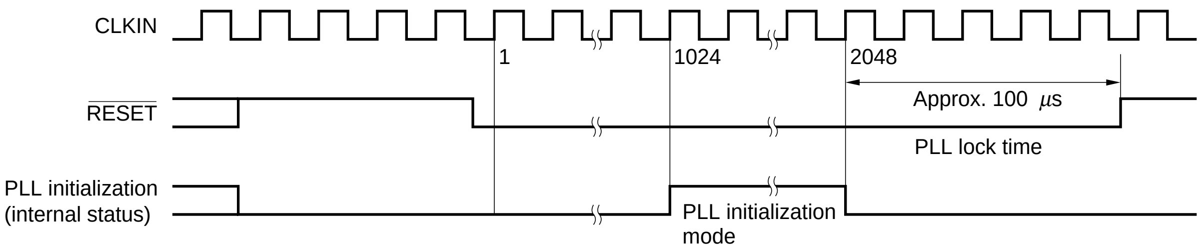
4.2 Initializing PLL

Initializing the PLL starts from the 1024th input clock after the $\overline{\text{RESET}}$ pin has been asserted active (low level). Initialization takes 1024 clocks and it takes the PLL 100 μs to be locked.

After that, the DSP operates with the set value of the PLL specified by a mask option when the $\overline{\text{RESET}}$ pin is deasserted inactive (high level).

After initializing the PLL, be sure to execute boot-up processing to re-initialize the internal RAM. To initialize the PLL, the internal memory contents and register status of the DSP are not retained.

If the $\overline{\text{RESET}}$ pin is deasserted inactive before the PLL initialization mode is set, the DSP is normally reset (the PLL is not initialized).



Caution Do not deassert the $\overline{\text{RESET}}$ signal inactive in the PLL initialization mode and during PLL lock period.

5. FUNCTIONS OF BOOT-UP ROM

To rewrite the contents of the instruction memory on power application or from program, boot up the instruction RAM by using the internal boot-up ROM.

The μPD77113A and 77114 have a function to verify the contents of the internal instruction RAM and a function to modify the instruction ROM in the boot-up ROM.

5.1 Boot at Reset

After hardware reset has been cleared, the boot program first reads the general-purpose I/O ports P0 and P1 and, depending on their bit pattern, determines the boot mode (self boot or host boot). After boot processing, processing is executed starting from the instruction at address 0x200 (reset entry) of the instruction memory.

The pins (P0 and P1) that specify the boot mode must be kept stable for the duration of 3 clocks before and for the duration of 12 clocks after reset has been cleared (the clock is input from CLKIN).

If host boot or self boot is specified, a self-check of the internal data RAM is performed at the same time as boot processing.

P1	P0	Boot Mode
0	0	Does not execute boot but branches to address 0x200[Note].
0	1	Executes host boot and then branches to address 0x200.
1	1	Executes self boot and then branches to address 0x200.
1	0	Setting prohibited

Note This setting is used when the DSP must be reset to recover from the standby mode after reset boot has been executed once.

5.1.1 Self boot

The boot-up ROM transfers the instruction code stored in the data memory space to the instruction RAM, based on the boot parameter written to address 0x4000 of the Y data memory. Generally, with a mask ROM model, this function is implemented by storing the instructions to be booted in the data ROM.

In addition, the instructions to be booted can be also stored in an external data area in the form of flash ROM, and self boot can be executed from this external data area.

5.1.2 Host boot

In this boot mode, a boot parameter and instruction code are obtained via the host interface, and transferred to the instruction RAM.

5.2 Reboot

By calling the next reboot entry from the program, the contents of the instruction RAM can be rewritten.

Reboot Mode			Entry Address
Self boot	X memory	Word reboot	0x2
		Byte reboot	0x4
	Y memory	Word reboot	0x1
		Byte reboot	0x3
Host boot	Host reboot		0x5

5.2.1 Self reboot

The instruction codes stored in the data memory are transferred to the instruction RAM.

Set the following parameters and call the entry address of the corresponding reboot mode to execute self reboot.

- R7L : Number of instruction steps for rebooting
- DP3: First address of X memory in which instruction codes are stored (in the case of reboot from X memory), or first address of the instruction memory to be loaded (in the case of reboot from Y memory)
- DP7: First address of instruction memory to be loaded (in the case of reboot from X memory), or first address of X memory in which instruction codes are stored (in the case of reboot from Y memory)

5.2.2 Host reboot

An instruction code is obtained via the host interface and transferred to the instruction RAM.

The entry address of is 0x5. Host reboot is executed by calling this address after setting the following parameter:

- R7L : Number of instruction steps for rebooting
- DP3: First address of instruction memory to be loaded

5.3 Signature Operation

The μPD77113A and 77114 have a signature operation function so that the contents of the internal instruction RAM can be verified. The signature operation performs a specific arithmetic operation on the data in the instruction RAM booted up, and returns the result to a register. Perform the signature operation in advance on the device when it is operating normally, and repeat the signature operation later to check whether the data in RAM is correct by comparing the operation result with the previous result. If the results are identical, there is no problem.

The entry address is 0x9. Execute the operation by calling this address after setting the following parameter. The operation result is stored in register R7.

- R7L: Number of instruction steps for operation
- DP3: First address of instruction memory for operation

5.4 Instruction ROM Modification

The μPD77113A and 77114 have a function to modify the contents of the internal instruction mask ROM. Instructions at up to four addresses can be modified.

The entry address is 0x10D. By calling this address with the following parameters, modification is performed.

R7L : Address of instruction ROM to be modified
R6H, R6L : Instruction code (32 bits)

6. STANDBY MODES

Two standby modes are available. By executing the corresponding instruction, each mode is set and the power consumption can be reduced.

6.1 HALT Mode

To set this mode, execute the HALT instruction. In this mode, functions other than clock circuit and PLL are stopped to reduce the current consumption.

To release the HALT mode, use an interrupt or hardware reset. When releasing the HALT mode using an interrupt, the contents of the internal registers and memory are retained. It takes several 10 system clocks to release the HALT mode when the HALT mode is released using an interrupt.

In the HALT Mode, the clock circuit of the μPD77111 family supplies the following clock as the internal system clock. The clock output from the CLKOUT pin is also as follows.

The clock output from the CLKOUT pin, however, has a high-level width that is equivalent to 1 cycle of the normal operation (i.e., the duty factor is not 50%).

- μPD77113A, 77114: 1/l of internal system clock (l = integer from 1 to 16, specified by mask option)

6.2 STOP Mode

To set this mode, execute the STOP instruction. In this mode, all the functions, including the clock circuit and PLL, are stopped and the power consumption is minimized with only leakage current flowing.

To release the STOP mode, use hardware reset or $\overline{\text{WAKEUP}}$ pin.

When releasing the STOP mode by using the $\overline{\text{WAKEUP}}$ pin, the contents of the internal registers and memory are retained, but it takes several 100 μs to release the mode.

The $\overline{\text{WAKEUP}}$ pin is multiplexed with the $\overline{\text{INT4}}$ pin. Usually, this pin functions as an interrupt pin, but functions as the $\overline{\text{WAKEUP}}$ pin when it is asserted active in the STOP mode. Whether the $\overline{\text{WAKEUP}}$ pin is used to release the STOP mode is selected by mask option. For details, refer to **8.2 WAKEUP Function**.

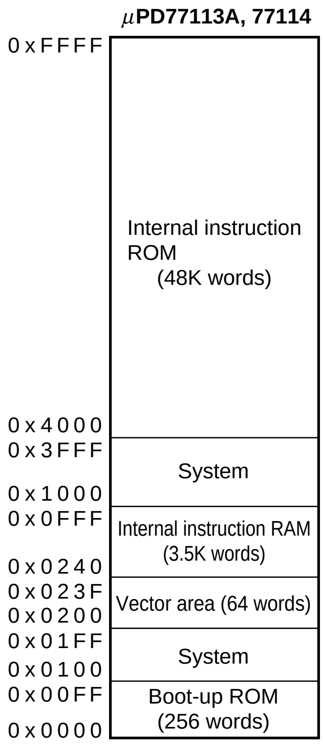
7. MEMORY MAP

A Harvard architecture, in which the instruction memory space and data memory space are separated is employed.

7.1 Instruction Memory

7.1.1 Instruction memory map

The instruction memory space consists of 64K words × 32 bits, and the capacity and type of the memory differ depending on the product.



Caution Programs and data cannot be placed at addresses reserved for the system, nor can these addresses be accessed. If these addresses are accessed, the normal operation of the device cannot be guaranteed.

7.1.2 Interrupt vector table

Addresses 0x200 through 0x23F of the instruction memory are entry points (vectors) of interrupts. Four instruction addresses are assigned to each interrupt source.

Vector	Interrupt Source
0x200	Reset
0x204	Reserved
0x208	
0x20C	
0x210	INT1
0x214	INT2
0x218	INT3
0x21C	INT4
0x220	SI1 input
0x224	SO1 output
0x228	SI2 input
0x22C	SO2 output
0x230	HI input
0x234	HO output
0x238	Reserved
0x23C	

Cautions 1. Although reset is not an interrupt, it is handled like an interrupt as an entry to a vector.

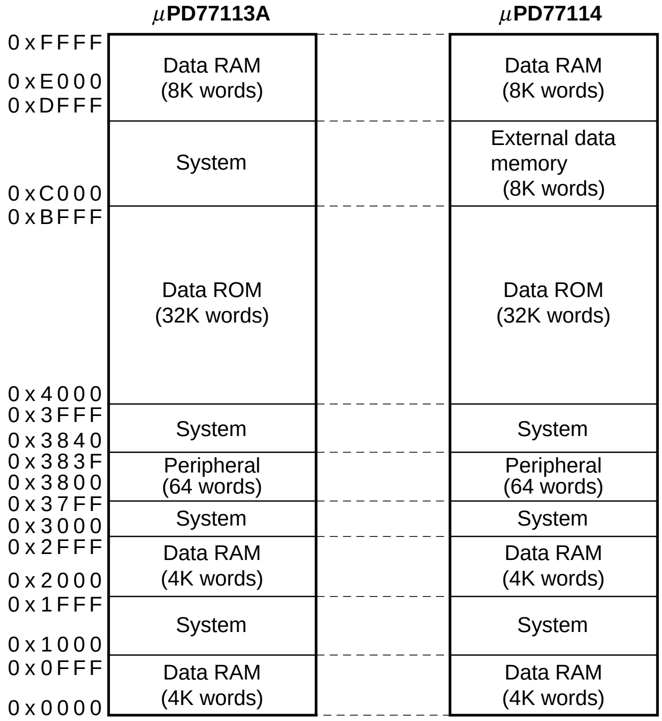
2. It is recommended that unused interrupt source vectors be used to branch an error processing routine.

3. Because a vector area also exists in the internal RAM area of the mask ROM model, this area must be booted up. In addition, because the entry address after reset is 0x200, address 0x200 must be booted up even when the internal instruction RAM and interrupts are not used.

7.2 Data Memory

7.2.1 Data memory map

The data memory space consists of an X memory space and a Y memory space of 64K words × 16 bits each, and the memory capacity and memory type differ depending on the product.



Caution Programs and data cannot be placed at addresses reserved for the system, nor can these addresses be accessed. If these addresses are accessed, the normal operation of the device cannot be guaranteed.

7.2.2 Internal peripherals

The internal peripherals are mapped to the internal data memory space.

X/Y Memory Address	Register Name	Function	Peripheral Name
0x3800	SDT1	First serial data register	SIO
0x3801	SST1	First serial status register	
0x3802	SDT2	Second serial data register	
0x3803	SST2	Second serial status register	
0x3804	PDT	Port data register	PIO
0x3805	PCD	Port command register	
0x3806	HDT	Host data register	HIO
0x3807	HST	Host status register	
0x3808	DWTR	Data memory wait cycle register	WTR
0x3809 - 0x383F	Reserved area	**Caution Do not access this area.**	–

Cautions
1. **The register names listed in this table are not reserved words of the assembler or the C language. Therefore, when using these names in assembler or C, the user must define them.**
2. **The same register is accessed, as long as the address is the same, regardless of whether the X memory space or Y memory space is accessed.**
3. **Even different registers cannot be accessed at the same time from both the X and Y memory spaces.**

8. MASK OPTION

The μPD77113A and 77114 have mask options that must be specified when an order for a ROM is placed. This section explains these mask options. The mask options are specified in the Workbench (WB77016) development tool. To order a mask ROM, output a mask ROM ordering file format (.msk file) using WB77016.

8.1 Clock Control Options

The following four clock related options must be specified.

- PLL multiple
- Output division ratio
- HALT division ratio
- Validity of CLKOUT pin

When the PLL multiple is m, output division ratio is n, and halt division ratio is l, the relationship between each operation mode and operating clock is as follows:

Operation Mode	Clock Supplied Inside DSP
Normal operation mode	m/n times external input clock
HALT mode	m/n/l times external input clock
STOP mode	Stopped

The PLL control circuit multiplies the input clock by an integer from 1 to 16. Specify the mask option of the PLL multiple so that the multiplied frequency falls within the specified PLL lock frequency range.

The output divider divides the clock multiplied by the PLL by an integer from 1 to 16. Specify the mask option of the output division ratio so that the frequency m/n times the external input clock supplied to the DSP falls within the specified operating frequency range of the DSP.

The HALT divider functions only in the HALT mode. It divides the clock of the output divider by an integer from 1 to 16 and supplies the divided clock to the internal circuitry. Specify the mask option of the HALT division ratio so that necessary division can be performed.

Whether the clock supplied to the internal circuitry of the DSP (internal system clock) is “output” or “not output” from the CLKOUT pin can be specified. Specify the mask option as necessary.

If an odd value (other than 1) is specified as the output division ratio, the high-level width of the clock output from the CLKOUT pin is equal to one cycle during normal operation (i.e., the clock does not have a duty factor of 50%).

8.2 WAKEUP Function

The $\overline{\text{WAKEUP}}$ pin can be used to release the STOP mode as well as a hardware reset.

If the STOP mode is released by means of a hardware reset, the status before the STOP mode was set cannot be restored after the STOP mode has been released. If the $\overline{\text{WAKEUP}}$ pin is used, however, the status before the STOP mode is set can be retained and program execution can be resumed starting from the instruction after the STOP instruction.

Whether the $\overline{\text{WAKEUP}}$ pin is used to release the STOP mode can be specified by a mask option.

When the WAKEUP function is specified valid, the $\overline{\text{WAKEUP}}$ pin is multiplexed with the $\overline{\text{INT4}}$ pin and it usually functions as an interrupt pin. The pin functions as the $\overline{\text{WAKEUP}}$ pin only in the STOP mode (if this pin is asserted active in the STOP mode, it is used only to release the STOP mode, and execution does not branch to an interrupt vector).

9. INSTRUCTIONS

9.1 Outline of Instructions

An instruction consists of 32 bits. Almost all the instructions, except some such as branch instructions, are executed with one system clock. The maximum instruction cycle of the μPD77113A and 77114 is 13.3 ns. The following nine types of instructions are available:

(1) Trinomial operation instructions

These instructions specify an operation by the MAC. As the operands, three general-purpose registers can be specified.

(2) Binomial operation instructions

These instructions specify an operation by the MAC, ALU, or BSFT. As the operands, two general-purpose registers can be specified. An immediate value can be specified for some of these instructions, instead of a general-purpose register, for one input.

(3) Uninominal operation instructions

These instructions specify an operation by the ALU. As the operands, one general-purpose register can be specified.

(4) Load/store instructions

These instructions transfer 16-bit values between memory and a general-purpose register. Any general-purpose register can be specified as the transfer source or destination.

(5) Register-to-register transfer instructions

These instructions transfer data from one general-purpose register to another.

(6) Immediate value setting instructions

These instructions write an immediate value to a general-purpose register and the registers of the address operation unit.

(7) Branch instructions

These instruction specify branching of program execution.

(8) Hardware loop instructions

These instruction specify repetitive execution of an instruction.

(9) Control instructions

These instructions are used to control the program.

9.2 Instruction Set and Operation

An operation is written in the operation field for each instruction in accordance with the operation representation format of that instruction. If two or more parameters can be written, select one of them.

(a) Representation formats and selectable registers

The following table shows the representation formats and selectable registers.

Representation Format	Selectable Register
r0, r0′, r0″	R0 - R7
rl, rl′	R0L - R7L
rh, rh′	R0H - R7H
re	R0E - R7E
reh	R0EH - R7EH
dp	DP0 - DP7
dn	DN0 - DN7
dm	DMX, DMY
dpx	DP0 - DP3
dpy	DP4 - DP7
dpx_mod	DPn, DPn++, DPn−−, DPn##, DPn%%, !DPn## (n = 0 - 3)
dpy_mod	DPn, DPn++, DPn−−, DPn##, DPn%%, !DPn## (n = 4 - 7)
dp_imm	DPn##imm (n = 0 - 7)
*xxx	Contents of memory with address xxx <Example> If the contents of the DP0 register are 1000, *DP0 indicates the contents of address 1000 of the memory.

(b) Modifying data pointer

The data pointer is modified after the memory has been accessed. The result of modification becomes valid starting from the instruction that immediately follows. The data pointer cannot be modified.

Example	Operation
DPn	Nothing is done (value of DPn is not changed.)
DPn++	DPn ← DPn + 1
DPn––	DPn ← DPn – 1
DPn##	DPn ← DPn + DNn (Adds value of corresponding DN0 to DN7 to DP0 to DP7.) Example: DP0 ← DP0 + DN0
DPn%%	(n = 0 - 3) DPn = ((DP_L + DNn) mod (DMX + 1)) + DP_H
	(n = 4 - 7) DPn = ((DP_L + DNn) mod (DMY + 1)) + DP_H
!DPn##	Reverses bits of DPn and then accesses memory. After memory access, DPn ← DPn + DNn
DPn##imm	DPn ← DPn + imm

(c) Instructions that can be simultaneously written

Instructions that can be simultaneously written are indicated by √.

(d) Status of overflow flag (OV)

The status of the overflow flag is indicated by the following symbol:

●: Not affected

↕: Set to 1 when overflow occurs

Caution If an overflow does not occur as a result of an operation, the overflow flag is not reset but retains the status before the operation.

Instruction Set

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Uninominal	Load/ store	Transfer	Immediate value	Branch	Loop	Control	OV
Trinomial operation	Multiply add	ro = ro + rh * rh′	ro ← ro + rh * rh′				√						↕
	Multiply sub	ro = ro – rh * rh′	ro ← ro – rh * rh′				√						↕
	Sign unsign multiply add	ro = ro + rh * rl (rl is in positive integer format.)	ro ← ro + rh * rl				√						↕
	Unsign unsign multiply add	ro = ro + rl * rl′ (rl and rl’ are in positive integer format.)	ro ← ro + rl * rl′				√						↕
	1-bit shift multiply add	ro = (ro>>1) + rh * rh′	ro ← $\frac{ro}{2}$ + rh * rh′				√						↕
	16-bit shift multiply add	ro = (ro>>16) + rh * rh′	ro ← $\frac{ro}{2^{16}}$ + rh * rh′				√						●
Binomial operation	Multiply	ro = rh * rh′	ro ← rh * rh′				√						●
	Add	ro″ = ro + ro′	ro″ ← ro + ro′				√						↕
	Immediate add	ro′ = ro + imm	ro′ ← ro + imm (where imm ≠ 1)										↕
	Sub	ro″ = ro – ro′	ro″ ← ro – ro′				√						↕
	Immediate sub	ro′ = ro – imm	ro ← ro – imm (where imm ≠ 1)										↕
	Arithmetic right shift	ro′ = ro SRA rl	ro′ ← ro >> rl				√						●
	Immediate arithmetic right shift	ro′ = ro SRA imm	ro′ ← ro >> imm										●
	Logical right shift	ro′ = ro SRL rl	ro′ ← ro >> rl				√						●
	Immediate logical right shift	ro′ = ro SRL imm	ro′ ← ro >> imm										●
	Logical left shift	ro′ = ro SLL rl	ro′ ← ro << rl				√						●
	Immediate logical left shift	ro′ = ro SLL imm	ro′ ← ro << imm										●
	AND	ro″ = ro & ro′	ro″ ← ro & ro′				√						●
	Immediate AND	ro′ = ro & imm	ro′ ← ro & imm										●
	OR	ro″ = ro ∣ ro′	ro″ ← ro ∣ ro′				√						●
	Immediate OR	ro′ = ro ∣ imm	ro′ ← ro ∣ imm										●
	Exclusive OR	ro″ = ro ^ ro′	ro″ ← ro ^ ro′				√						●
	Immediate exclusive OR	ro′ = ro ^ imm	ro′ ← ro ^ imm										●

Instruc-tion	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trino-mial	Bino-mial	Unino-minal	Load/store	Trans-fer	Imme-diate-value	Bran-ch	Loop	Cont-rol	OV
Binomial operation	Less than	ro″ = LT (ro, ro′)	if (ro < ro′) {ro″ ← 0x0000000001} else {ro″ ← 0x0000000000}				√						●
Uninom-inal operation	Clear	CLR (ro)	ro ← 0x0000000000				√					√	●
	Increment	ro′ = ro + 1	ro′ ← ro + 1				√					√	↕
	Decrement	ro′ = ro – 1	ro′ ← ro – 1				√					√	↕
	Absolute value	ro′ = ABS (ro)	if (ro < 0) {ro′ ← –ro} else {ro′ ← ro}				√					√	↕
	1's complement	ro′ = ~ro	ro′ ← ~ro				√					√	●
	2's complement	ro′ = –ro	ro′ ← –ro				√					√	↕
	Clip	ro′ = CLIP (ro)	if (ro > 0x007FFFFFFF) {ro′ ← 0x007FFFFFFF} elseif {ro < 0xFF80000000} {ro′ ← 0xFF80000000} else {ro′ ← ro}				√					√	●
	Round	ro′ = ROUND (ro)	if (ro > 0x007FFF0000) {ro′ ← 0x007FFF0000} elseif {ro < 0xFF80000000} {ro′ ← 0xFF80000000} else {ro′ ← (ro + 0x8000) & 0xFFFFFF0000}				√					√	●
	Exponent	ro′ = EXP (ro)	ro′ ← $\log_2 (\frac{1}{ro})$				√					√	●
	Substitution	ro′ = ro	ro′ ← ro				√					√	●
	Accumulated addition	ro′ + = ro	ro′ ← ro′ + ro				√					√	↕
	Accumulated subtraction	ro′ – = ro	ro′ ← ro′ – ro				√					√	↕
	Division	ro′ / = ro	if (sign (ro′) == sign (ro)) {ro′ ← (ro′ – ro) << 1} else {ro′ ← (ro′ + ro)<<1} if (sign (ro′)==0) {ro′ ← ro′ + 1}				√					√	↕

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Uninominal	Load/store	Transfer	Immediate value	Branch	Loop	Control	OV
Load/store	Parallel load/store[Notes 1, 2]	ro = *dpx_mod ro′ = *dpy_mod	ro ← *dpx, ro′ ← *dpy	√	√	√							●
		ro = *dpx_mod *dpy_mod = rh	ro ← *dpx, *dpy ←rh										
		*dpx_mod = rh ro = *dpy_mod	*dpx ← rh, ro ← *dpy										
		*dpx_mod = rh *dpy_mod = rh′	*dpx ← rh, *dpy ← rh′										
	Partial load/store[Notes 1, 2, 3]	dest = *dpx_mod dest′ = *dpy_mod	dest ← *dpx, dest′ ← *dpy										●
		dest = *dpx_mod *dpy_mod = source	dest ← *dpx, *dpy ← source										
		*dpx_mod = source dest = *dpy_mod	*dpx ← source, dest ← *dpy										
		*dpx_mod = source *dpy_mod = source′	*dpx ← source, *dpy ← source′										
	Direct addressing load/store[Note 4]	dest = *addr	dest ← *addr										●
		*addr = source	*addr ← source										
	Immediate value index load/store[Note 5]	dest = *dp_imm	dest ← *dp										●
		*dp_imm = source	*dp ← source										
Register-to-register transfer	Register-to-register transfer[Note 6]	dest = rl	dest ← rl									√	●
		rl = source	rl ← source										
Immediate value setting	Immediate value setting	rl = imm (where imm = 0 to 0xFFFF)	rl ← imm										●
		dp = imm (where imm = 0 to 0xFFFF)	dp ← imm										
		dn = imm (where imm = 0 to 0xFFFF)	dn ← imm										
		dm = imm (where imm = 1 to 0xFFFF)	dm ← imm										

Notes **1.** Of the two mnemonics, either one of them or both can be written.

2. After transfer, modification specified by mod is performed.

3. Select any of dest, dest' = {ro, reh, re, rh, rl}, source, source' = {re, rh, rl}.

4. Select any of dest = {ro, reh, re, rh, rl}, source = {re, rh, rl}, addr = $\left\{\begin{array}{l}\text{0: X-0xFFF : X (X memory)} \\ \text{0: Y-0xFFFF: Y (Y memory)}\end{array}\right\}$.

5. Select any of dest = {ro, reh, re, rh, rl}, source = {re, rh, rl}.

6. Select any register other than general-purpose registers as dest and source.

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Uninominal	Load/ store	Transfer	Immediate value	Branch	Loop	Control	OV
Branch	Jump	JMP imm	PC ← imm									√	●
	Register indirect jump	JMP dp	PC ← dp									√	●
	Subroutine call	CALL imm	SP ← SP + 1 STK ← PC + 1 PC ← imm									√	●
	Register indirect subroutine call	CALL dp	SP ← SP + 1 STK ← PC + 1 PC ← dp									√	●
	Return	RET	PC ← STK SP ← SP – 1									√	●
	Interrupt return	RETI	PC ← STK STK ← SP – 1 Recovery of interrupt enable flag									√	●
Hardware loop	Repeat	REP count	Start RC ← count RF ← 0 During repeat PC ← PC RC ← RC – 1 End PC ← PC + 1 RF ← 1										●
	Loop	LOOP count (instruction of two or more lines)	Start RC ← count RF ← 0 During repeat PC ← PC RC ← RC – 1 End PC ← PC + 1 RF ← 1										●
	Loop hop	LPOP	LC ← LSR3 LE ← LSR2 LS ← LSR1 LSP ← LSP – 1										●
Control	No operation	NOP	PC ← PC + 1										●
	Halt	HALT	CPU stops.										●
	Stop	STOP	CPU, PLL, and OSC stop.										●
	Condition	IF (ro cond)	Condition test			√		√		√			●
	Forget interrupt	FINT	Discard interrupt request										●

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	IV_{DD}	For DSP core	– 0.5 to +3.6	V
	EV_{DD}	For I/O pins	–0.5 to +4.6	V
Input voltage	V_I	V_I < EV_{DD} + 0.5 V	–0.5 to +4.1	V
Output voltage	V_O		–0.5 to +4.1	V
Storage temperature	T_{stg}		–65 to +150	°C
Operating temperature	T_A		–40 to +85	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used unber conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Operating voltage	IV_{DD}	For DSP core		1.8		2.7	V
	EV_{DD}	For I/O pins	IV_{DD} = 1.8 to 2.7 V	2.7		3.3	V
			IV_{DD} = 2.3 to 2.7 V			3.6	
Input voltage	V_I			0		EV_{DD}	V

Capacitance (T_A = +25°C, IV_{DD} = 0 V, EV_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, Pins other than those tested: 0 V		10		pF
Output capacitance	C_O			10		pF
I/O capacitance	C_{IO}			10		pF

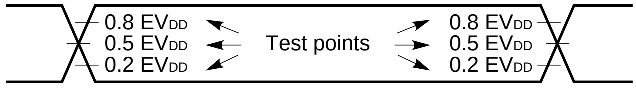
DC Characteristics (Unless otherwise specified, T_A = –40 to +85°C, with IV_{DD} and EV_{DD} within recommended operating condition range)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IHN}	Pins other than below	0.7 EV_{DD}		EV_{DD}	V
	V_{IHS}	CLKIN, $\overline{\text{RESET}}$, $\overline{\text{INT1}}$ - $\overline{\text{INT4}}$, SCK1, SIEN1, SOEN1, SCK2, SIEN2, SOEN2	0.8 EV_{DD}		EV_{DD}	V
	V_{IHC}	CLKIN	0.5 EV_{DD} +0.25		EV_{DD}	V
Low-level input voltage	V_{IL}	Pins other than below	0		0.2 EV_{DD}	V
	V_{IC}	CLKIN	0		0.5 EV_{DD} –0.25	V
High-level output voltage	V_{OH}	I_{OH} = –2.0 mA	0.7 EV_{DD}			V
		I_{OH} = –100 μA	0.8 EV_{DD}			V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA			0.2 EV_{DD}	V
High-level input leakage current	I_{LH}	Other than TDI, TMS, and $\overline{\text{TRST}}$ V_I = EV_{DD}	0		10	μA
Low-level input leakage current	I_{LL}	Other than TDI, TMS, and $\overline{\text{TRST}}$ V_I = 0 V	–10		0	μA
Pull-up pin current	I_{PUI}	TDI, TMS, 0 V ≤ V_I ≤ EV_{DD}	–250		0	μA
Pull-down pin current	I_{PDI}	$\overline{\text{TRST}}$, 0 V ≤ V_I ≤ EV_{DD}	0		250	μA
Internal supply current [V_{IHN} = V_{IHS} = EV_{DD}, V_{IL} = 0 V, no load]	I_{DD} Note	During operating, 30 ns, IV_{DD} = 2.7 V		TBD	75	mA
	I_{DDH}	In halt mode, t_{cC} = 30 ns, divided by eight, IV_{DD} = 2.7 V		TBD	10	mA
	I_{DDS}	In stop mode, 0°C < T_A < 60°C			100	μA

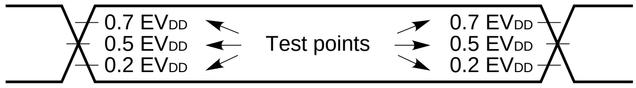
Note The TYP. values are when an ordinary program is executed.
The MAX. values are when a special program that brings about frequent switching inside the device is executed.

Common Test Criteria of Switching Characteristics

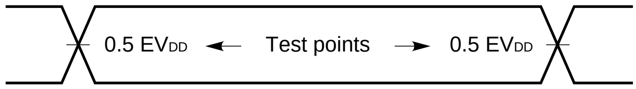
CLKIN, $\overline{\text{RESET}}$, $\overline{\text{INT1}}$ - $\overline{\text{INT4}}$, SCK1, SIEN1, SOEN1, SCK2, SIEN2, SOEN2



Input
(other than above)



Output



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AC Characteristics (T_A = –40 to +85°C, with IV_{DD} and EV_{DD} within recommended operating condition range)

Clock

Timing requirements

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
CLKIN cycle time[Note 1]	t_{cCX}			25			ns
		PLL lock range[Note 2]	IV_{DD} = 1.8 to 2.7 V	25 × m		50 × m	ns
			IV_{DD} = 2.3 to 2.7 V	10 × m		50 × m	ns
CLKIN high-level width	t_{wCXH}			12.5			ns
CLKIN low-level width	t_{wCXL}			12.5			ns
CLKIN rise/fall time	t_{rfCX}					5	ns
Internal clock cycle time requirements[Note 3]	$t_{cC\ (R)}$	IV_{DD} = 1.8 to 2.7 V		25			ns
		IV_{DD} = 2.3 to 2.7 V		13.3			ns

Notes 1. m: Multiple, n: Division ratio

2. This is the range in which the PLL is locked (stably oscillates). Input t_{cCX} within this range.

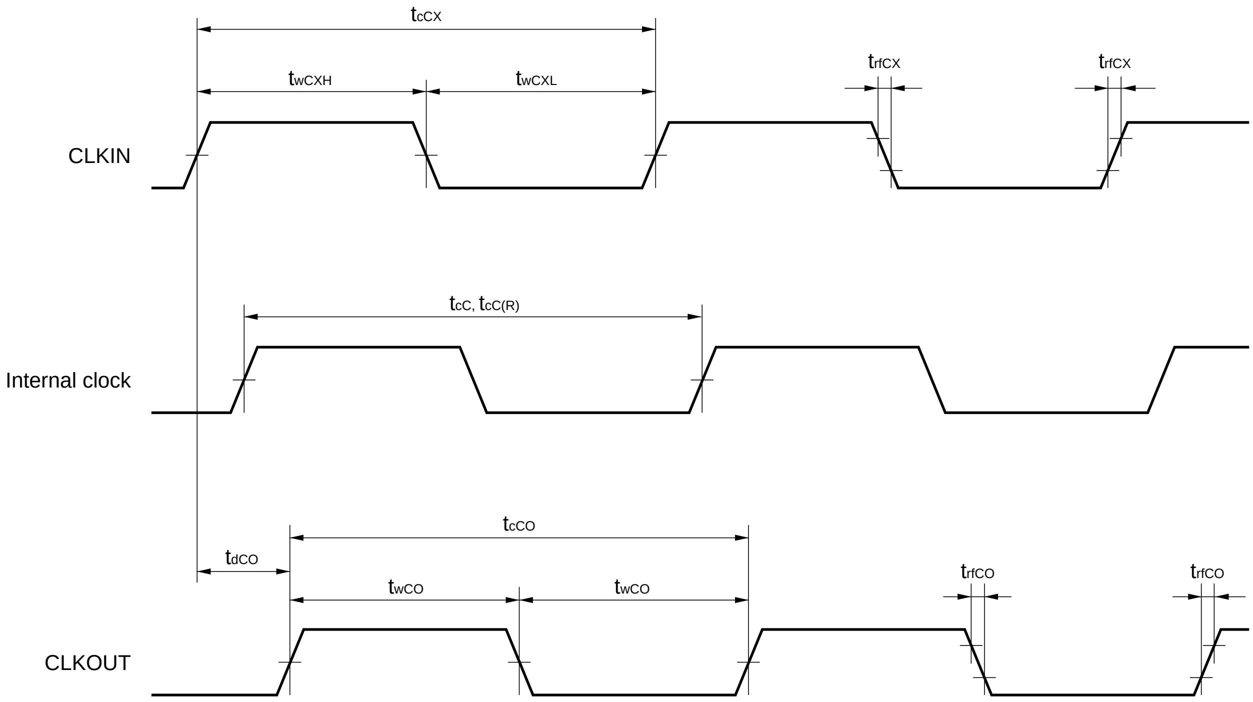
3. Input t_{cCX} so that the value of (t_{cCX} ÷ m × n) satisfies this condition.

Switching characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Internal clock cycle[Note]	t_{cC}	During normal operation			t_{cCX} × n ÷ m		ns
		In HALT mode			t_{cCX} × n ÷ m × l		ns
CLKOUT cycle time	t_{cCO}				t_{cC}		ns
★ CLKOUT width	t_{wCO}	During normal operation	n = 1, or even number	t_{cC} ÷ 2 – 3			ns
			n = odd number (other than 1)	t_{cC} ÷ n ÷ 2 – 3			ns
		In HALT mode		t_{cC} ÷ n ÷ 2 – 3			ns
CLKOUT rise/fall time	t_{rfCO}					5	ns
CLKOUT delay time	t_{dCO}	IV_{DD} = 1.8 to 2.7 V				20	ns
		IV_{DD} = 2.3 to 2.7 V				15	ns

Note m: Multiple, n: Division ratio, l: HALT division ratio

Clock I/O timing



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Reset, Interrupt

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	$t_{w\ (RL)}$	On power application[Note 1], in STOP mode	100 + $2048t_{cCX}$			μs
		During normal operation, in HALT mode	$4t_{cC}$[Note 2]		**Note 3**	ns
$\overline{\text{RESET}}$ recovery time	$t_{rec\ (R)}$	On power application[Note 4]	$4t_{cCX}$			ns
			$4t_{cC}$[Note 2]			ns
$\overline{\text{WAKEUP}}$ low-level width	$t_{w\ (WAKEUPL)}$		100			μs
$\overline{\text{INT1}}$ - $\overline{\text{INT4}}$ low-level width	$t_{w\ (INTL)}$		$3t_{cC}$[Note 2]			ns
$\overline{\text{INT1}}$ - $\overline{\text{INT4}}$ recovery time	$t_{rec\ (INT)}$		$3t_{cC}$			ns

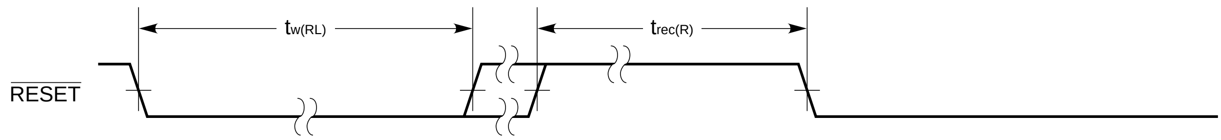
Notes 1. The value on power application is the time from when the supply voltages have reached IV_{DD} = 1.8 V and EV_{DD} = 2.7 V. A stable clock input is also required.

2. Note that t_{cC} is I (I = integer of 1 to 16) times that during normal operation in the HALT mode.

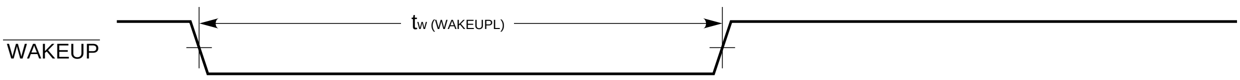
3. If the low-level width of $\overline{\text{RESET}}$ is greater than $1024t_{cC}$, the PLL initialization mode is triggered. If there is no need to use the PLL initialization mode, set the width to less than $1024t_{cC}$.

4. When the power is turned on, a recovery period of $4t_{cCX}$ is necessary before inputting RESET.

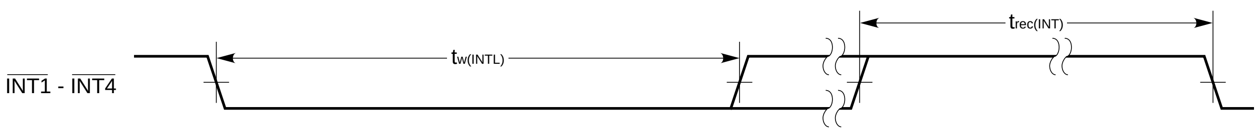
Reset timing



WAKEUP timing



Interrupt timing



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External Data Memory Access (μPD77114 only)

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Read data setup time	t_{suDDRD}		18			ns
Read data hold time	t_{hDDRD}		0			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address cycle time	t_{rcDA}			$t_{cC} + (t_{cC} \times t_{cDW})$ Note		ns
Address output hold time	t_{hDA}		0			ns
$\overline{\text{MRD}}$ output delay time	t_{dDR}				5	ns
Write data output valid time	t_{vDDWD}				5	ns
Write data output hold time	t_{hDDWD}		0			ns
$\overline{\text{MWR}}$ output delay time	t_{dDW}		0		0.5 t_{cC}	ns
$\overline{\text{MWR}}$ output hold time	t_{hDA}		0			ns
$\overline{\text{MWR}}$ low-level width	t_{wDWL}		$t_{cC} \times t_{cDW} - 3$			ns
$\overline{\text{MWR}}$ high-level width	t_{wDWH}		0.5 $t_{cC} - 3$			ns

Note t_{cDW}: Number of data wait cycles

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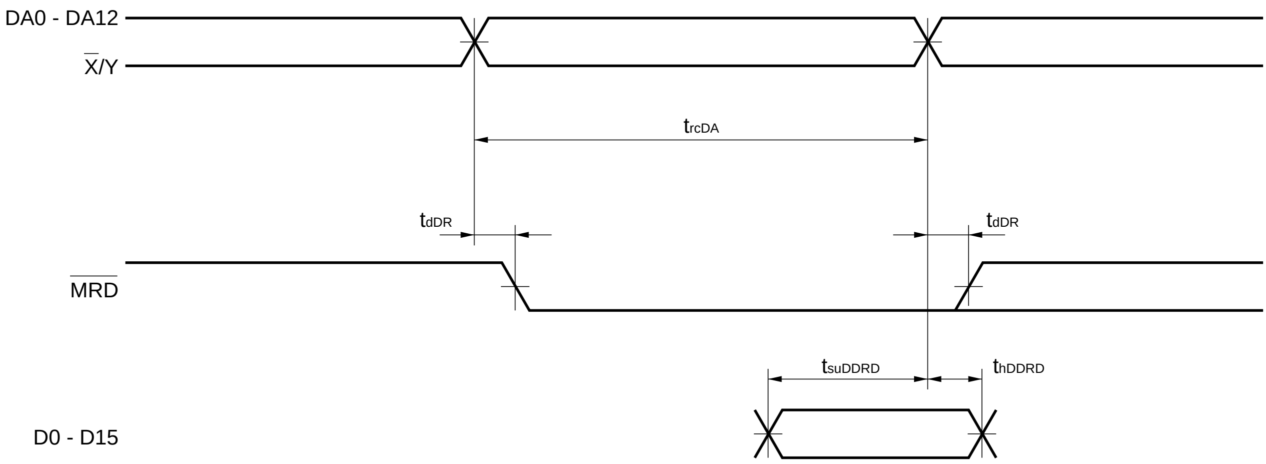
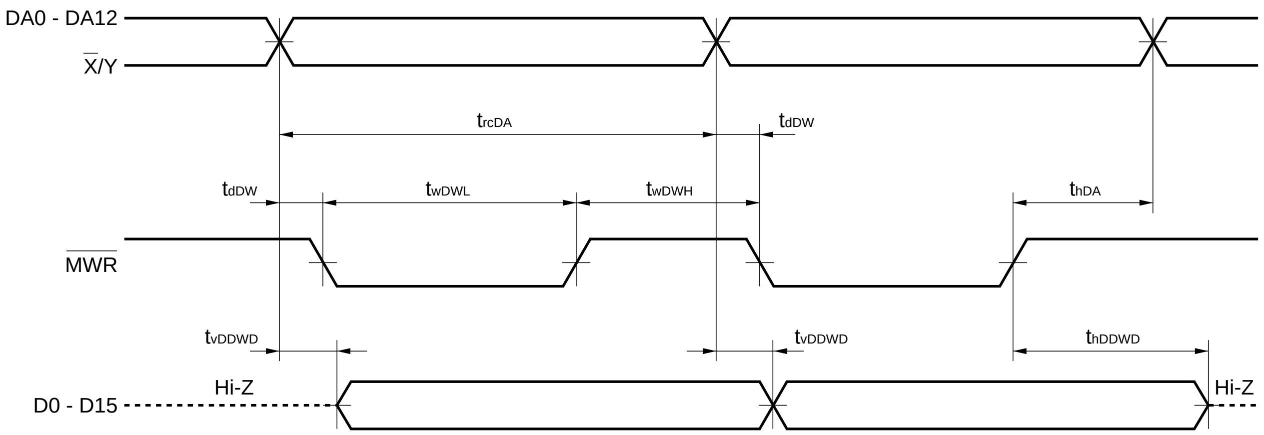
External data memory access timing (read)



External data memory access timing (write)



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Bus Arbitration (μPD77114 only)

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{HOLDRQ}}$ setup time	t_{suHRQ}		0			ns
$\overline{\text{HOLDRQ}}$ hold time	t_{hHRQ}		0			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{BSTB}}$ hold time	t_{hBS}		0			ns
$\overline{\text{BSTB}}$ output delay time	t_{dBS}				20	ns
$\overline{\text{HOLDAK}}$ output delay time	t_{dHAK}				18	ns
Data hold time during bus arbitration	$t_{h\ (BS\text{-}D)}$				25	ns
Data valid time during bus arbitration	$t_{v\ (BS\text{-}D)}$				25	ns

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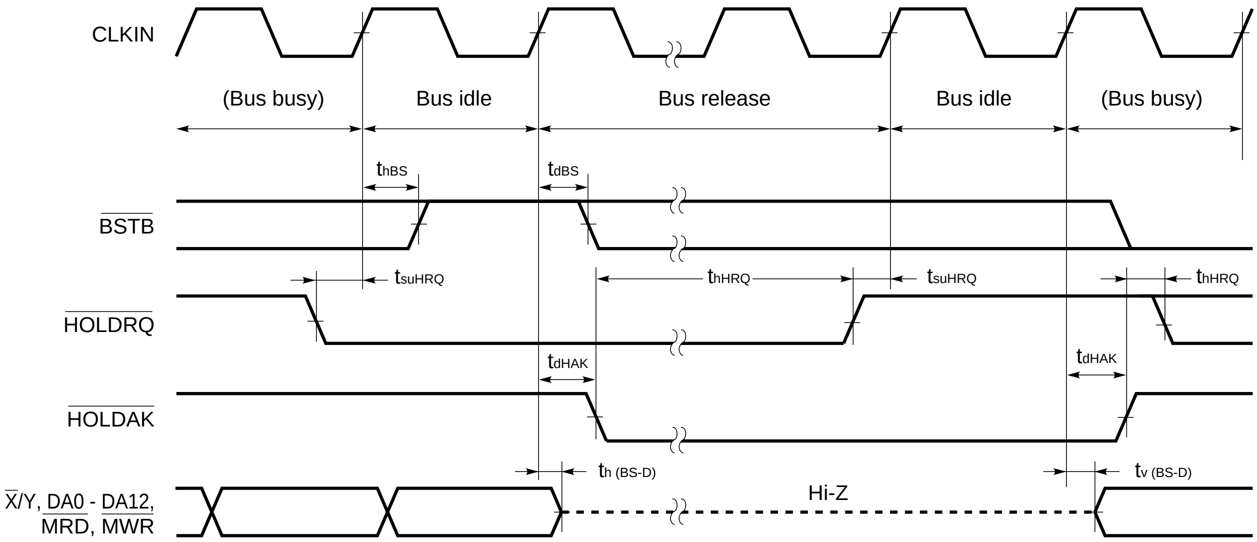
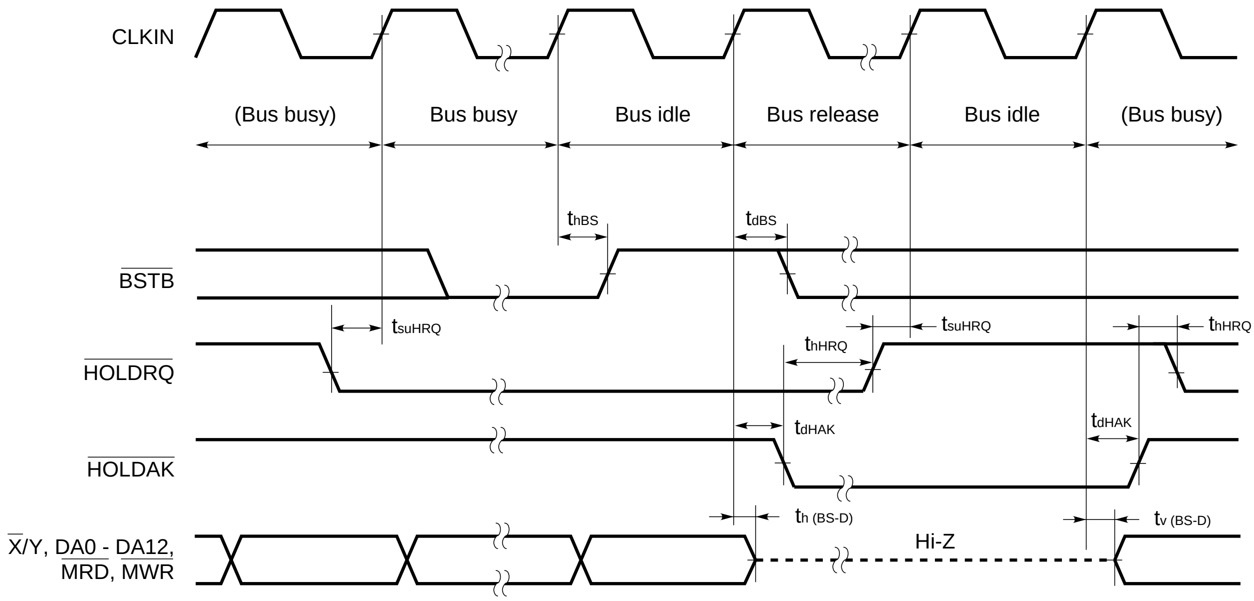
Bus arbitration timing (when bus is idle)



Bus arbitration timing (when bus is busy)



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Serial Interface

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK cycle time	t_{cSC}		60			ns
SCK high-/low-level width	t_{wSC}		25			ns
SCK rise/fall time	t_{rfSC}				20	ns
SOEN setup time	t_{suSOE}	IV_{DD} = 1.8 to 2.7 V	10			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
SOEN hold time	t_{hSOE}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
SIEN setup time	t_{suSIE}	IV_{DD} = 1.8 to 2.7 V	10			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
SIEN hold time	t_{hSIE}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
SI setup time	t_{suSI}	IV_{DD} = 1.8 to 2.7 V	10			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
SI hold time	t_{hSI}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SORQ output delay time	t_{dSOR}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
SORQ hold time	t_{hSOR}		0			ns
SO output delay time	t_{dSO}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
SO hold time	t_{hSO}		0			ns
SIAK output delay time	t_{dSIA}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
SIAK hold time	t_{hSIA}		0			ns

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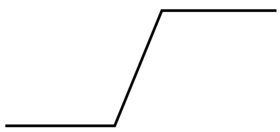
Caution If noise is superimposed on the serial clock, the serial interface may be deadlocked. Bear in mind the following points when designing your system:

- **Reinforce the wiring for power supply and ground (if noise is superimposed on the power and ground lines, it has the same effect as if noise were superimposed on the serial clock).**
- **Shorten the wiring between the device's SCK1 and SCK2 pins, and clock supply source.**
- **Do not cross the signal lines of the serial clock with any other signal lines. Do not route the serial clock line in the vicinity of a line through which a high alternating current flows.**
- **Supply the clock to the SCK1 and SCK2 pins of the device from the clock source on a one-to-one basis. Do not supply clock to several devices from one clock source.**
- **Exercise care that the serial clock does not overshoot or undershoot. In particular, make sure that the rising and falling of the serial clock waveform are clear.**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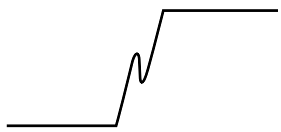
Make sure that the serial clock rises and falls linearly.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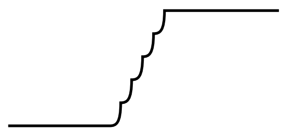
The serial clock must not bound. Noise must not be superimposed on the serial clock.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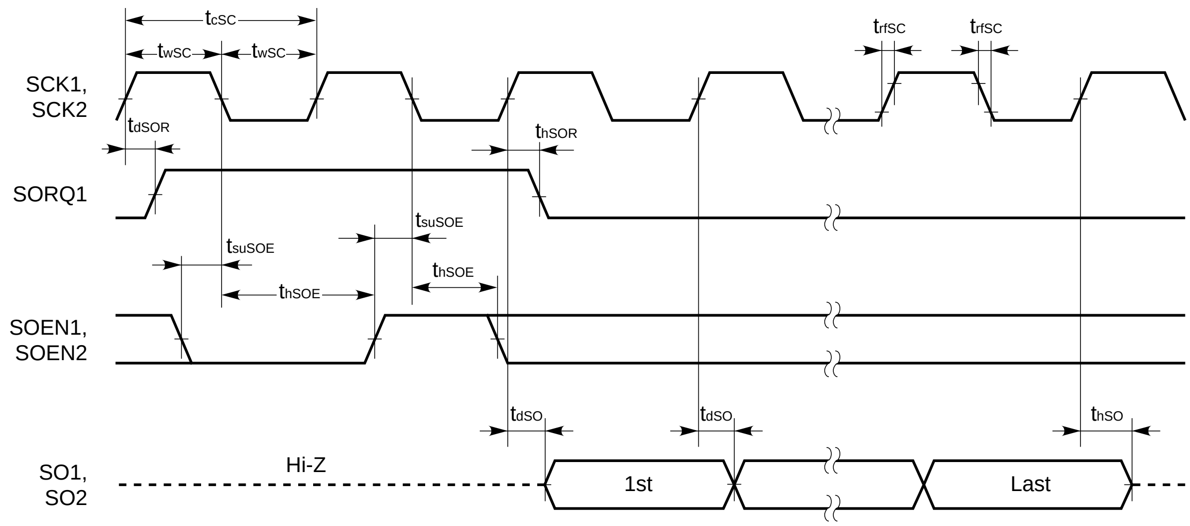
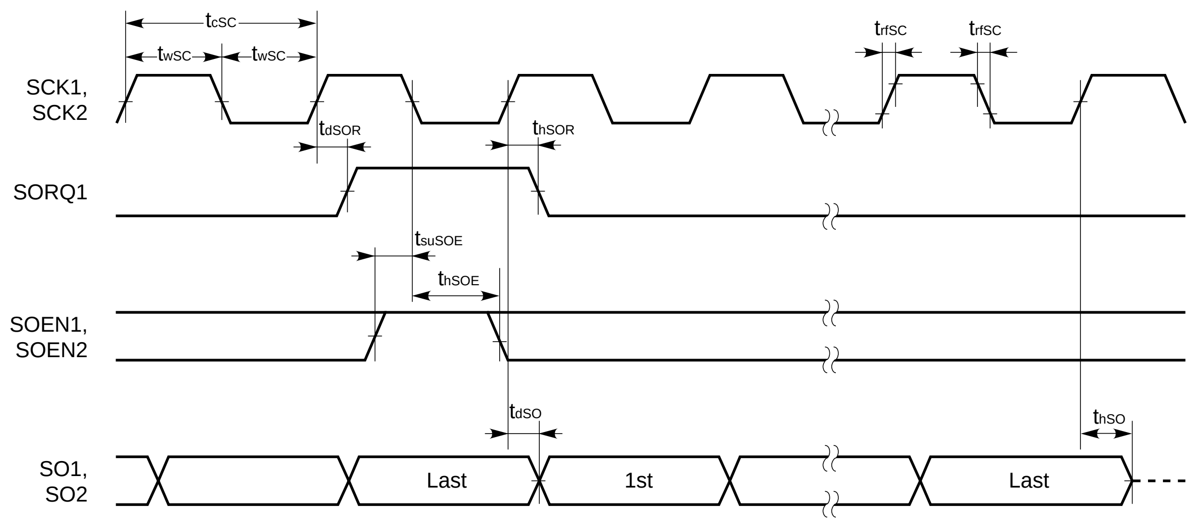
The serial clock must not rise or fall step-wise.

Serial output timing 1



Serial output timing 2 (during successive output)



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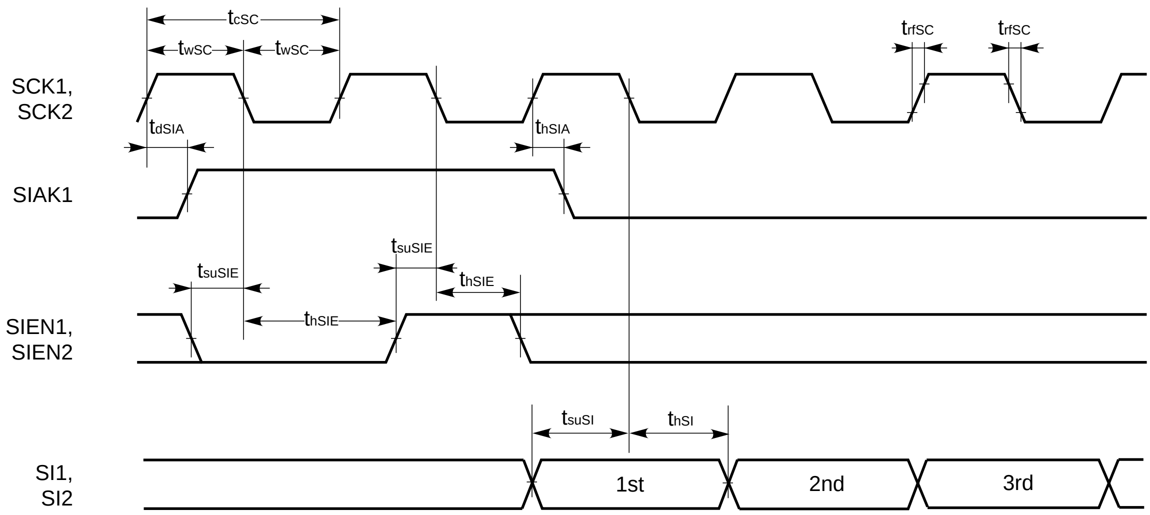
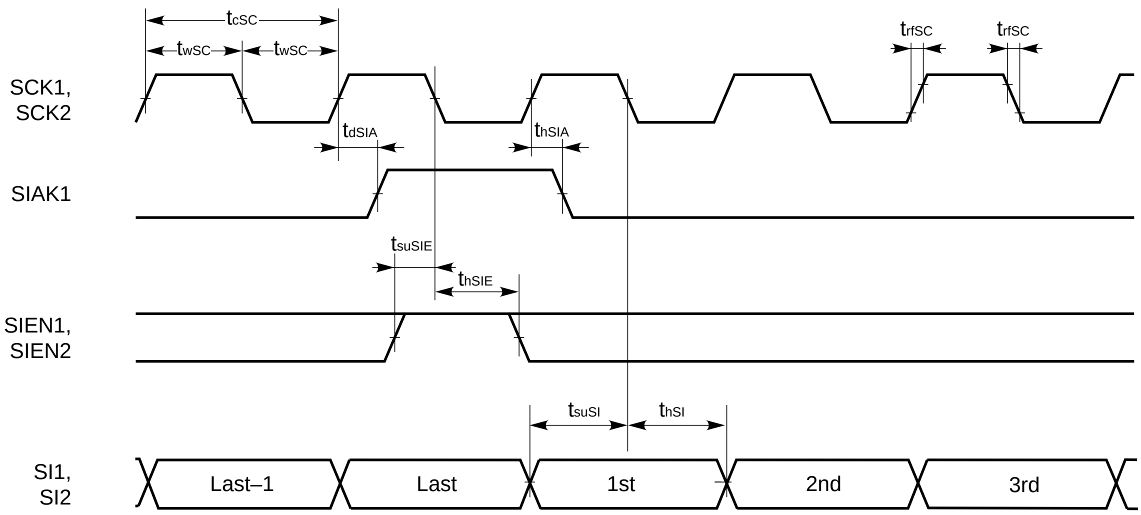
Serial input timing 1



Serial input timing 2 (during successive input)



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Host Interface

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{HRD}}$ delay time	t_{dHR}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
$\overline{\text{HRD}}$ width	t_{wHR}		60			ns
$\overline{\text{HCS}}$, HA0, HA1, read hold time	t_{hHCAR}		0			ns
$\overline{\text{HCS}}$, HA0, HA1 write hold time	t_{hHCAW}		0			ns
$\overline{\text{HRD}}$, $\overline{\text{HWR}}$ recovery time	t_{recHS}		60			ns
$\overline{\text{HWR}}$ delay time	t_{dHW}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
$\overline{\text{HWR}}$ width	t_{wHW}		60			ns
$\overline{\text{HWR}}$ hold time	t_{hHDW}		0			ns
$\overline{\text{HWR}}$ setup time	t_{suHDW}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{HRE}}$, $\overline{\text{HWE}}$ output delay time	t_{dHE}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
$\overline{\text{HRE}}$, $\overline{\text{HWE}}$ hold time	t_{hHE}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
$\overline{\text{HRD}}$ valid time	t_{vHDR}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
$\overline{\text{HRD}}$ hold time	t_{hHDR}		0			ns

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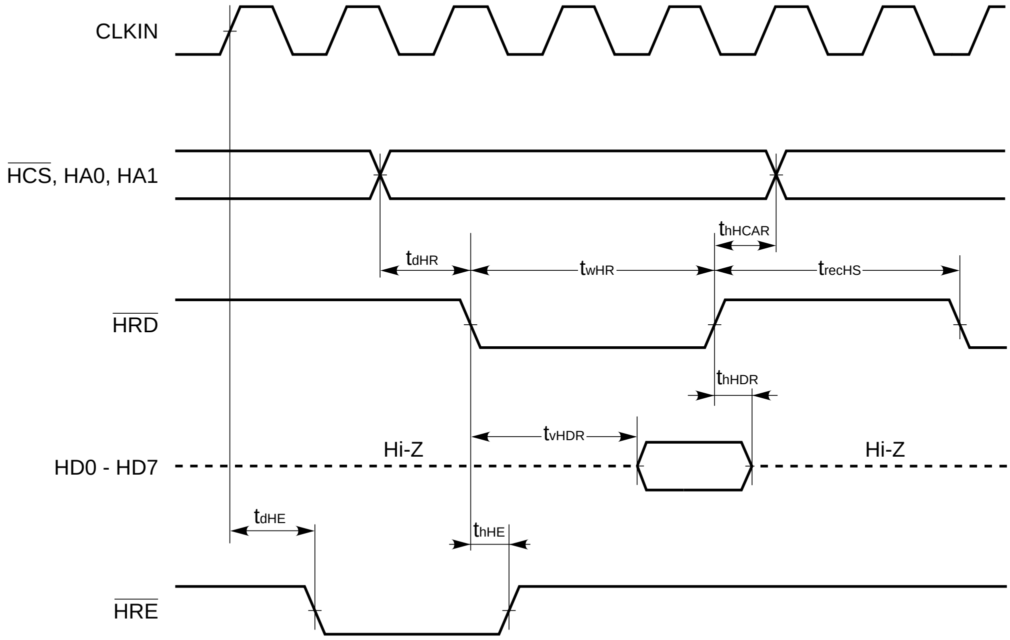
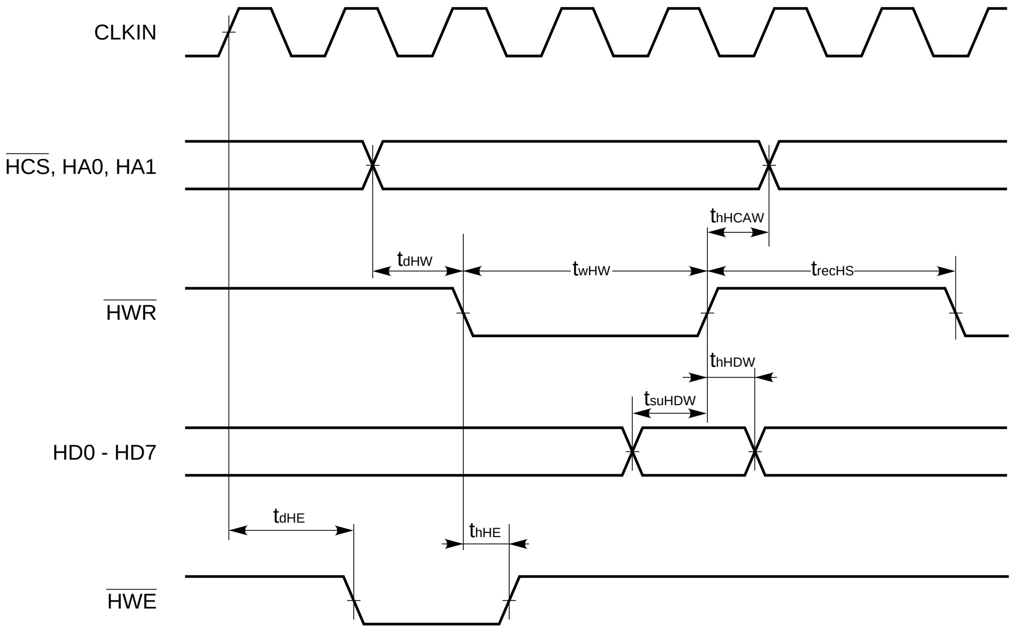
Host read interface timing



Host write interface timing



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General-purpose I/O Port

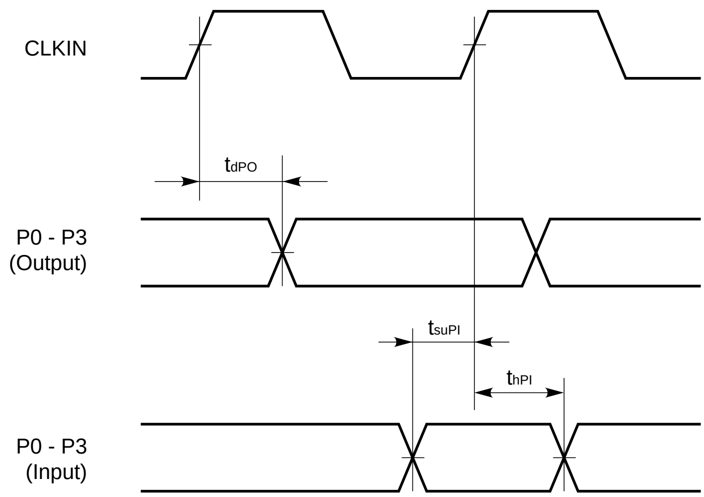
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Port input setup time	t_{suPI}		0			ns
Port input hold time	t_{hPI}	IV_{DD} = 1.8 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Port output delay time	t_{dPO}	IV_{DD} = 1.8 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns

General-purpose I/O port timing



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Debugging Interface (JTAG)

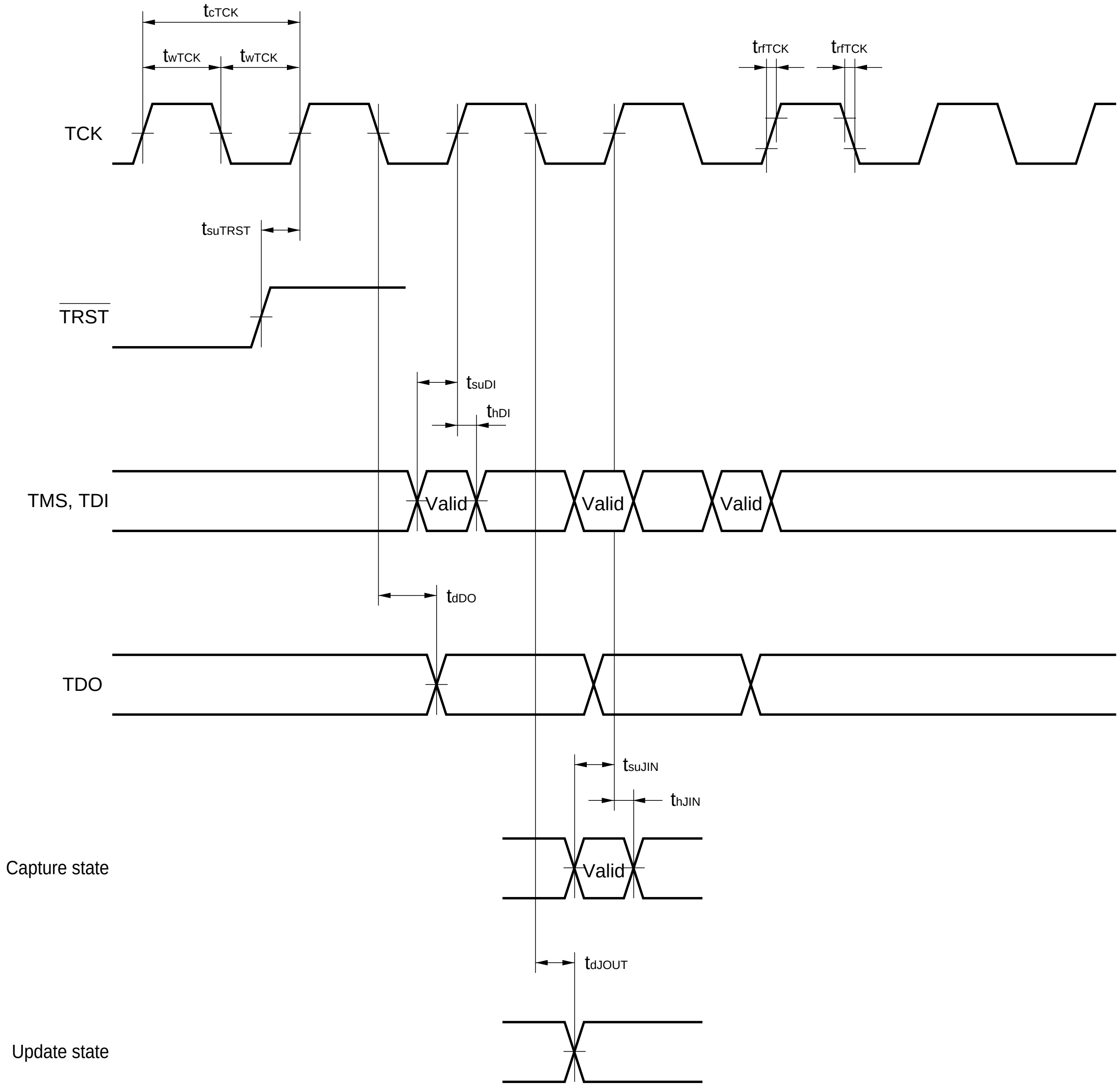
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK cycle time	t_{cTCK}		120			ns
TCK high-/low-level width	t_{wTCK}		50			ns
TCK rise/fall time	t_{rfTCK}				20	ns
TMS, TDI setup time	t_{suDI}	IV_{DD} = 1.8 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
TMS, TDI hold time	t_{hDI}	IV_{DD} = 1.8 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
Input pin setup time	t_{suJIN}	IV_{DD} = 1.8 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
Input pin hold time	t_{hJIN}	IV_{DD} = 1.8 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
$\overline{\text{TRST}}$ setup time	t_{suTRST}		100			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TDO output delay time	t_{dDO}	IV_{DD} = 1.8 to 2.7 V			25	ns
		IV_{DD} = 2.3 to 2.7 V			20	ns
Output pin output delay time	t_{dJOUT}	IV_{DD} = 1.8 to 2.7 V			25	ns
		IV_{DD} = 2.3 to 2.7 V			20	ns

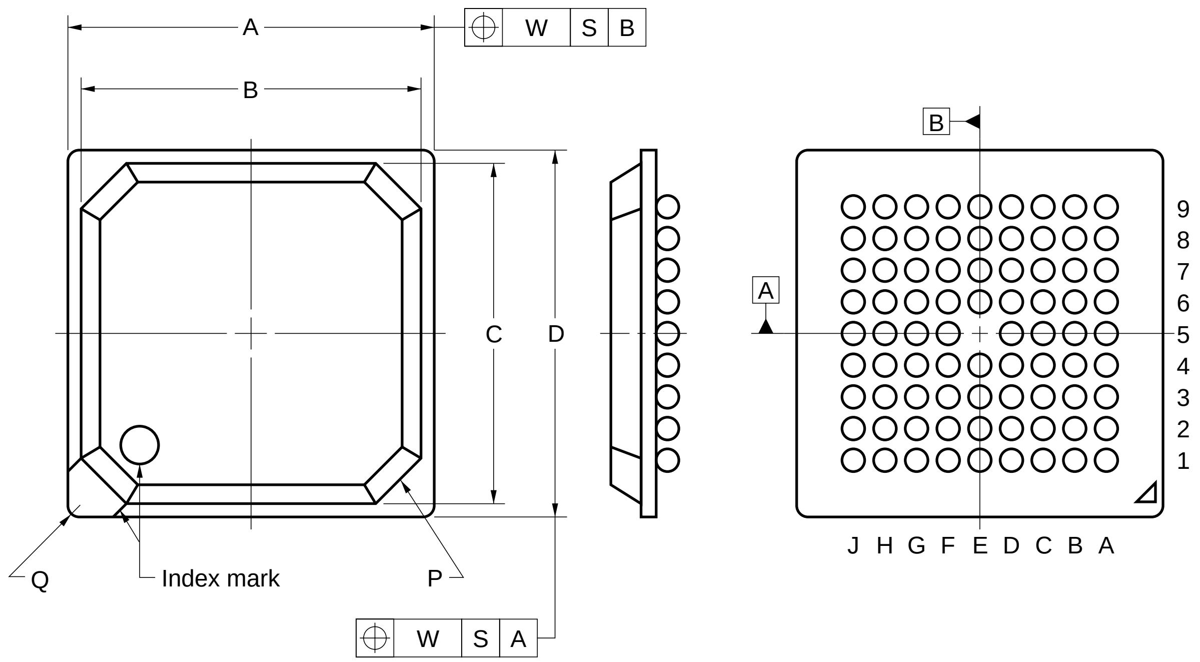
Debugging interface timing

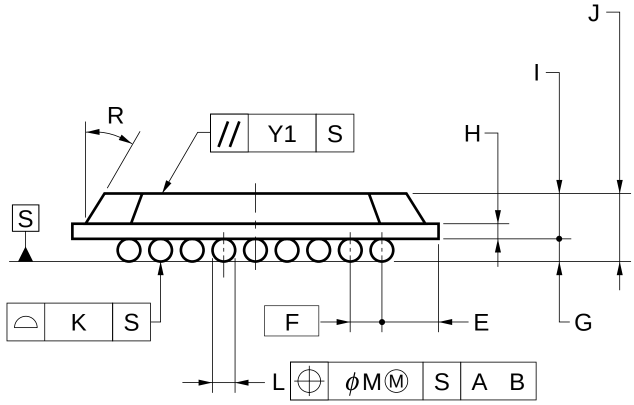


Remark For details of JTAG, refer to **IEEE1149.1**.

11. PACKAGE DRAWINGS

80-PIN PLASTIC FBGA (9x9)

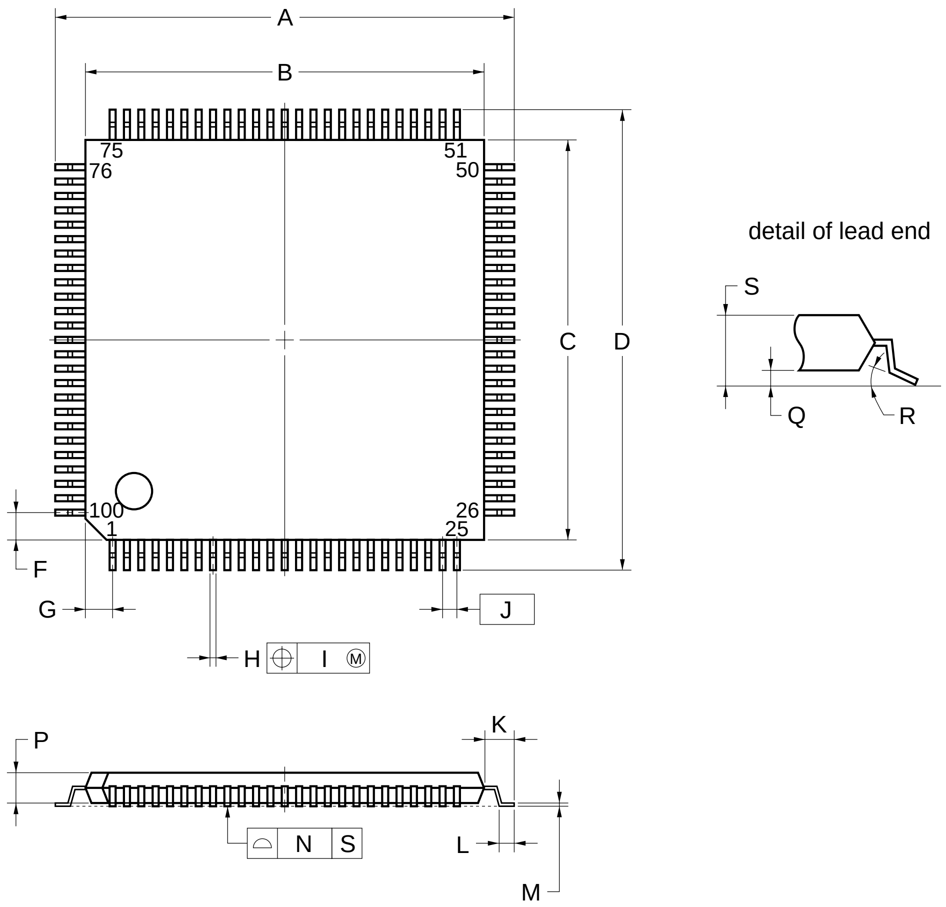




ITEM	MILLIMETERS
A	9.00±0.10
B	8.40
C	8.40
D	9.00±0.10
E	1.30
F	0.8 (T.P.)
G	0.35±0.1
H	0.36
I	0.96
J	1.31±0.15
K	0.10
L	$\phi 0.50^{+0.05}_{-0.10}$
M	0.08
P	C1.0
Q	R0.3
R	25°
W	0.20
Y1	0.20

S80F1-80-CN1-1

100-PIN PLASTIC TQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3°^{+7°}_{-3°}$
S	1.27 MAX.

S100GC-50-9EU-2

★ 12. RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder this product under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Surface mount type

μPD77113AF1-xxx-CN1: 80-pin plastic fine-pitch BGA (9 x 9)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 sec. Max. (at 210°C or higher). Count: two times or less Exposure limit: 3 days[Note] (after that prebake at 125°C for 10 hours)	IR30-103-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

μPD77114GC-xxx-9EU: 100-pin plastic TQFP (fine-pitch) (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher). Count: two times or less Exposure limit: 3 days[Note] (after that prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher). Count: two times or less Exposure limit: 3 days[Note] (after that prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store is at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating for pins).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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