LMU557/558
8 x 8-bit Parallel Multiplier

FEATURES

- 60 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces Am25S557/558, 54S557/558
- Fully Combinatorial, No Clocks Required
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP

DESCRIPTION

The **LMU557** and **LMU558** are high-speed, low power 8-bit parallel multipliers. They are pin for pin equivalents with 54S557 and 54S558 type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU557 and LMU558 produce the 16-bit product of two 8-bit signed or unsigned numbers in a single unclocked operation. Assertion of control inputs TCA and TCB indicate that the corresponding input value is in two's complement notation.

Provision is made for proper rounding for any combination of signed or unsigned inputs. The RU input to the LMU558 causes the product to be rounded to 8 bits of precision for unsigned or mixed mode multiplication. For multiplication of two signed operands, the RS input is used for rounding, and the most significant bit of the product is discarded. [It will be identical to the sign bit for all except the $(-2^8)\bullet(-2^8)$ case, which will cause overflow if the result MSB is not considered.]

The LMU557 internally produces the RU and RS controls from a single round input, denoted R. With R asserted, RS rounding occurs if either TCA or TCB is asserted, while RU rounding is implemented for TCA and TCB not asserted. This implementation frees a pin for control of the transparent output latch in the LMU557 via the G input.

Both the LMU557 and LMU558 offer three-state output buffers controlled by the $\overline{OE}$ input. The LMU557 has a 16-bit transparent latch between the multiplier array and the output drivers for flexibility in implementing pipelined systems. This latch is transparent when G is HIGH, and holds its state when G is LOW. In addition, both polarities of the result MSB (R15) are available as separate output pins to allow simple expansion to longer word lengths in signed multiplication.

LMU557/558 Block Diagram

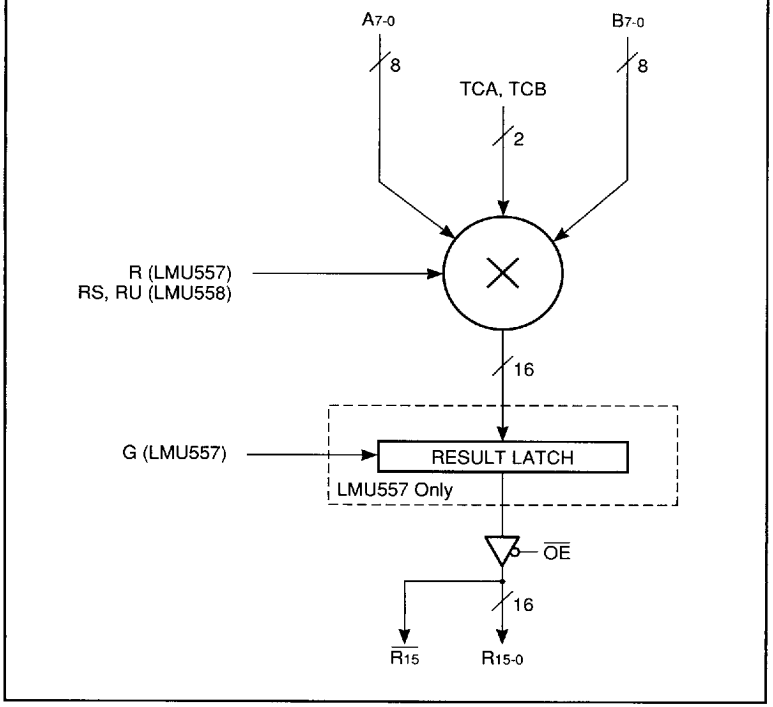


FIGURE 1A. INPUT FORMATS

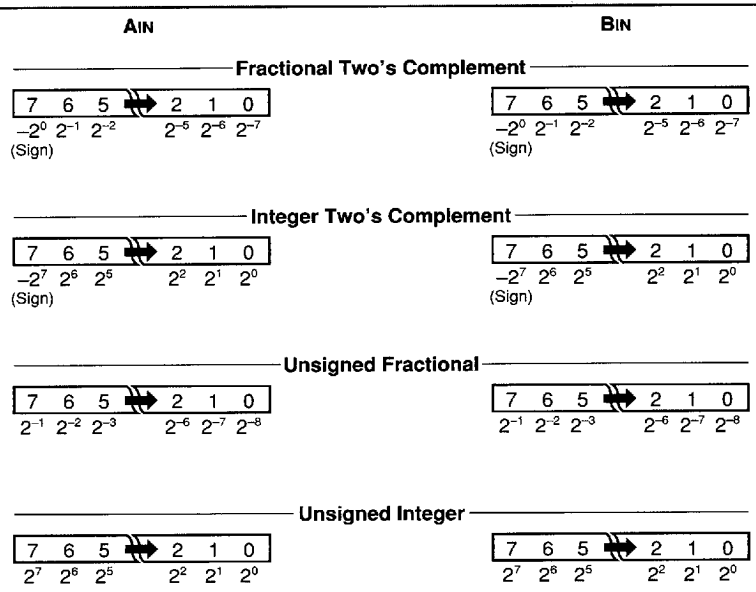
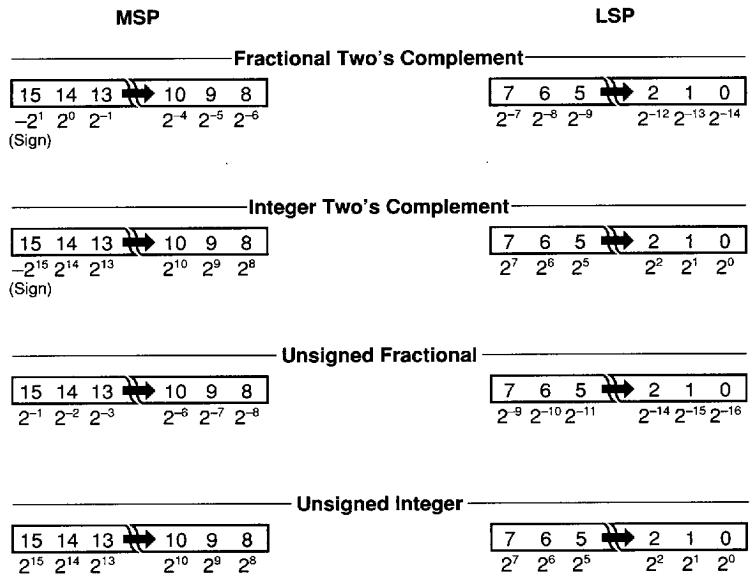


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		17	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

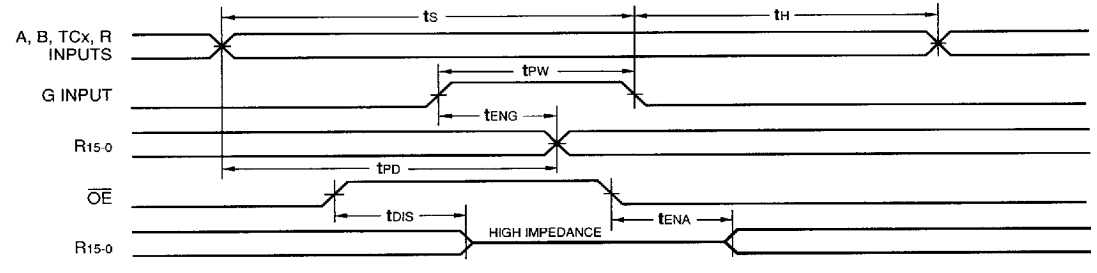
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU557/558–60 Min	LMU557/558–60 Max
t_{PD}	A, B, TCx, R Inputs to R_{15-8}, $\overline{R_{15}}$		60
t_{PD}	A, B, TCx, R Inputs to R_{7-0}		55
t_{PW}	G Pulse Width	15	
t_S	A, B, TCx, R Inputs to G Setup Time	45	
t_H	G to A, B, TCx, R Hold Time	0	
t_{ENG}	G Enable to Result		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		20

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU557/558–70 Min	LMU557/558–70 Max
t_{PD}	A, B, TCx, R Inputs to R_{15-8}, $\overline{R_{15}}$		70
t_{PD}	A, B, TCx, R Inputs to R_{7-0}		60
t_{PW}	G Pulse Width	20	
t_S	A, B, TCx, R Inputs to G Setup Time	55	
t_H	G to A, B, TCx, R Hold Time	0	
t_{ENG}	G Enable to Result		35
t_{ENA}	Three-State Output Enable Delay (Note 11)		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

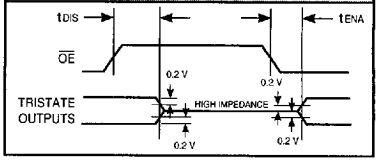
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 2. THRESHOLD LEVELS



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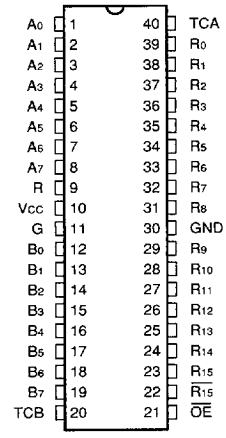
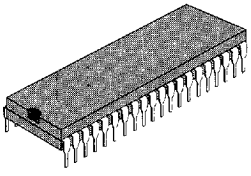
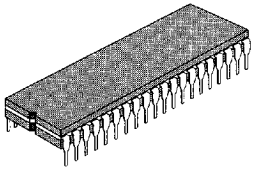
LMU557 — ORDERING INFORMATION

40-pin — 0.6" wide



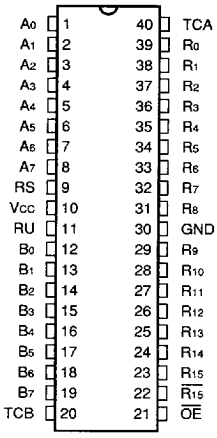


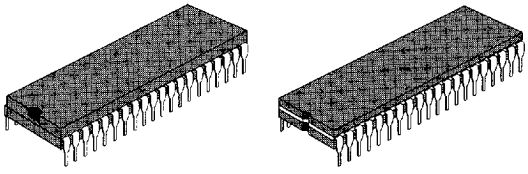


Speed	Plastic DIP (P3)	Ceramic DIP (C11)		
	0°C to +70°C — COMMERCIAL SCREENING			
60 ns	LMU557PC60	LMU557CC60		
	–55°C to +125°C — COMMERCIAL SCREENING			
70 ns		LMU557CM70		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
70 ns		LMU557CMB70		

LMU558 — ORDERING INFORMATION

40-pin — 0.6" wide





Speed	Plastic DIP (P3)	Ceramic DIP (C11)		
	0°C to +70°C — COMMERCIAL SCREENING			
60 ns	LMU558PC60	LMU558CC60		
	–55°C to +125°C — COMMERCIAL SCREENING			
70 ns		LMU558CM70		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
70 ns		LMU558CMB70		