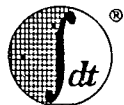


NOTICE

SEE ORDER OF DATA FOR ERRATA INFORMATION

T-46-23-12



Integrated Device Technology, Inc.

CMOS STATIC RAMS  
64K (8K x 8-BIT)

IDT7164S  
IDT7164L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select access time
  - Military: 20/25/30/35/45/55/70/85/100/120/150/200ns (max.)
  - Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in:
  - 28-pin 300 mil Plastic and Ceramic DIP
  - 28-pin 600 mil Plastic and Ceramic DIP
  - 28-pin 330 mil SOIC
  - 28-pin 300 mil SOJ
  - 28-pin LCC
  - 32-pin LCC
  - 32-pin PLCC
  - 28-pin CERPACK
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is listed on this function

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. Timing parameters have been specified to meet the demands of the fastest IDT79R3000 RISC processors.

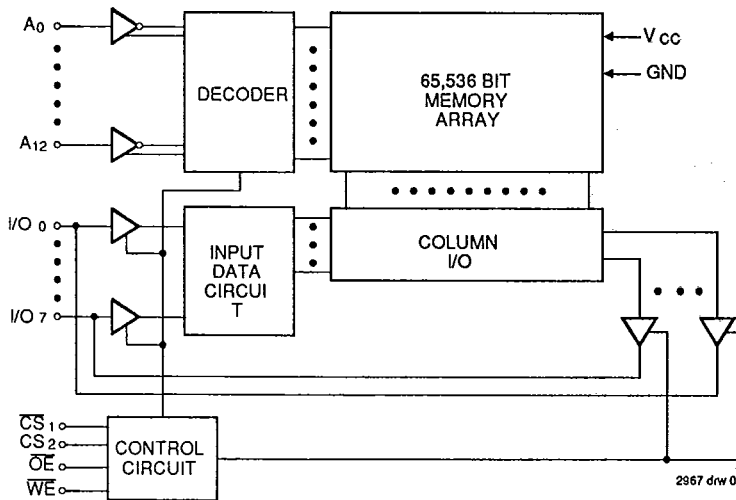
Address access times as fast as 15ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When CS<sub>1</sub> goes high or CS<sub>2</sub> goes low, the circuit will automatically go to, and remain in, a low-power stand by mode. In the full standby mode, the low-power device typically consumes less than 30μW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin PLCC and LCC; and 28-pin LCC, providing high-level board packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

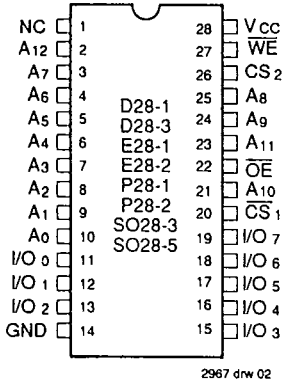
DECEMBER 1990

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

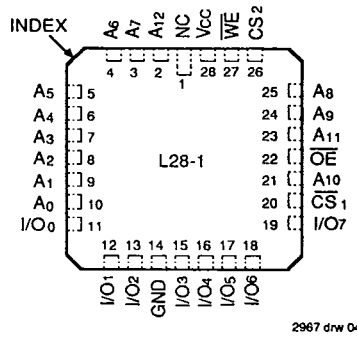
MILITARY AND COMMERCIAL TEMPERATURE RANGES

PIN CONFIGURATIONS

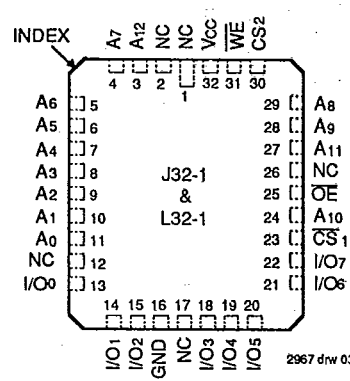
T-46-23-12



DIP/SOIC/SOJ  
TOP VIEW



28-PIN LCC  
TOP VIEW



32-PIN LCC/PLCC  
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0-A12	Address
I/O0-I/O7	Data Input/Output
CS1	Chip Select
CS2	Chip Select
WE	Write Enable
OE	Output Enable
GND	Ground
VCC	Power

2967 tbl 01

TRUTH TABLE<sup>(1,2)</sup>

WE	CS1	CS2	OE	I/O	Function
X	H	X	X	High-Z	Standby (ISB)
X	X	L	X	High-Z	Standby (ISB)
X	VHC	VHC or VLC	X	High-Z	Standby (ISB1)
X	X	VLC	X	High-Z	Standby (ISB1)
H	L	H	H	High-Z	Output Disable
H	L	H	L	DOUT	Read
L	L	H	X	DIN	Write

NOTE:

- CS2 will power-down CS1, but CS1 will not power-down CS2.
- H = VIH, L = VIL, X = don't care.

2967 tbl 02

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2967 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

NOTE:

- VIL (min.) = -3.0V for pulse width less than 20ns.

2967 tbl 06

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

**CAPACITANCE** (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

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NOTE: 2967 tbl 04  
1. This parameter is determined by device characterization, but is not production tested.

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	Power	7164S15 7164L15		7164S20 <sup>(4)</sup> 7164L20 <sup>(4)</sup>		7164S25 <sup>(4)</sup> 7164L25 <sup>(4)</sup>		7164S30 7164L30		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current, CS <sub>1</sub> = VIL, CS <sub>2</sub> = VIH, Outputs Open, VCC = Max., f = 0 <sup>(3)</sup>	S	110	—	100	110	90	110	90	100	mA
		L	100	—	90	100	80	100	80	90	
ICC2	Dynamic Operating Current CS <sub>1</sub> = VIL, CS <sub>2</sub> = VIH, Outputs Open, VCC = Max., f = fMAX <sup>(3)</sup>	S	180	—	170	180	170	180	160	170	mA
		L	150	—	150	160	150	160	140	150	
ISB	Standby Power Supply Current (TTL Level), CS <sub>1</sub> ≥ VIH, CS <sub>2</sub> ≤ VIL VCC = Max., Outputs Open, f = fMAX <sup>(3)</sup>	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
ISB1	Full Standby Power Supply Current (CMOS Level), f = 0 <sup>(3)</sup> 1. CS <sub>1</sub> ≥ VHC and CS <sub>2</sub> ≥ VHC 2. CS <sub>2</sub> ≤ VLC, VCC = Max.	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup> (Continued)**

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	Power	7164S35 7164L35		7164S45 7164L45		7164S55 7164L55		7164S70/85 <sup>(2)</sup> 7164L70/85 <sup>(2)</sup>		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current, CS <sub>1</sub> = VIL, CS <sub>2</sub> = VIH, Outputs Open, VCC = Max., f = 0 <sup>(3)</sup>	S	90	100	—	100	—	100	—	100	mA
		L	80	90	—	90	—	90	—	90	
ICC2	Dynamic Operating Current CS <sub>1</sub> = VIL, CS <sub>2</sub> = VIH, Outputs Open, VCC = Max., f = fMAX <sup>(3)</sup>	S	150	160	—	160	—	160	—	160	mA
		L	130	140	—	130	—	125	—	120	
ISB	Standby Power Supply Current (TTL Level), CS <sub>1</sub> ≥ VIH, CS <sub>2</sub> ≤ VIL VCC = Max., Outputs Open, f = fMAX <sup>(3)</sup>	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	3	—	5	—	5	
ISB1	Full Standby Power Supply Current (CMOS Level), f = 0 <sup>(3)</sup> 1. CS <sub>1</sub> ≥ VHC and CS <sub>2</sub> ≥ VHC 2. CS <sub>2</sub> ≤ VLC, VCC = Max.	S	15	20	—	15	—	20	—	20	mA
		L	0.2	1	—	0.2	—	1	—	1	

NOTES: 2967 tbl 07  
1. All values are maximum guaranteed values.  
2. Also available: 100, 120, 150 and 200ns military devices.  
3. At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.  
4. Military values for 20 and 25ns device are preliminary only.

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS

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VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT7164S		IDT7164L		Unit	
			Min.	Max.	Min.	Max.		
I <sub>L</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
I <sub>O</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS}_1 = V_{IH}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.		—	0.4	—	0.4	V
			I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.	—	0.5	—	0.5	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

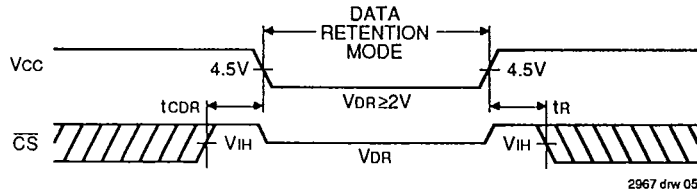
Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup> V <sub>CC</sub> @		Max. V <sub>CC</sub> @		Unit
				2.0v	3.0V	2.0V	3.0V	
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	—	2.0	—	—	—	—	V
I <sub>CCDR</sub>	Data Retention Current	MIL. COM'L.	—	10	15	200	300	μA
			—	10	15	60	90	
t <sub>CDR</sub> <sup>(3)</sup>	Chip Deselect to Data Retention Time	1. $\overline{CS}_1 \geq V_{HC}$ , $\overline{CS}_2 \geq V_{HC}$ 2. $\overline{CS}_2 \leq V_{LC}$	0	—	—	—	—	ns
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	—	—	ns
I <sub>L</sub>   <sup>(3)</sup>	Input Leakage Current		—	—	—	2	2	μA

NOTES:

- TA = +25°C.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed, but not tested.

2967 tkl 10

LOW V<sub>CC</sub> DATA RETENTION WAVEFORM



2967 drw 05

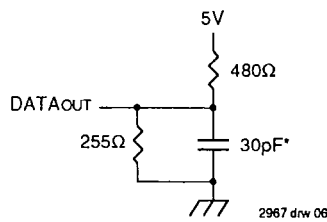


Figure 1. Output Load

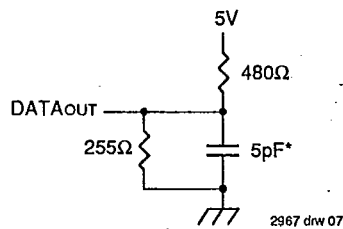


Figure 2. Output Load  
(for t<sub>CLZ</sub>1, 2, t<sub>OLZ</sub>, t<sub>CHZ</sub>1, 2, t<sub>OHZ</sub>, t<sub>LOW</sub>, t<sub>WHZ</sub>)

\*Includes scope and jig capacitances

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S15 <sup>(1)</sup> 7164L15 <sup>(1)</sup>		7164S20 <sup>(5)</sup> 7164L20 <sup>(5)</sup>		7164S25 <sup>(5)</sup> 7164L25 <sup>(5)</sup>		7164S30 7164L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
IRC	Read Cycle Time	15	—	20	—	25	—	30	—	ns
IAA	Address Access Time	—	15	—	19	—	25	—	29	ns
IACS1	Chip Select-1 Access Time <sup>(3)</sup>	—	15	—	20	—	25	—	30	ns
IACS2	Chip Select-2 Access Time <sup>(3)</sup>	—	20	—	25	—	30	—	35	ns
ICLZ1,2	Chip Select-1, 2 to Output in Low Z <sup>(4)</sup>	5	—	5	—	5	—	5	—	ns
IOE	Output Enable to Output Valid	—	7	—	8	—	12	—	15	ns
IOLZ	Output Enable to Output in Low Z <sup>(4)</sup>	3	—	3	—	3	—	3	—	ns
ICHZ1,2	Chip Select-1, 2 to Output in High Z <sup>(4)</sup>	—	8	—	9	—	13	—	13	ns
IOHZ	Output Disable to Output in High Z <sup>(4)</sup>	—	7	—	8	—	10	—	12	ns
IOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
IPU	Chip Select to Power Up Time <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
IPD	Chip Select to Power Down Time <sup>(4)</sup>	—	15	—	20	—	25	—	30	ns
<b>Write Cycle</b>										
IWC	Write Cycle Time	15	—	20	—	25	—	30	—	ns
ICW1,2	Chip Select to End of Write	14	—	15	—	18	—	22	—	ns
IAW	Address Valid to End of Write	14	—	15	—	18	—	22	—	ns
IAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
IWP	Write Pulse Width	14	—	15	—	21	—	23	—	ns
IWR1	Write Recovery Time ( $\overline{CS}_1, \overline{WE}$ )	0	—	0	—	0	—	0	—	ns
IWR2	Write Recovery Time (CS <sub>2</sub> )	5	—	5	—	5	—	5	—	ns
IWHZ	Write Enable to Output in High Z <sup>(4)</sup>	—	6	—	8	—	10	—	12	ns
IDW	Data to Write Time Overlap	8	—	10	—	13	—	13	—	ns
IDH1	Data Hold from Write Time ( $\overline{CS}_1, \overline{WE}$ )	0	—	0	—	0	—	0	—	ns
IDH2	Data Hold from Write Time (CS <sub>2</sub> )	5	—	5	—	5	—	5	—	ns
IOW	Output Active from End of Write <sup>(4)</sup>	5	—	5	—	5	—	5	—	ns

- NOTES:
- 0° to +70°C temperature range only.
  - 55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
  - Both chip selects must be active for the device to be selected.
  - This parameter is guaranteed, but not tested.
  - Military values for 20 and 25ns devices are preliminary only.

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IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (Continued) (V<sub>CC</sub> = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45 <sup>(2)</sup> 7164L45 <sup>(2)</sup>		7164S55 <sup>(2)</sup> 7164L55 <sup>(2)</sup>		7164S70 <sup>(2)</sup> /85 <sup>(2)</sup> 7164L70 <sup>(2)</sup> /85 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		<b>Read Cycle</b>								
IRC	Read Cycle Time	35	—	45	—	55	—	70/85	—	ns
IAA	Address Access Time	—	35	—	45	—	55	—	70/85	ns
IACS1	Chip Select-1 Access Time <sup>(3)</sup>	—	35	—	45	—	55	—	70/85	ns
IACS2	Chip Select-2 Access Time <sup>(3)</sup>	—	40	—	45	—	55	—	70/85	ns
ICLZ1,2	Chip Select-1, 2 to Output in Low Z <sup>(4)</sup>	5	—	5	—	5	—	5	—	ns
IOE	Output Enable to Output Valid	—	18	—	25	—	30	—	35/40	ns
IOLZ	Output Enable to Output in Low Z <sup>(4)</sup>	3	—	3	—	3	—	3	—	ns
ICHZ1,2	Chip Select-1, 2 to Output in High Z <sup>(4)</sup>	—	15	—	20	—	25	—	30/35	ns
IOHZ	Output Disable to Output in High Z <sup>(4)</sup>	—	15	—	20	—	25	—	30/35	ns
IOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
IPU	Chip Select to Power Up Time <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
IPD	Chip Select to Power Down Time <sup>(4)</sup>	—	35	—	45	—	55	—	70/85	ns
<b>Write Cycle</b>										
IWC	Write Cycle Time	35	—	45	—	55	—	70/85	—	ns
ICW1,2	Chip Select to End of Write	25	—	33	—	50	—	60/75	—	ns
IAW	Address Valid to End of Write	25	—	33	—	50	—	60/75	—	ns
IAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
IWP	Write Pulse Width	25	—	25	—	50	—	60/75	—	ns
IWR1	Write Recovery Time ( $\overline{CS}_1, \overline{WE}$ )	0	—	0	—	0	—	0	—	ns
IWR2	Write Recovery Time (CS <sub>2</sub> )	5	—	5	—	5	—	5	—	ns
IWHZ	Write Enable to Output in High Z <sup>(4)</sup>	—	14	—	18	—	25	—	30/35	ns
IDW	Data to Write Time Overlap	15	—	20	—	25	—	30/35	—	ns
IDH1	Data Hold from Write Time ( $\overline{CS}_1, \overline{WE}$ )	0	—	0	—	0	—	0	—	ns
IDH2	Data Hold from Write Time (CS <sub>2</sub> )	5	—	5	—	5	—	5	—	ns
IOW	Output Active from End of Write <sup>(4)</sup>	5	—	5	—	5	—	5	—	ns

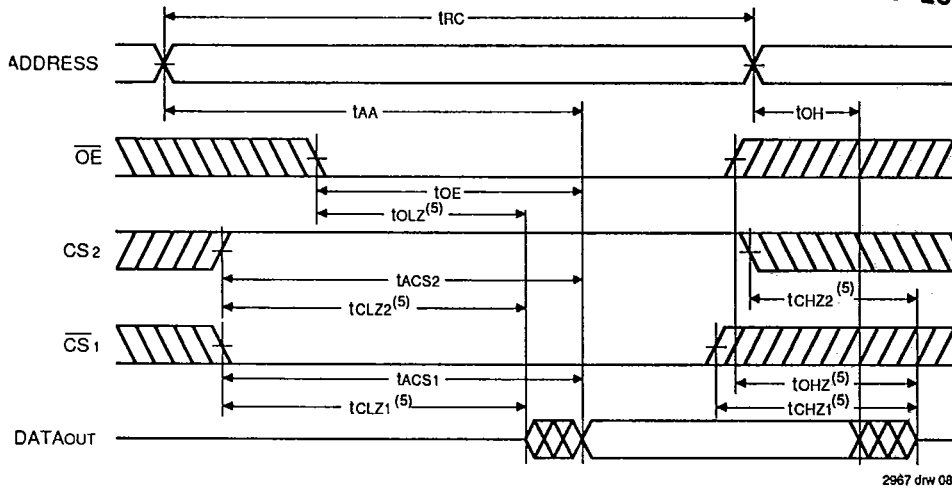
## NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only. Also available: 100, 120, 150, and 200ns military devices.
- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed, but not tested.

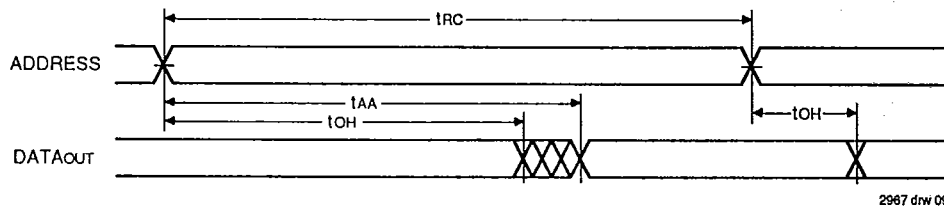
2967 (b) 11

TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>

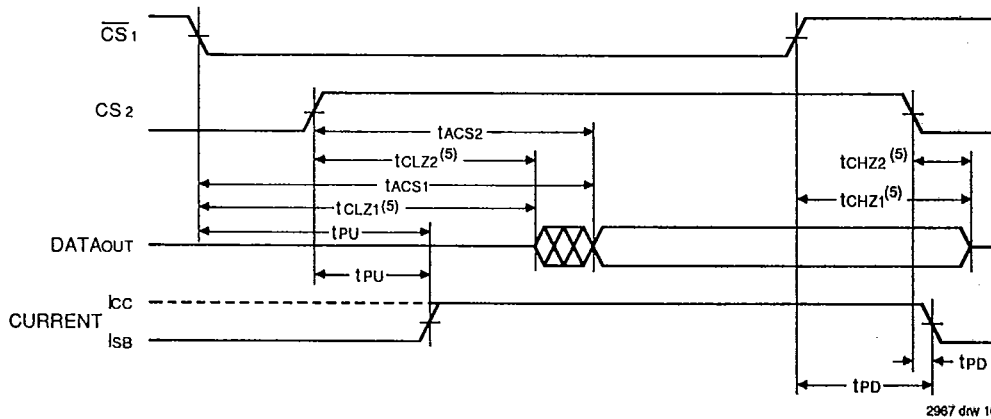
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TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>

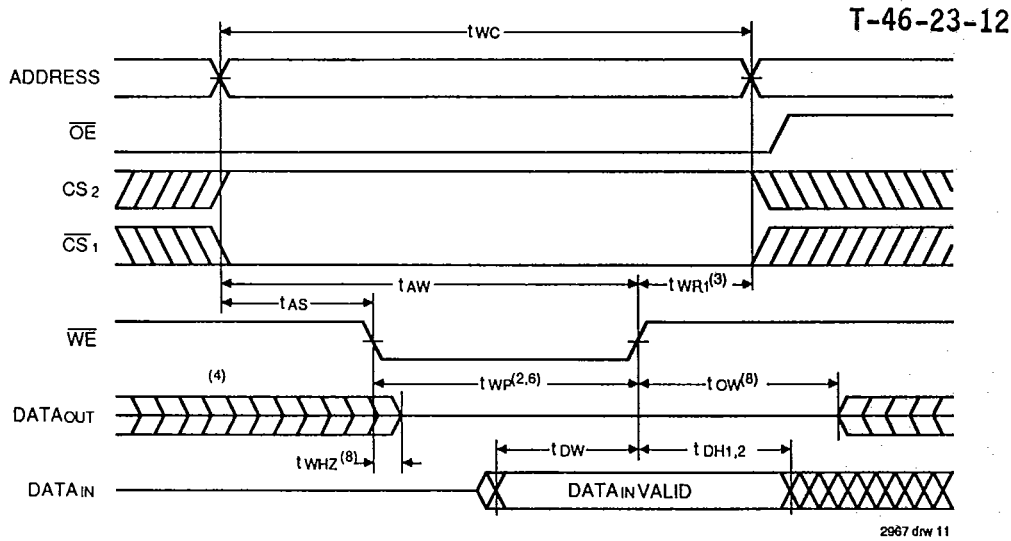


TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>

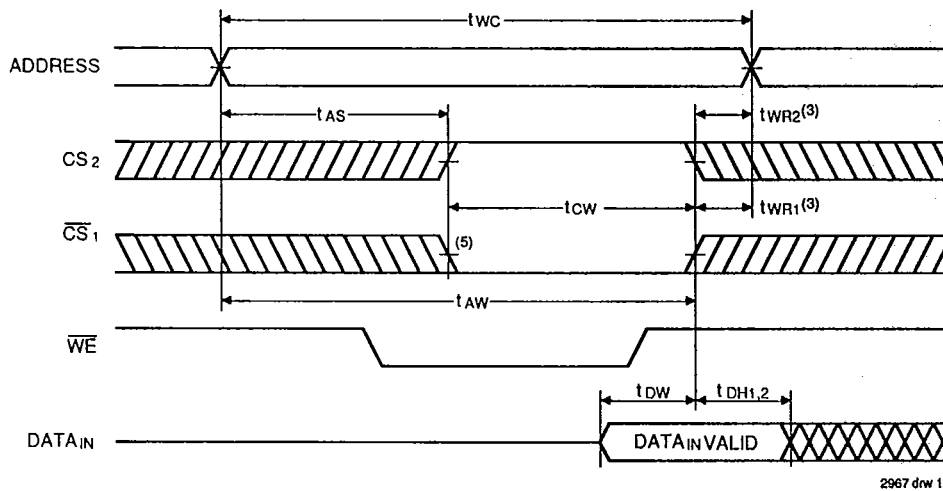


- NOTES:
1.  $\overline{WE}$  is high for read cycle.
  2. Device is continuously selected,  $\overline{CS1} = V_{IL}$ ,  $CS2 = V_{IH}$ .
  3. Address valid prior to or coincident with  $\overline{CS1}$  transition low and  $CS2$  transition high.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 200mV$  from steady state.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1)</sup>**



**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1)</sup>**



**NOTES:**

1.  $\overline{WE}$ ,  $\overline{CS1}$  or  $CS2$  must be inactive during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{WE}$ , a low  $\overline{CS1}$  and a high  $CS2$ .
3.  $t_{WR1,2}$  is measured from the earlier of  $\overline{CS1}$  or  $\overline{WE}$  going high or  $CS2$  going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the  $\overline{CS1}$  low transition or  $CS2$  high transition occurs simultaneously with or after the  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6. If  $\overline{OE}$  is low during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WHZ} + t_{OW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is high during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .
7.  $DATA_{OUT}$  is the same phase of write data of this write cycle.
8. Transition is measured  $\pm 200mV$  from steady state.

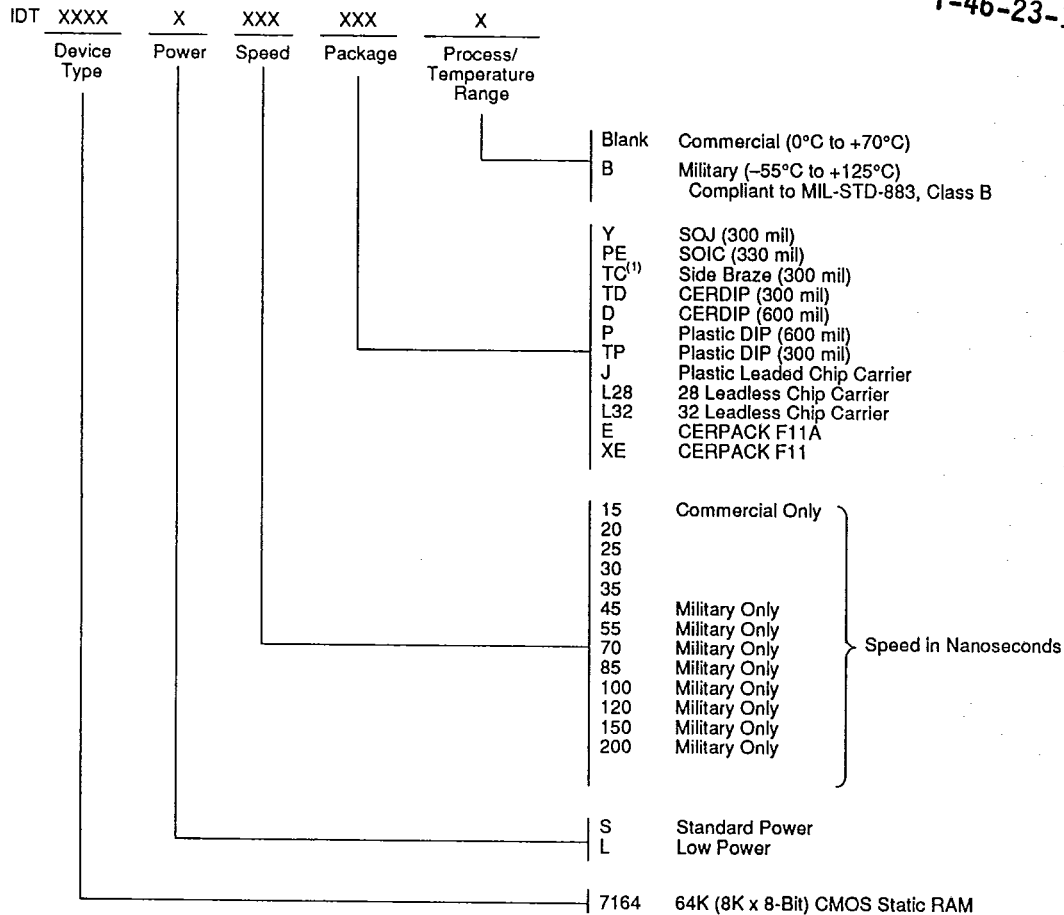


IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ORDERING INFORMATION

T-46-23-12



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NOTE:

1. TC package will be replaced by TD.