
BIC701M

Bias Controlled Monolithic IC
VHF/UHF RF Amplifier

HITACHI

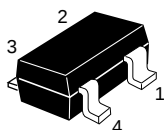
ADE-208-703C (Z)
4th. Edition
Nov. 1, 1998

Features

- Bias Controlled Monolithic IC (No external DC biasing voltage on gate1.);
To reduce using parts cost & PC board space.
- High gain;
PG = 27 dB typ. (at f = 200 MHz), PG = 21.5 dB typ. (at f = 900 MHz)
- Low noise;
NF = 1.1 dB typ. (at f = 200 MHz), NF = 1.75 dB typ. (at f = 900 MHz)
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4(SOT-143mod)

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1. Marking is "AZ-".

2. BIC701M is individual type number of HITACHI BICMIC.

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 – 0	V
Gate2 to source voltage	V_{G2S}	+6 – 0	V
Drain current	I_D	20	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

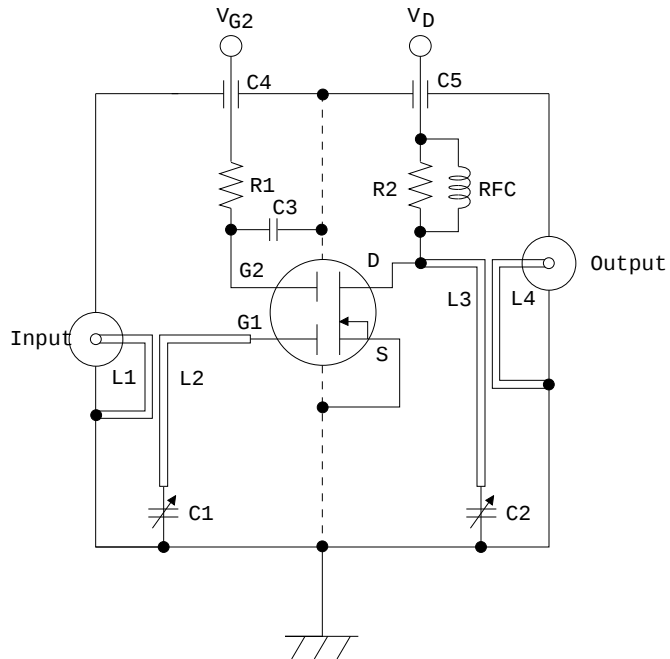
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$ $V_{G2S} = 0, V_{G1} = \text{open}$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A$ $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10\mu A$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5V$ $V_{G1S} = V_{DS} = 0$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5V, I_D = 100\mu A$ $V_{G1} = \text{open}$
Drain current	$I_{DS(op)}$	7	10	13	mA	$V_{DS} = 5V, V_{G2S} = 4V$ $V_{G1} = \text{open}$
Forward transfer admittance	$ y_{fs} $	22	27	32	mS	$V_{DS} = 5V, I_D = 10mA$ $V_{G2S} = 4V, f = 1kHz$
Input capacitance	C_{iss}	1.6	2.0	2.3	pF	$V_{DS} = 5V, V_{G2S} = 4V$
Output capacitance	C_{oss}	0.6	1.0	1.4	pF	$V_{G1} = \text{open}$
Reverse transfer capacitance	C_{rss}	—	0.024	0.05	pF	$f = 1MHz$
Power gain	PG1	23	27	—	dB	$V_{DS} = 5V, V_{G2S} = 4V$ $V_{G1} = \text{open}$
Noise figure	NF1	—	1.1	1.6	dB	$f = 200MHz$
Power gain	PG2	17	21.5	—	dB	$V_{DS} = 5V, V_{G2S} = 4V$ $V_{G1} = \text{open}$
Noise figure	NF2	—	1.75	2.3	dB	$f = 900MHz$

The diagram shows a two-terminal device with two gates, Gate 1 and Gate 2. Gate 2 is connected to a voltage source V_{G2} . Gate 1 is connected to a voltage source V_{G1} through a resistor R_G . The drain and source terminals are connected to a current source I_D and ground, respectively. The device is represented by a central rectangular block with four terminals: Gate 2, Gate 1, Drain, and Source.

Unit @Resistance @(Ω)
 @@ Capacitance @(F)

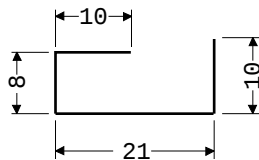
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900MHz Power Gain, Noise Test Circuit

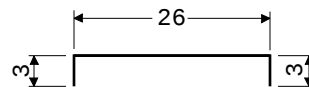


C1, C2 F Variable Capacitor i10pF MAX)
 C3 F Disk Capacitor i1000pF)
 C4, C5 F Air Capacitor i1000pF)
 R1 F 47 k Ω
 R2 F 4.7 k Ω

L1 F

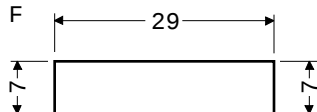


L2 F

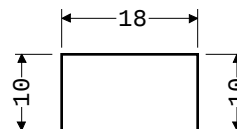


i 0.1mm Copper wire j
Unit Fmm

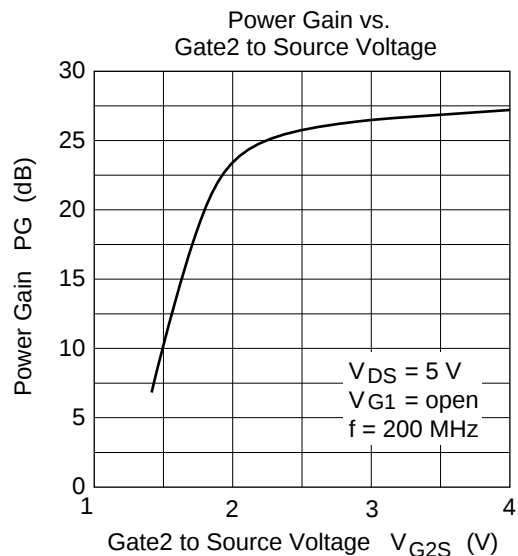
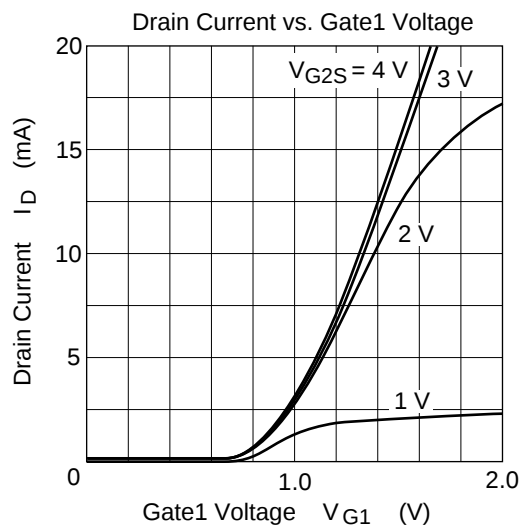
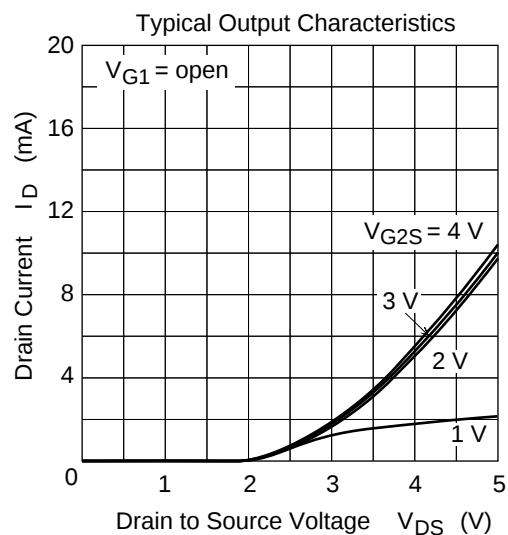
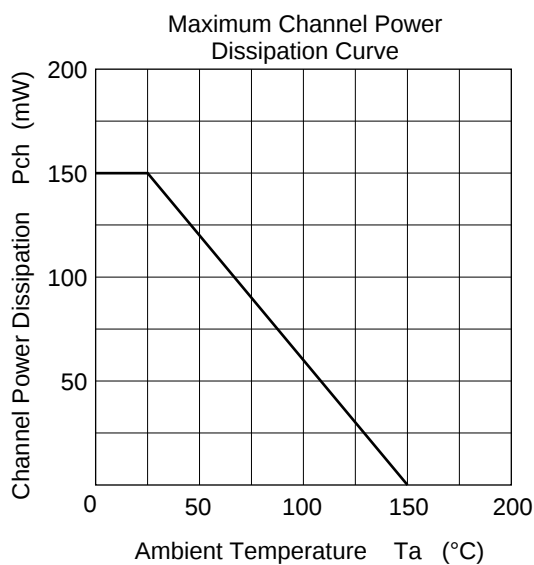
L3 F

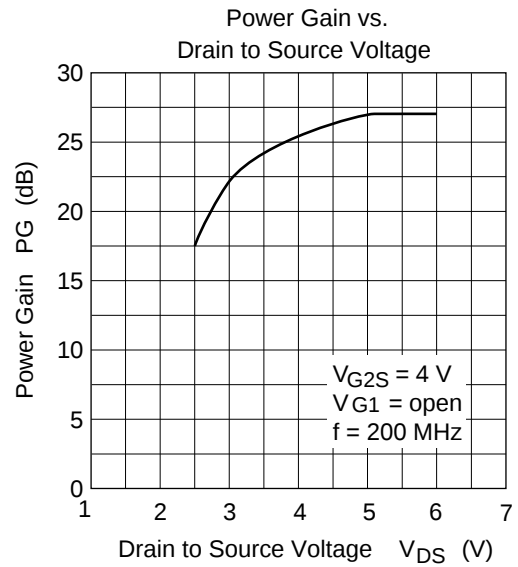
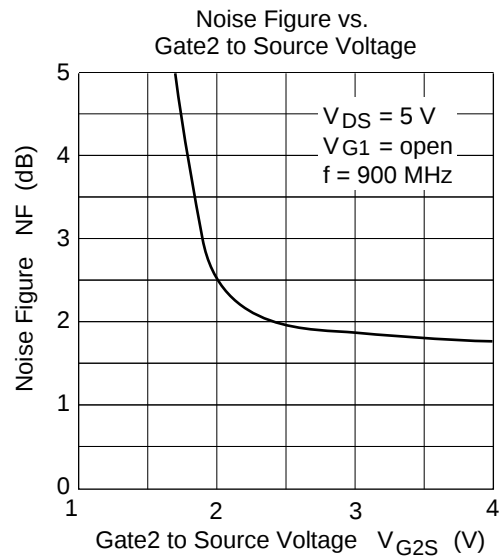
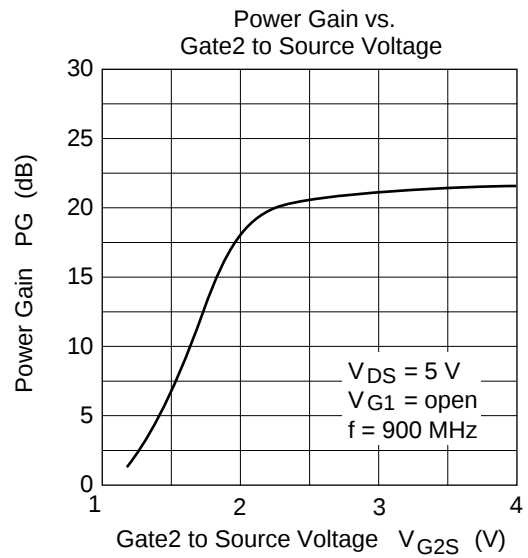
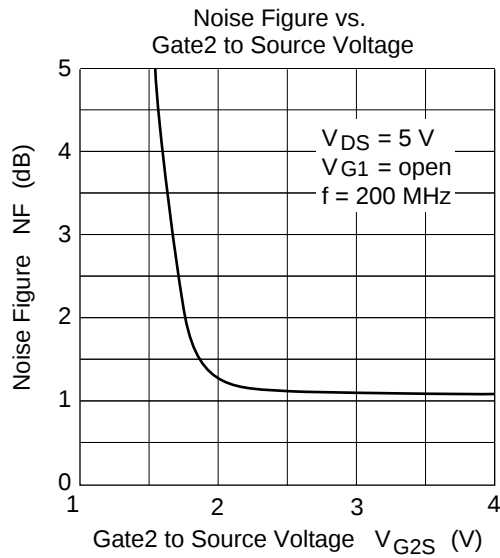


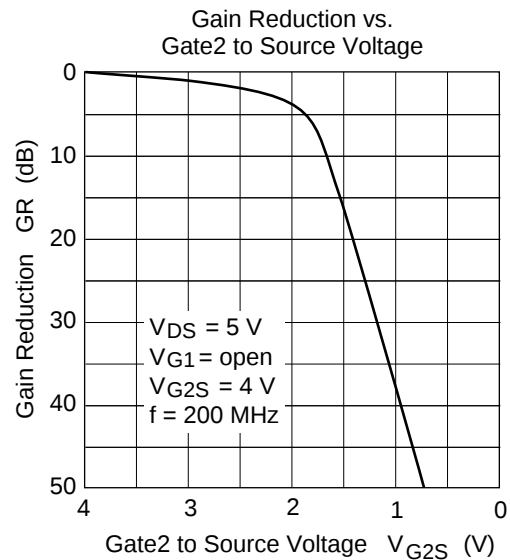
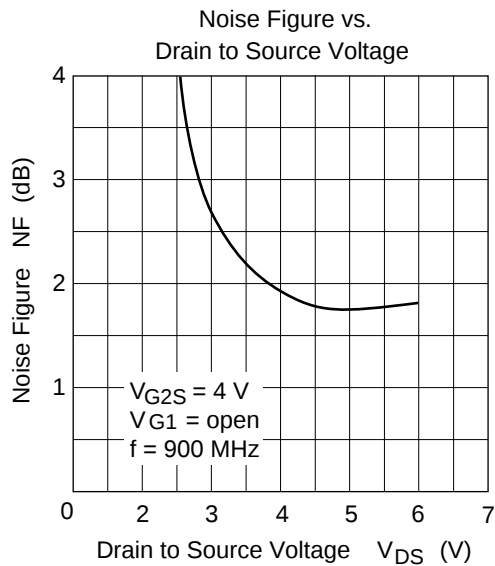
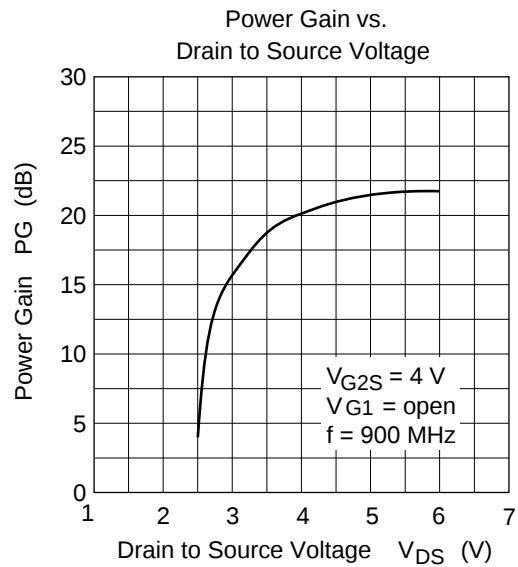
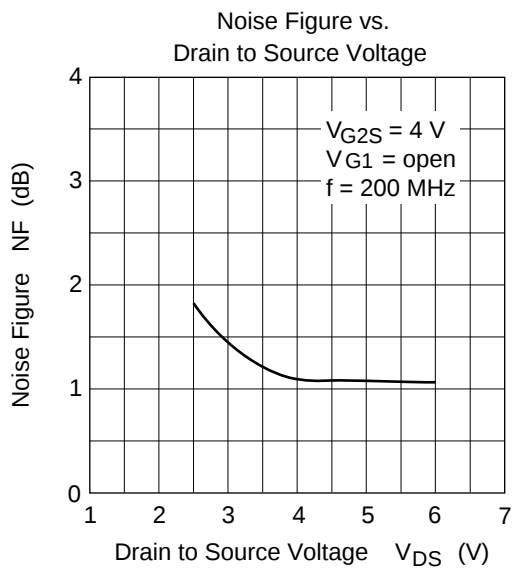
L4 F

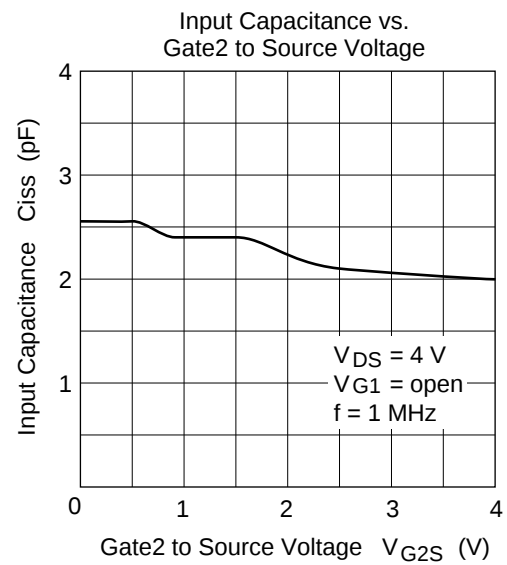
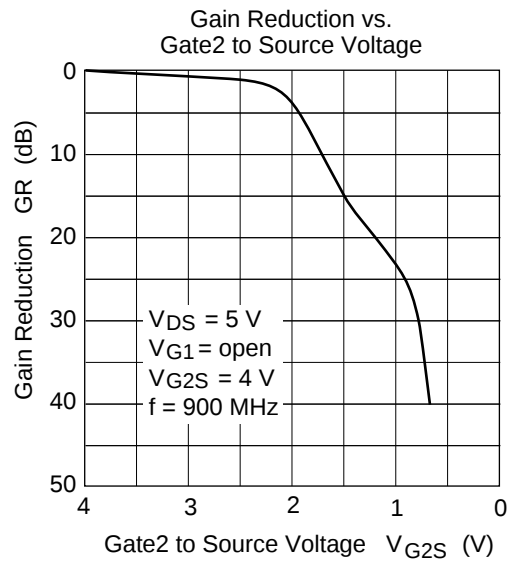


RFC F 0.1mm Copper wire with enamel 4 turns inside di

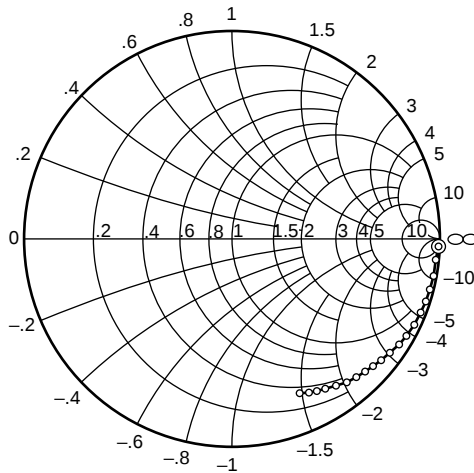






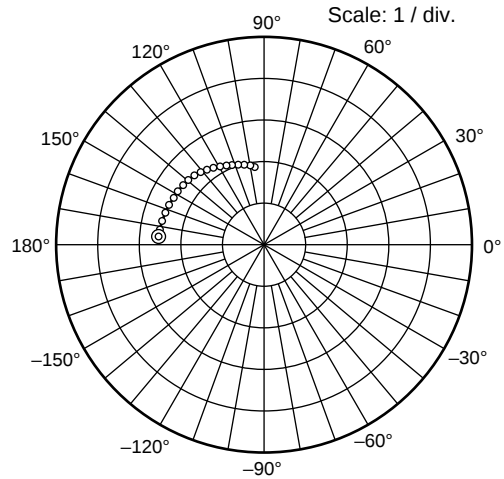


S11 Parameter vs. Frequency



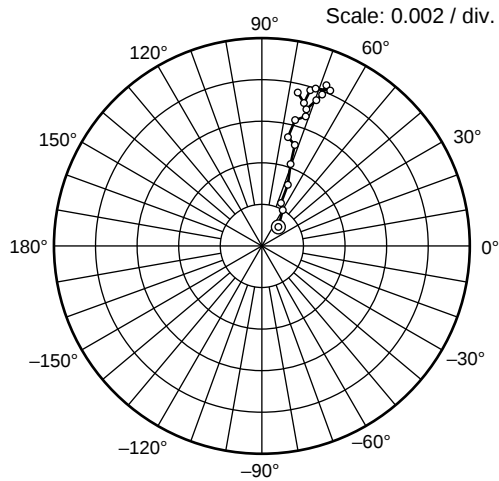
Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$, $Z_0 = 50\ \Omega$
 50 ' 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency



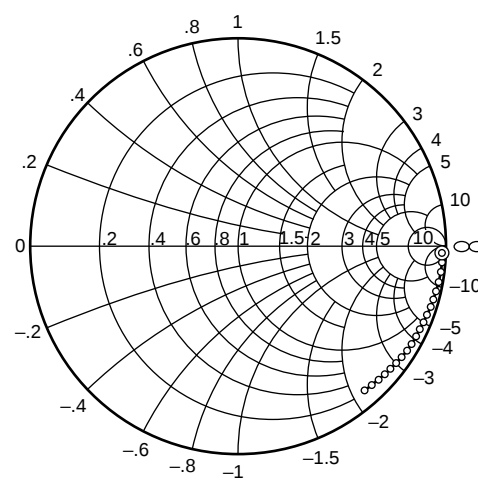
Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$, $Z_0 = 50\ \Omega$
 50 ' 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency



Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$, $Z_0 = 50\ \Omega$
 50 ' 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



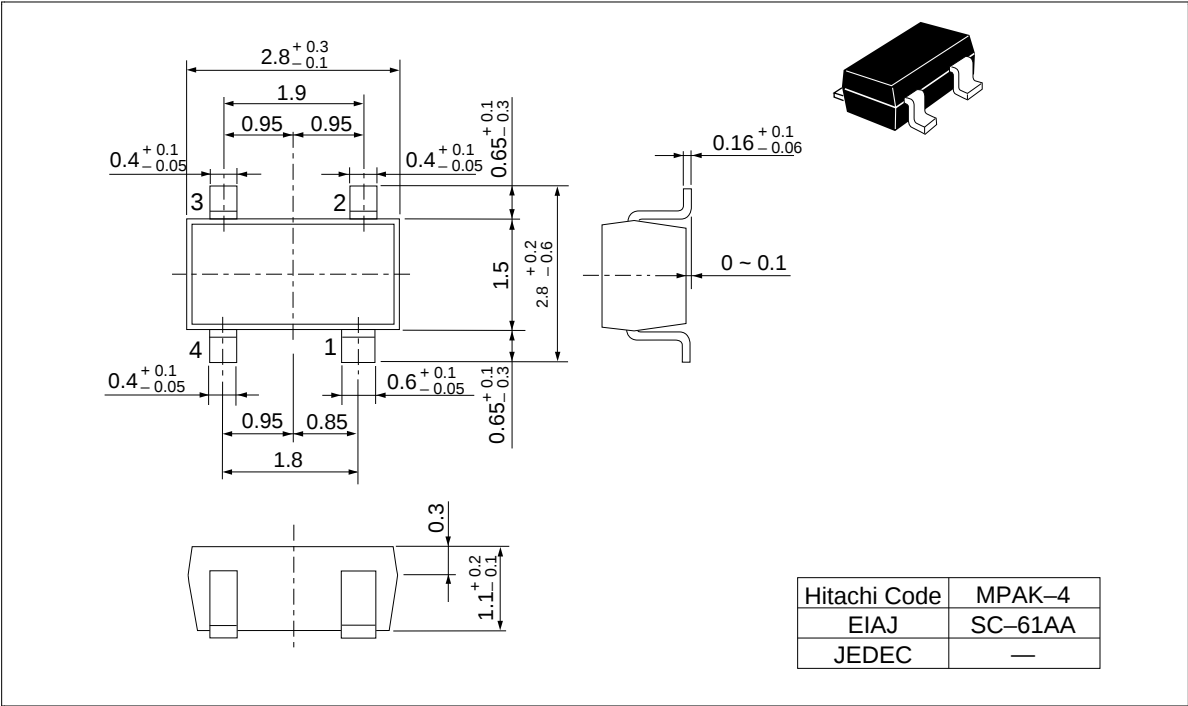
Test Condition : $V_{DS} = 5\text{ V}$, $V_{G1} = \text{open}$
 $V_{G2S} = 4\text{ V}$, $Z_0 = 50\ \Omega$
 50 ' 1000 MHz (50 MHz step)

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Sparameter ($V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$, $V_{G1} = \text{open}$, $Z_0 = 50\Omega$)

f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.994	-3.1	2.54	175.5	0.00132	50.0	0.978	-2.4
100	0.993	-6.6	2.52	171.0	0.00201	59.8	0.981	-5.1
150	0.988	-10.5	2.51	166.4	0.00228	66.1	0.979	-7.5
200	0.983	-14.1	2.49	161.6	0.00323	66.7	0.979	-10.1
250	0.977	-17.9	2.46	157.2	0.00420	70.2	0.976	-12.7
300	0.970	-21.8	2.43	152.8	0.00514	71.9	0.974	-15.1
350	0.963	-25.4	2.40	148.6	0.00532	76.1	0.971	-17.6
400	0.951	-28.8	2.37	143.7	0.00629	74.2	0.969	-20.1
450	0.943	-32.4	2.34	139.4	0.00665	70.8	0.966	-22.4
500	0.933	-35.4	2.29	135.1	0.00700	71.6	0.962	-24.9
550	0.918	-39.1	2.25	131.1	0.00756	69.3	0.958	-27.3
600	0.906	-42.0	2.21	127.2	0.00790	68.1	0.954	-29.7
650	0.895	-45.5	2.17	123.0	0.00836	67.6	0.951	-32.2
700	0.882	-48.7	2.13	119.4	0.00820	66.1	0.946	-34.4
750	0.879	-51.1	2.09	115.6	0.00818	65.9	0.942	-36.8
800	0.860	-54.6	2.05	111.7	0.00819	66.5	0.938	-39.2
850	0.845	-58.3	2.02	107.8	0.00798	70.7	0.933	-41.5
900	0.835	-60.7	1.96	104.2	0.00787	71.9	0.929	-43.8
950	0.827	-63.3	1.92	100.5	0.00727	73.1	0.924	-46.2
1000	0.812	-66.4	1.88	97.0	0.00758	75.6	0.919	-48.5

Package Dimensions (Unit: mm)



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