512MB- 64Mx64 SDRAM, UNBUFFERED

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3 volt ± 0.3v Power Supply
- 144 Pin SO-DIMM JEDEC

DESCRIPTION

The WED3DG6466V is a 64Mx64 synchronous DRAM module which consists of eight 64Mx8 SDRAM components in TSOP- 11 package, and one 2K EEPROM in an 8- pin TSSOP package for Serial Presence Detect which are mounted on a 144 Pin SO-DIMM multilayer FR4 Substrate.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PINOUT

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	VCC	102	VCC
7	DQ2	8	DQ34	55	VSS	56	VSS	103	A6	104	A7
9	DQ3	10	DQ35	57	**NC**	58	**NC**	105	A8	106	BA0
11	VCC	12	VCC	59	**NC**	60	**NC**	107	VSS	108	VSS
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	VCC	64	VCC	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS\	66	CAS\	113	VCC	114	VCC
19	DQ7	20	DQ39	67	WE\	68	**NC**	115	DQM2	116	DQM6
21	VSS	22	VSS	69	**CS0**	70	A12	117	DQM3	118	DQM7
23	DQM0	24	DQM4	71	**NC**	72	**NC**	119	VSS	120	VSS
25	DQM1	26	DQM5	73	NC	74	CLK1	121	DQ24	122	DQ56
27	VCC	28	VCC	75	VSS	76	VSS	123	DQ25	124	DQ57
29	A0	30	A3	77	**NC**	78	**NC**	125	DQ26	126	DQ58
31	A1	32	A4	79	**NC**	80	**NC**	127	DQ27	128	DQ59
33	A2	34	A5	81	VCC	82	VCC	129	VCC	130	VCC
35	VSS	36	VSS	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	VSS	92	VSS	139	VSS	140	VSS
45	VCC	46	VCC	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	VCC	144	VCC

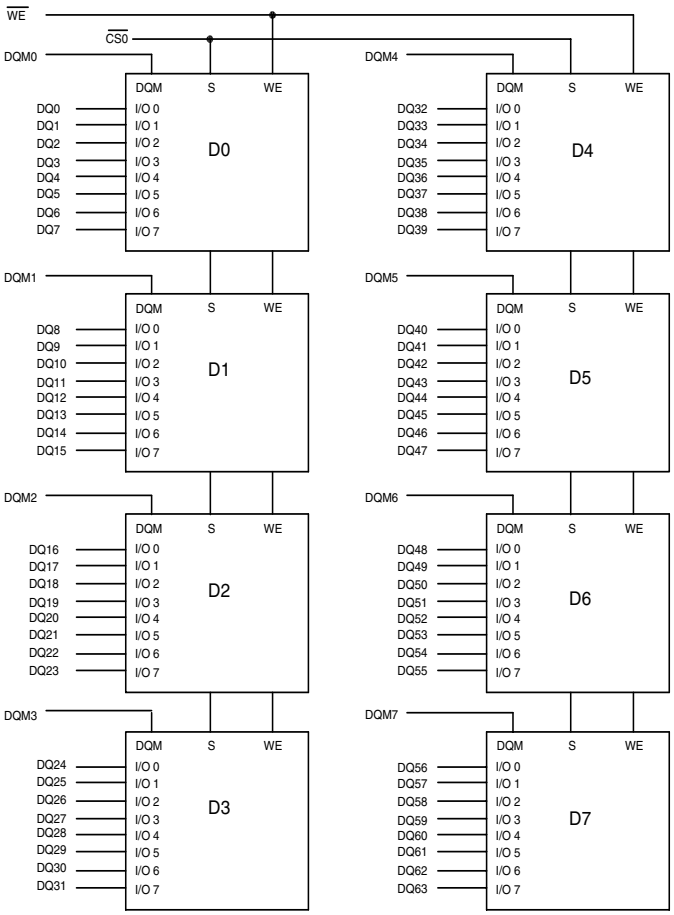
PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0,CLK1	Clock input
CKE0	Clock Enable input
$\overline{CS0}$	Chip select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0-7	DQM
VDD	Power Supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

** These pins should be NC in the system which does not support SPD.

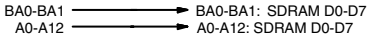
White Electronic Designs Corp reserves the right to change products or specifications without notice.

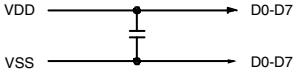
FUNCTIONAL BLOCK DIAGRAM

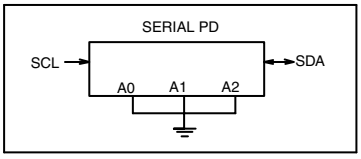


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

*CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CLK0	4 SDRAMS
*CLK1	4 SDRAMS







White Electronic Designs Corp reserves the right to change products or specifications without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to VSS	VIN, Vout	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	8	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: VSS = 0V, TA = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input Low Voltage	VIL	-0.3	—	0.8	V	2
Output High Voltage	VOH	2.4	—	—	V	IOH= -2mA
Output Low Voltage	VOL	—	—	0.4	V	IOL= -2mA
Input Leakage Current	ILI	-10	—	10	µA	3

Note: 1. VIH (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(TA = 23°C, f = 1MHz, VDD = 3.3V, VREF=1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12)	CIN1	-	15	pF
Input Capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN2	-	15	pF
Input Capacitance (CKE0)	CIN3	-	15	pF
Input Capacitance (CLK0)	CIN4	-	20	pF
Input Capacitance ($\overline{CS0}$)	CIN5	-	15	pF
Input Capacitance (DQM0-DQM7)	CIN6	-	15	pF
Input Capacitance (BA0-BA1)	CIN7	-	15	pF
Data input/output capacitance (DQ0-DQ63)	Cout	-	22	pF
Data input/output capacitance (CB0-7)	Cout 1	-	22	pF

White Electronic Designs Corp reserves the right to change products or specifications without notice.

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Version 133	Version 100	Units	Note
Operating Current (One bank active)	ICC1	Burst Length = 1 tRC ≥ tRC(min) IOL = 0mA	1,530	1,440	mA	1
Precharge Standby Current in Power Down Mode	ICC2P	CKE ≤ VIL(max), tCC = 10ns	50		mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tCC = ∞	50			
Precharge Standby Current in Non-Power Down Mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are charged one time during 20	370		mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	200			
Active standby current in power-down mode	ICC3P	CKE ≥ VIL(max), tCC = 10ns	80		mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	80			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	550		mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ input signals are stable	410		mA	
Operating current (Burst mode)	ICC4	Io = mA Page burst 4 Banks activated tCCD = 2CLK	2,070	1,620	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	3,150	2,880	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	60		mA	

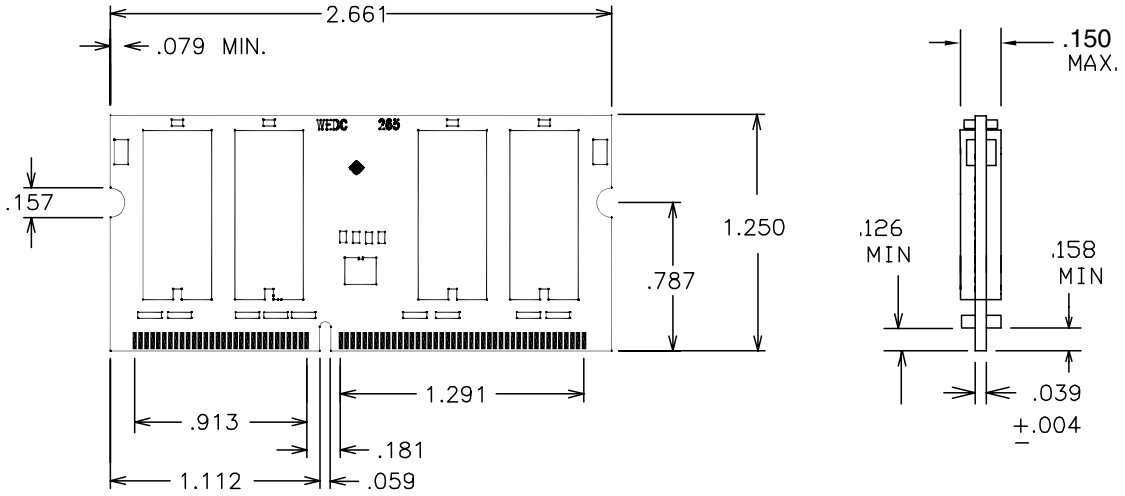
Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS (VIH/VIL = VDDQ/VssQ)

White Electronic Designs Corp reserves the right to change products or specifications without notice.

Part number	Speed	Cas Latency
WED3DG6466V10D1	100MHz	CL=2
WED3DG6466V7D1	133MHz	CL=2
WED3DG6466V75D1	133MHz	CL=3

Note: For industrial temperature range product, add an "I" to the end of the part number.

PACKAGE DIMENSIONS



ALL DIMENSIONS ARE IN INCHES

White Electronic Designs Corp reserves the right to change products or specifications without notice.

REV.	DATE	REQUESTED BY	DETAILS
A	10-21-02	PAUL MARIEN	CREATED
0	6-19-03	PAUL MARIEN	-Add PC100 & PC133 to features on page 1 -Add disclaimer note to the bottom of each page -Add industrial temp range note to order info page 5

DATASHEET APPROVALS

ECO#

EDI PART NO. _____ NEW REV _____ DATE _____

APPROVAL:	INITIAL	DATE	CORRECTION ON PAGES
JUAN GUZMAN	_____	_____	_____
MUKESH TRIVEDI	_____	_____	_____
PAUL MARIEN	_____	_____	_____
LARRY WINROTH	_____	_____	_____
DAVE KELLY	_____	_____	_____
MARK DOWNEY	_____	_____	_____
DAVE HARRISON	_____	_____	_____
TONY LEE	_____	_____	_____
BOB KHEDERIAN	_____	_____	_____
LUIS ESTELLA	_____	_____	_____

	YES	NO	
WILL THIS DATASHEET GO ON THE WEB?			LINE:_____ FAMILY:_____ PROD.TYPE:_____ ORG:_____
IS THIS A NEW DATASHEET?			DENSITY:_____ SPEED:_____
WILL THIS DATASHEET REPLACE AN EXISTING DATASHEET THAT'S ALREADY ON THE WEB?			PKG:_____ VOLTAGE:_____

IF YES, WHAT DATASHEET IS IT REPLACING? _____

WHAT SECTION SHOULD THIS DATASHEET BE PLACED IN ON THE WEB? _____

AFTER REVIEWING OR MAKING CORRECTIONS ON THE DATASHEET (S)
PLEASE SIGN-OFF ON THIS SHEET AND ,MAKE YOUR CORRECTIONS –ON **THE ORIGINAL COPY(S).**

AFTER REVIEWING THE DATA SHEET, TEST ENGINEERING WILL COMPLETE THE SECTION BELOW.

TEST PROGRAM CHANGE REQUIRED:
YES:_____NO_____DATE:_____

TEST ENGINEER SIGNATURE_____

IF YES, DO NOT RELEASE DATA SHEET UNTIL TEST PROGRAM CHANGE IS COMPLETED.
TEST PROGRAM CHANGE COMPLETION DATE:_____
TEST PROGRAM NAME AND REVISION_____
TEST ENGINEER SIGNATURE_____