INTERNATIONAL CMOS TECHNOLOGY, INC.

Product Preview

T-46-19-07

PEEL™18CV8-10/PEEL™18CV8-12
CMOS Programmable Electrically Erasable Logic Device

Features

- **1-Micron CMOS EEPROM Technology**
- **Low Power Consumption**
  - CMOS: 80mA standby + 0.5mA/MHz max
  - TTL: 90mA standby + 0.5mA/MHz max
- **Ultra High Performance**
  - 18CV8P-10: t_{PD} = 10ns max
  - 18CV8P-12: t_{PD} = 12ns max
- **EE Instant Reprogrammability**
  - 100% factory tested
  - Cost-effective windowless package
  - Erases and programs in seconds
  - Reduces retrofit and development costs
  - Provides low risk inventory
- **Foolproof Design Security**
  - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Independently programmable 12-configuration I/O macro cells
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces SSI/MSI logic
  - Emulates PAL*, GAL* and EPLDs
  - Simplifies inventory control
  - Allows new design possibilities
- **Development/Programmer Support**
  - PC-based development tools and programmer support from ICT and third-party manufacturers

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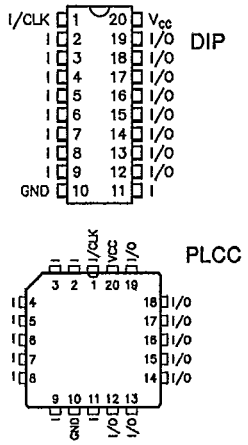
General Description

The ICT PEEL18CV8-10 or PEEL18CV8-12 is a CMOS Programmable Electrically Erasable Logic devices that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8 to replace existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party PC-based development tools and programmers from third-party manufacturers. ICT also offers a free design software package and a low-cost development system.

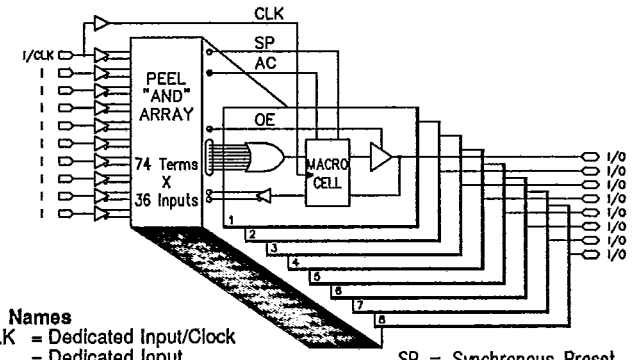
Pin Configuration



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

Block Diagram



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Fig. 1. Pinouts for DIP and PLCC

Figure 2. Block diagram of the PEEL18CV8