M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S

FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

This device has 1$\overline{CAS}$ and 2$\overline{W}$ terminals. Refresh cycle is 1024 cycles every 16.4 ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mw)
M5M44170AXX-6,-6S	60	15	30	120	580
M5M44170AXX-7,-7S	70	20	35	140	500
M5M44170AXX-8,-8S	80	20	40	160	440
M5M44170AXX-10,-10S	100	25	50	190	375

XX=J,L,TP,RT

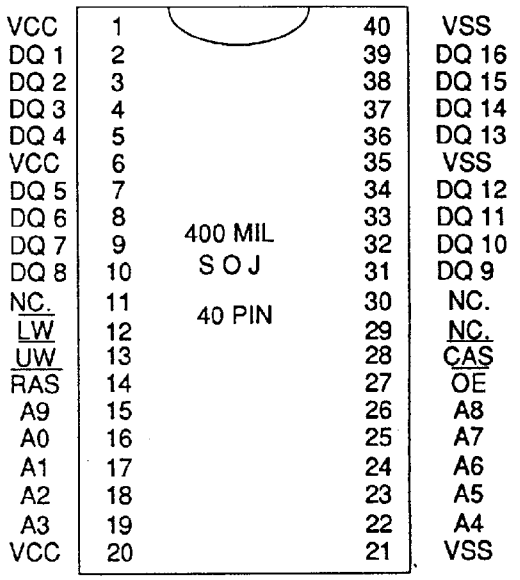
40 pin 400mil SOJ
40 pin 475mil ZIP
● 44 pin 400mil TSOP
● Single 5V±10% supply
● Low stand-by power dissipation
● 5.5mW (Max.). . . . . CMOS Input level
0.55mW*(Max.). . . . . CMOS Input level
Low operating power dissipation
● M5M44170Axx-6,-6S. . 770mW (Max.)
M5M44170Axx-7,-7S. . 660mW (Max.)
M5M44170Axx-8,-8S. . 578mW (Max.)
M5M44170Axx-10,-10S. . 495mW (Max.)
● Fast-page mode (256-bit random access), Read -modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
● Self reflesh capability
Self reflesh current..200us
● Extended reflesh capability
Extended reflesh current..250us
● Early write mode and $\overline{LW}$/$\overline{UW}$ and $\overline{OE}$ to control output buffer impedance
● All inputs, output TTL compatible and low capacitance
● 1024 refresh cycles every 16.4ms (A0 — A9)
● 1024 refresh cycles every 128 ms (A0 — A9)*

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

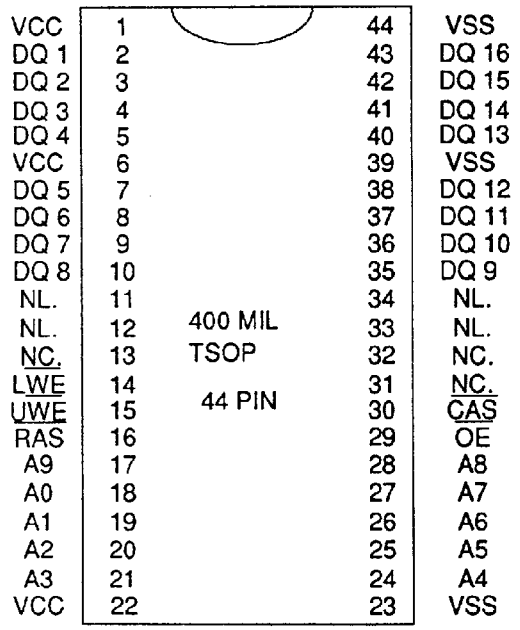
*:Applicable to self refresh version(M5M44170AJ,L,TP,RT -6S,-7S,-8S,-10S:option)only.

PIN CONFIGURATION (TOP VIEW)



(M5M44170AJ)

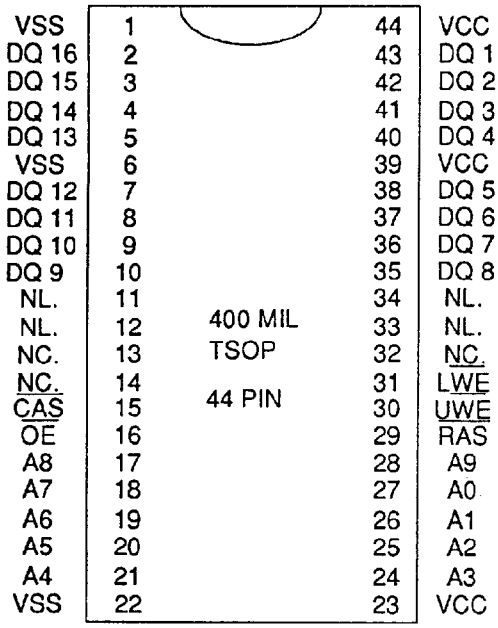
PIN CONFIGURATION (TOP VIEW)



(M5M44170ATP)

NL=NO LEAD

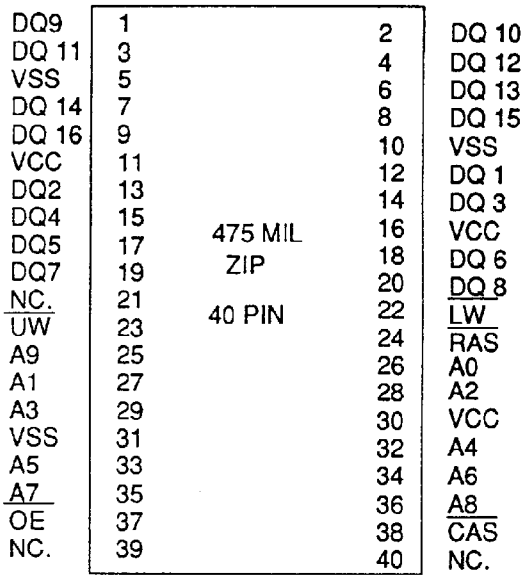
PIN CONFIGURATION (TOP VIEW)



(M5M44170ART)

NL=NO LEAD

PIN CONFIGURATION (TOP VIEW)



(M5M44170AL)

FUNCTION

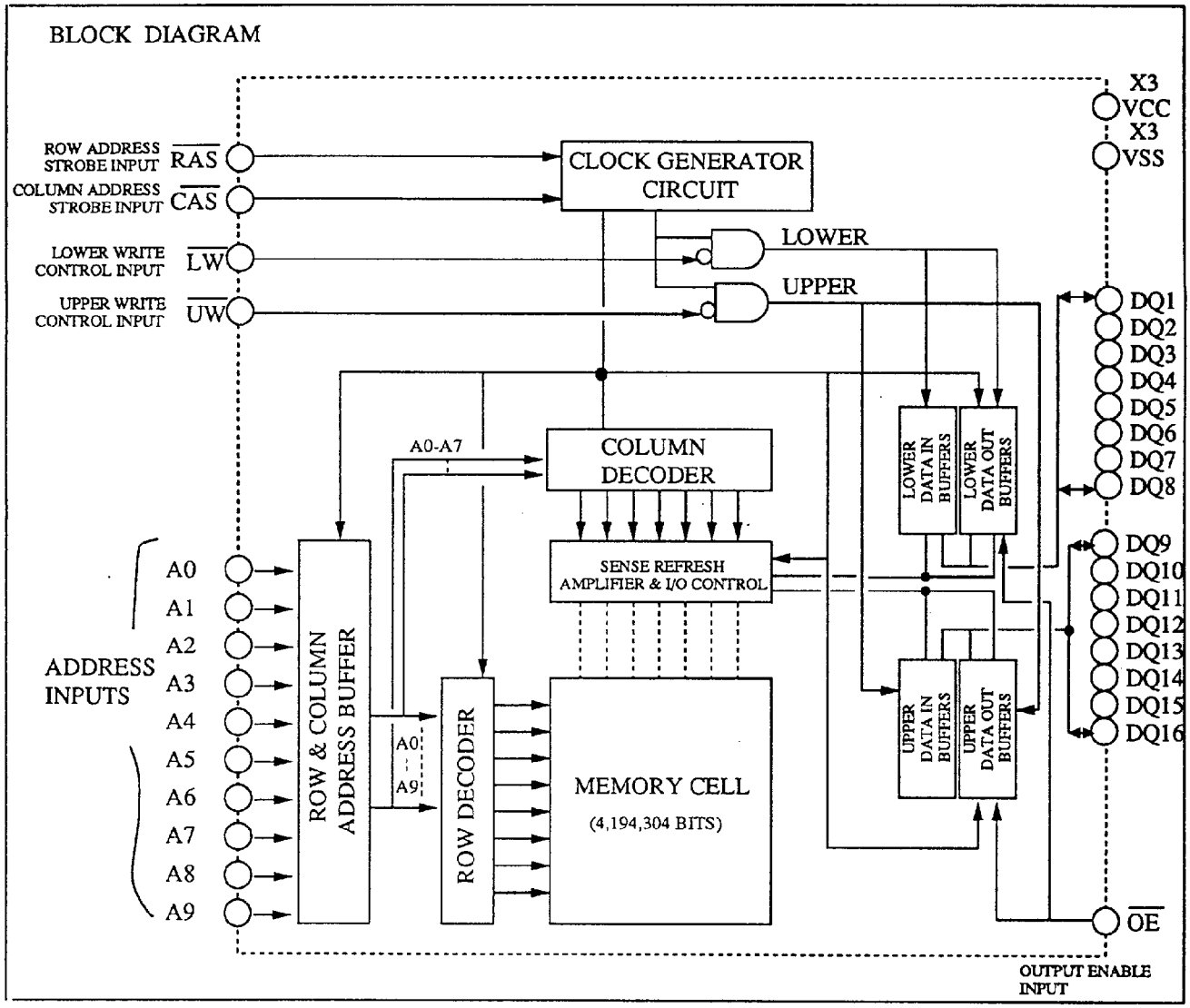
The M5M44170AJ, TP,RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input condition for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{LW}$	$\overline{UW}$	$\overline{OE}$	DQ1 - DQ8	DQ9 - DQ16		
Read	ACT	ACT	NAC	NAC	ACT	DOUT	DOUT	YES	Fast page mode indentical
Lower byte write	ACT	ACT	ACT	NAC	NAC	DIN	DNC	YES	
Upper byte write	ACT	ACT	NAC	ACT	NAC	DNC	DIN	YES	
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	DOUT	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	DNC	DNC	DNC	OPN	OPN	YES	
Self refresh*	ACT	ACT	DNC	DNC	DNC	OPN	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN	NO	

Note ACT:active, NAC:nonactive, DNC:don't care, OPN:open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1～7	V
Vi	Input voltage		-1～7	V
Vo	Output voltage		-1～7	V
Io	Output current		50	mA
Pd	Power dissipation	Ta = 25℃	1000	mW
Topr	Operating temperature		0～70	℃
Tstg	Storage temperature		-65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 ℃, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
Vcc	Supply voltage		4.5	5	5.5	V
Vss	Supply voltage		0	0	0	V
VIH	High-level input voltage, all inputs		2.4		6.5	V
VIL	Low-level input voltage	DQ1 ~ DQ16	-1.0		0.8	V
		Others	-2.0		0.8	V

Note 1: All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70 ℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH = -5mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL = 4.2mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V ≦ Vout ≦ 5.5V	-10		10	uA
Ii	Input current		0 ≦ VIH ≦ 6.5V, Other inputs pins = 0V	-10		10	uA
ICC1	Average supply current from Vcc operating (Note 3, 4, 5)	M5M44170A-6,-6S	$\overline{RAS}$,$\overline{CAS}$ cycling tRC = tWC = min. output open			140	mA
		M5M44170A-7,-7S				120	
		M5M44170A-8,-8S				105	
		M5M44170A-10,-10S				90	
ICC2	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = VIH, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ VCC-0.5 output open			1	
						0.1*	
ICC3	Average supply current from Vcc refreshing (Note 3, 5)	M5M44170A-6,-6S	$\overline{RAS}$ cycling $\overline{CAS}$ = VIH, tRC = min. output open			140	mA
		M5M44170A-7,-7S				120	
		M5M44170A-8,-8S				105	
		M5M44170A-10,-10S				90	
ICC4	Average supply current from Vcc Fast-Page-Mode (Note 3, 4, 5)	M5M44170A-6,-6S	$\overline{RAS}$ = VIL $\overline{CAS}$ cycling tPC = min., output open			140	mA
		M5M44170A-7,-7S				120	
		M5M44170A-8,-8S				105	
		M5M44170A-10,-10S				90	
ICC6	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M44170A-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, tRC = min. output open			120	mA
		M5M44170A-7,-7S				105	
		M5M44170A-8,-8S				90	
		M5M44170A-10,-10S				80	

ELECTRICAL CHARACTERISTICS (continued) (Ta = 0 ~ 70 ℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ICC 8 *	Averange supply current from VCC Extended refresh mode (Note 6)	$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ befor $\overline{RAS}$ refresh cycling $\overline{OE}$≦ 0.2V or≧ Vcc - 0.2V $\overline{WE}$≦ 0.2V or ≧ Vcc - 0.2V A0 ~ A9≦ 0.2V or≧ Vcc - 0.2V DQ = open tRC = 125 us tRAS = tRAS min ~ 1us			250	u A
ICC 9 *	Averange supply current from VCC Self refresh mode (Note 6)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V $\overline{OE}$≦ 0.2V or≧ Vcc - 0.2V $\overline{WE}$≦ 0.2V or ≧ Vcc - 0.2V A0 ~ A9≦ 0.2V or≧ Vcc - 0.2V			200	u A

Note 2: Current flowing into an IC is positive. out is negative.
3: Icc1(AV), Icc3(AV) and Icc4(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1(AV) and Icc4(AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.

CAPACITANCE (Ta = 0 ~ 70 ℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
CI (A)	Input capacitance, address inputs	M5M44170AJ,TP,RT	VI=VSS f=1MHZ Vi=25mVrms			5	pF
		M5M44170AL				7	pF
CI (CLK)	Input capacitance, clock inputs	M5M44170AJ,TP,RT				7	pF
		M5M44170AL				9	pF
CI/O	Input/Output capacitance, data ports	M5M44170AJ,TP,RT				7	pF
		M5M44170AL				9	pF

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70 ℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 5, 12, 13)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS (Note 7, 8)		15		20		20		25	ns
tRAC	Access time from RAS (Note 7, 9)		60		70		80		100	ns
tAA	Column Address access time (Note 7, 10)		30		35		40		50	ns
tCPA	Access time from CAS precharge (Note 7, 11)		35		40		45		55	ns
tOEA	Access time from OE (Note 7)		15		20		20		25	ns
tCLZ	Output low impedance from CAS low (Note 7)	5		5		5		5		ns
tOFF	Output disable time after CAS high (Note 12)	0	15	0	20	0	20	0	25	ns
tOEZ	Output disable time after OE high (Note 12)	0	15	0	20	0	20	0	25	ns

Note 6: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 2TTL loads and 100pF.

8: Assumes that tRCD ≧ tRCD(max) and tASC≧ tASC (max).

9: Assumes that tRCD ≦ tRCD(max) and tRAD≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD or tRAD exceeds the value shown.

10: Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC (max).

11: Assumes that tCP ≦ tCP(max) and tASC ≧ tASC (max).

12: tOFF(max) and tOEZ(max) defines the time at which the output achieves the high impedance state (Iout ≦ | ± 10 μ A |) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)
(Ta = 0 ~ 70 ℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 12, 13)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4		16.4	ms
tREF	Refresh cycle time*		128		128		128		128	ms
tRP	$\overline{RAS}$ high pulse width	50		60		70		80		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 15)	20	45	20	50	20	60	25	75	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width	10		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low (Note 16)	15	30	15	35	15	40	20	50	ns
tASR	Row address setup time before $\overline{RAS}$ low	0		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low (Note 17)	0	10	0	10	0	15	0	20	ns
tRAH	Row address hold time after $\overline{RAS}$ low	10		10		10		15		ns
tCAH	Column address hold time after $\overline{CAS}$ low	15		15		15		20		ns
tDZC	Delay time, data to $\overline{CAS}$ low (Note 18)	0		0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low (Note 18)	0		0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data (Note 19)	15		20		20		25		ns
tODD	Delay time, $\overline{OE}$ high to data (Note 19)	15		20		20		25		ns
tT	Transition time (Note 20)	1	50	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT = 5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) = tRAH(min) + 2tT + tASC(min).
16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	120		140		160		190		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	100	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	20	10000	25	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		100		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		25		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		40		50		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		20		25		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		20		25		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	120		140		160		190		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	100	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	20	10000	25	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		100		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		25		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		15		15		20		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		20		25		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		20		25		ns
t WP	Write pulse width	10		15		15		20		ns
tDS	Data setup time before $\overline{CAS}$ low or W low	0		0		0		0		ns
tDH	Data hold time after CAS low or W low	10		15		15		20		ns
tOEH	OE hold time after W low	15		20		20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRWC	Read Write/read modify write cycle time (Note 22)	160		185		205		245		ns
tRAS	$\overline{RAS}$ low pulse width	95	10000	115	10000	125	10000	155	10000	ns
tCAS	$\overline{CAS}$ low pulse width	50	10000	65	10000	65	10000	80	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	95		115		125		155		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	50		65		65		80		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	35		40		40		50		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	80		90		100		125		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	50		55		60		75		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		20		25		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		20		25		ns
tWP	Write pulse width	10		15		15		20		ns
tDS	Data setup time before $\overline{W}$ low	0		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		15		15		20		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	15		15		20		25		ns

Note 22: tRWC is specified as tRWC(min) = tRAC(max) + tODD(min) + tRWL(min) + tRP(min) + 4tT.

23: tWCS, tCWD, tRWD and tAWD and tCPWD are specified as reference points only. If tWCS ≧ tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD ≧ tCWD(min), tRWD ≧ tRWD(min), tAWD ≧ tAWD(min), and tCPWD ≧ tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		50		60		ns
tPRWC	Fast page mode read write/read modify write cycle time	75		95		100		115		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	100	100000	115	100000	135	100000	160	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note 26)	10	15	10	15	10	20	10	25	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		55		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	35		40		45		55		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.
26: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle ,Extended Refresh* (Note 27)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before RAS low	10		10		10		10		ns
tCHR	$\overline{CAS}$ hold time after RAS low	10		15		15		20		ns
tCAS	$\overline{CAS}$ low pulse width	25		30		30		35		ns

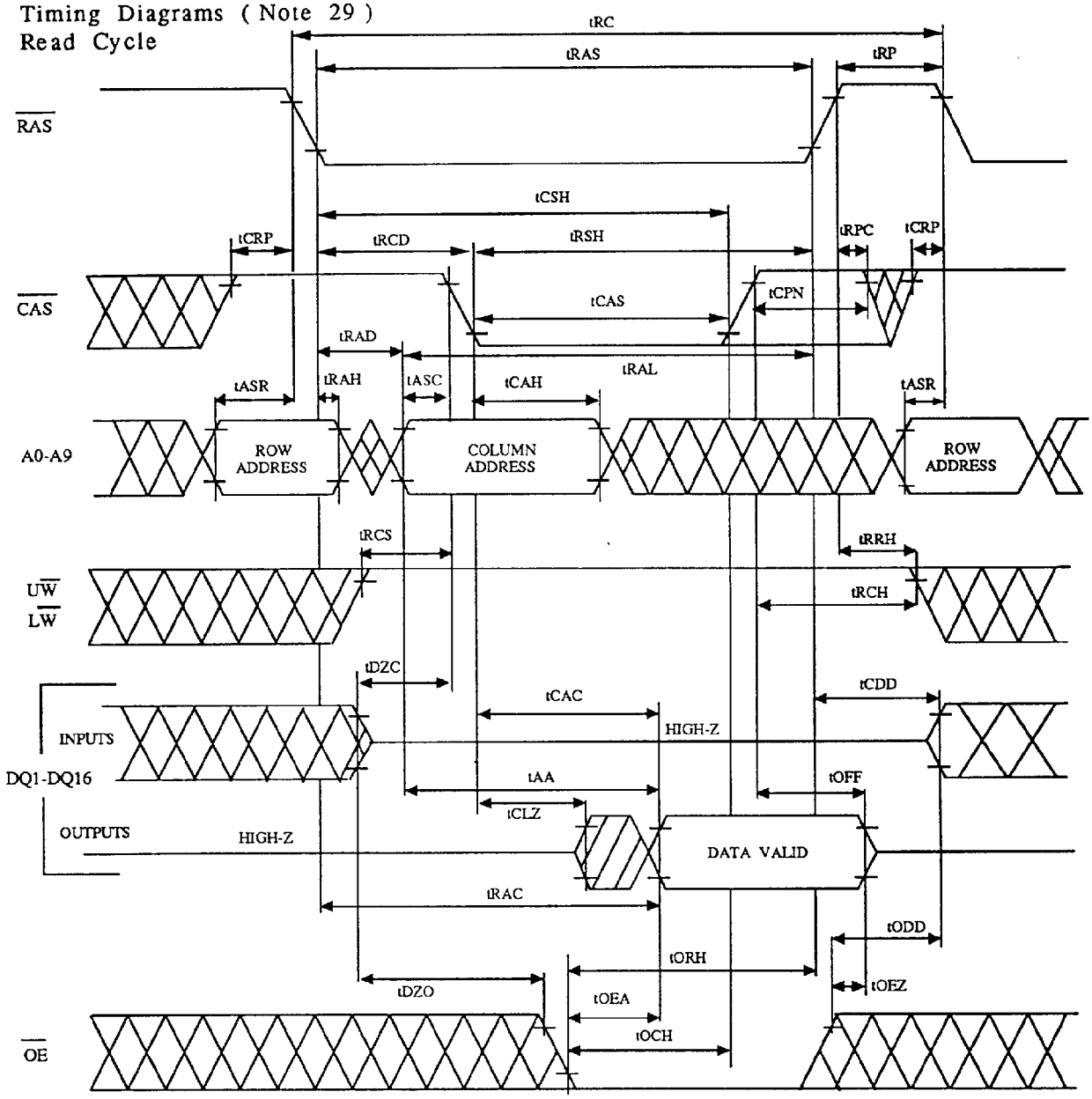
Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

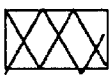
$\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle* (Note 28)

Symbol	Parameter	Limits								Unit
		M5M44170A-6S		M5M44170A-7S		M5M44170A-8S		M5M44170A-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRASS	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		100		μs
tRPS	CBR self refresh $\overline{RAS}$ high precharge time	120		140		160		190		ns
tCHS	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		-50		ns

Timing Diagrams (Note 29)

Read Cycle

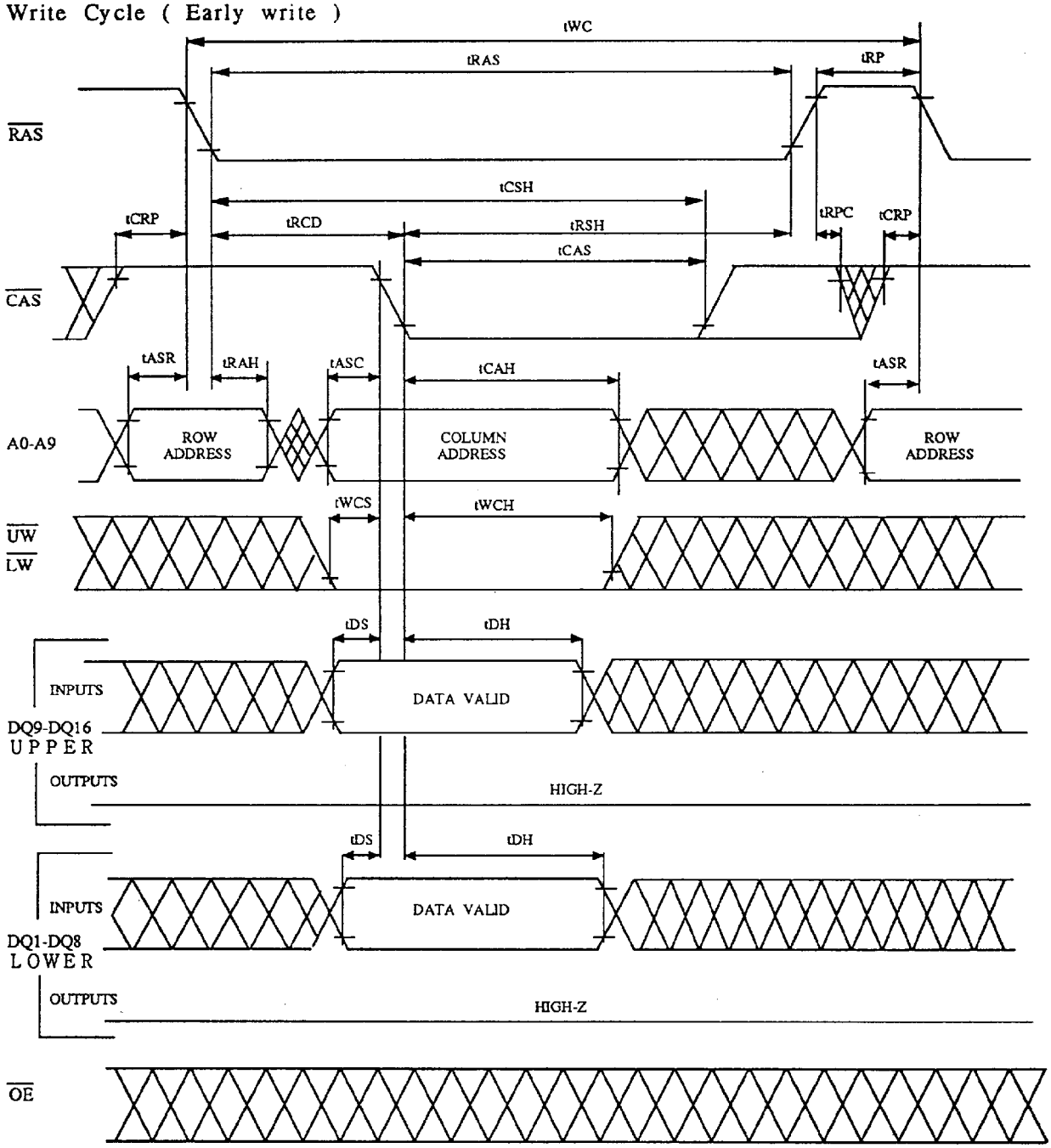


Note 29  Indicates the don't care input.
VIH(min) ≦ VIN ≦ VIH(max) or VIL(min) ≦ VIN ≦ VIL(max)

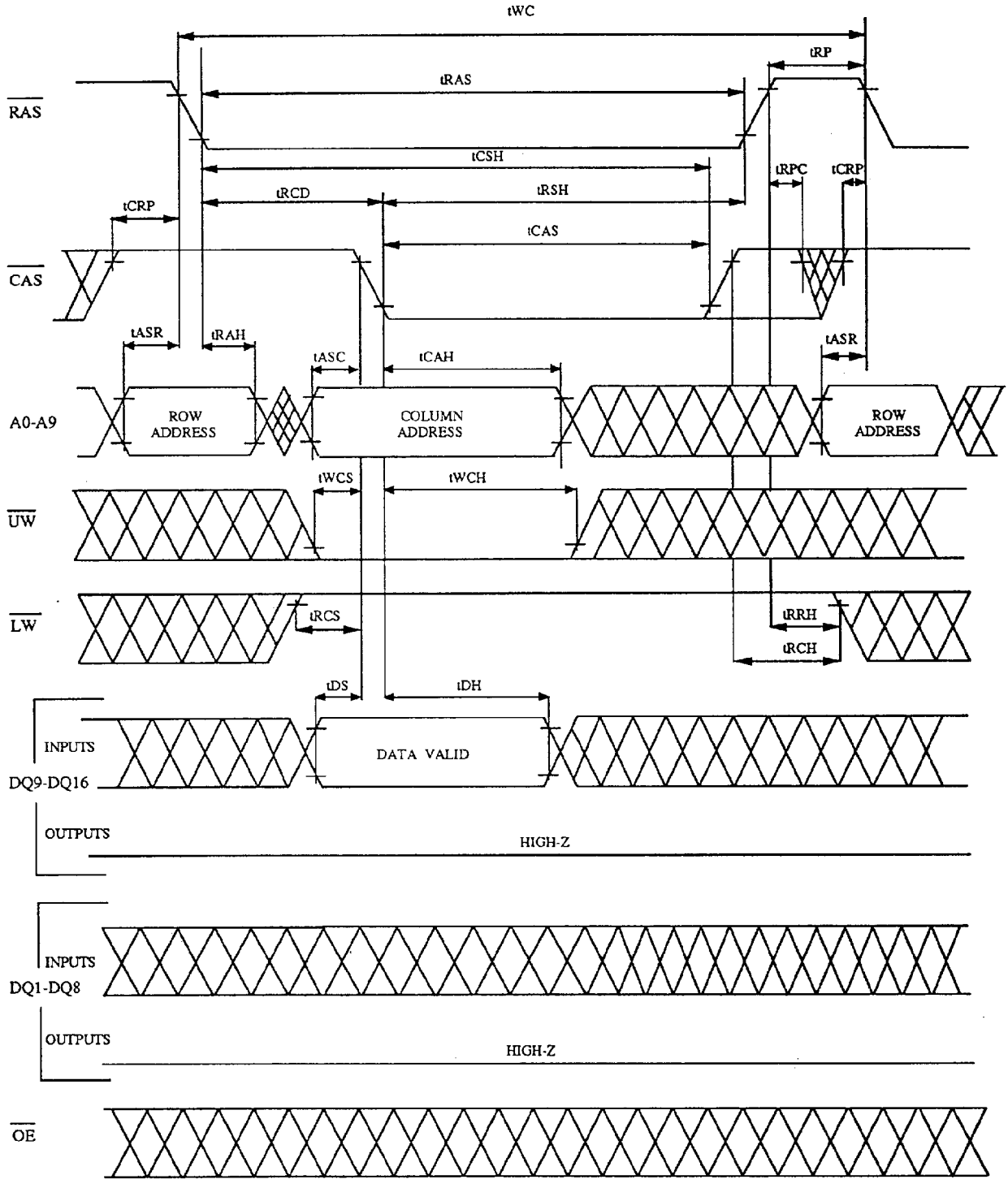
 Indicates the invalid output.

 Indicates the skew of the two inputs.

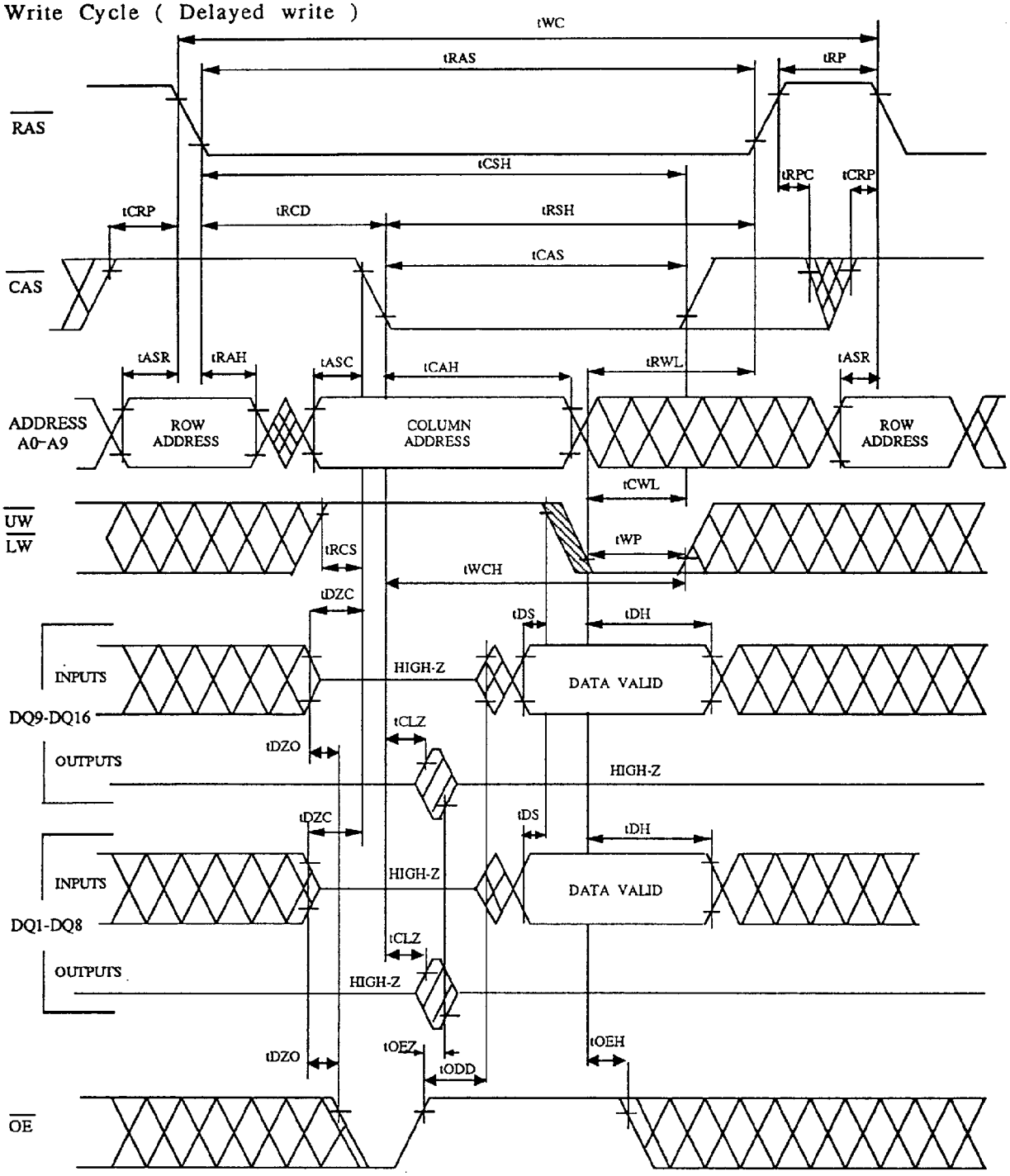
Write Cycle (Early write)



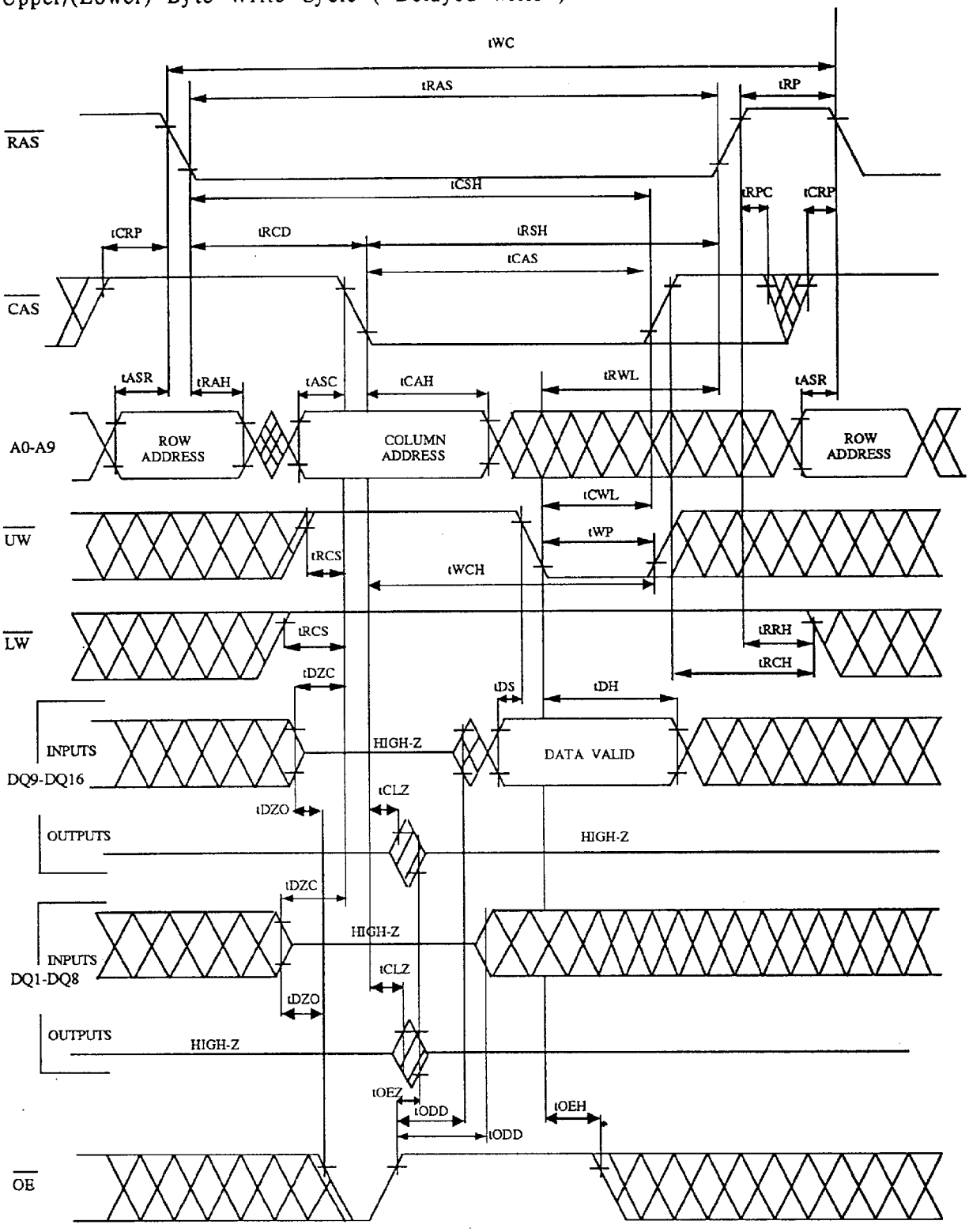
Upper/(Lower) Byte Write Cycle (Early write)



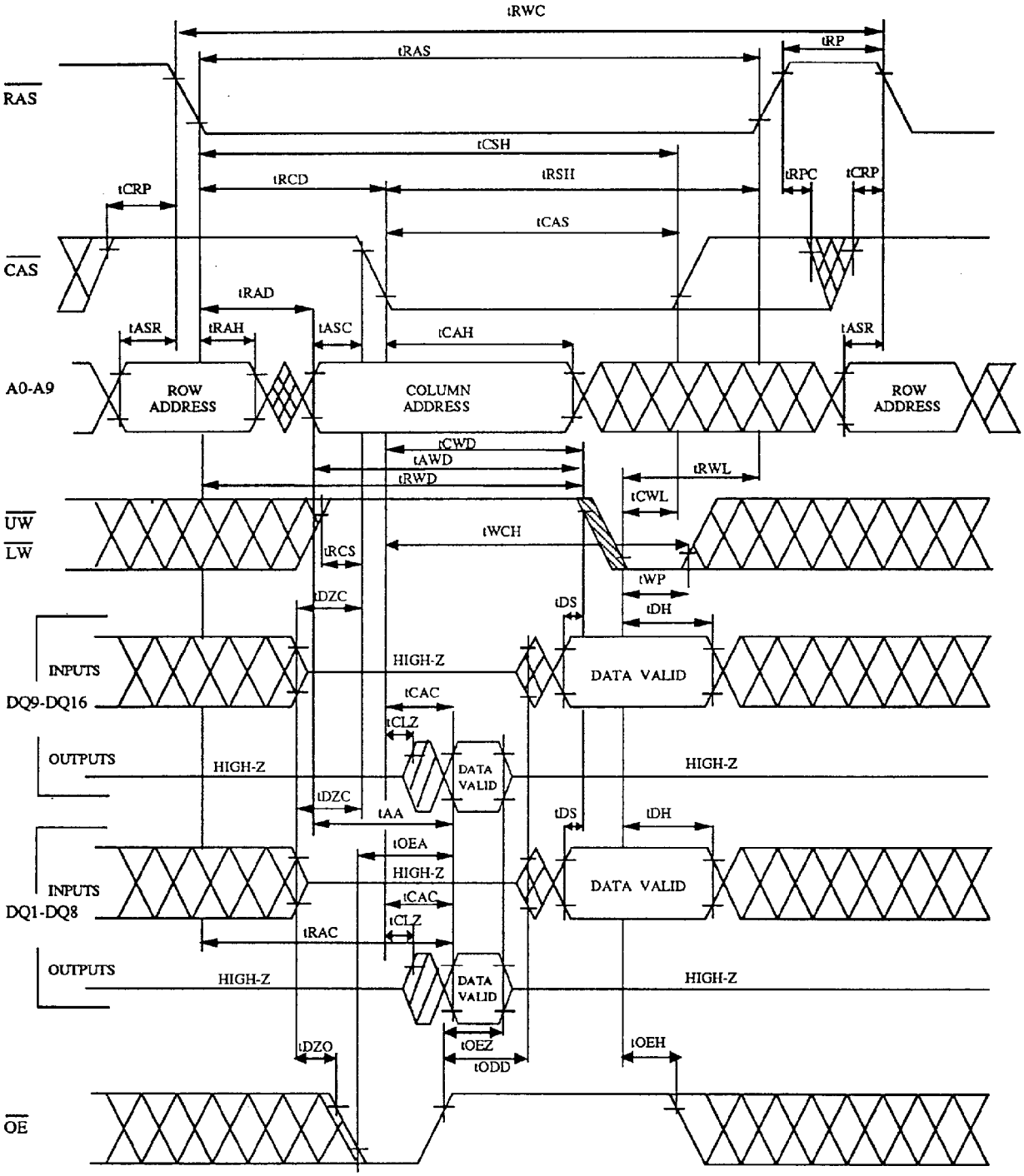
Write Cycle (Delayed write)



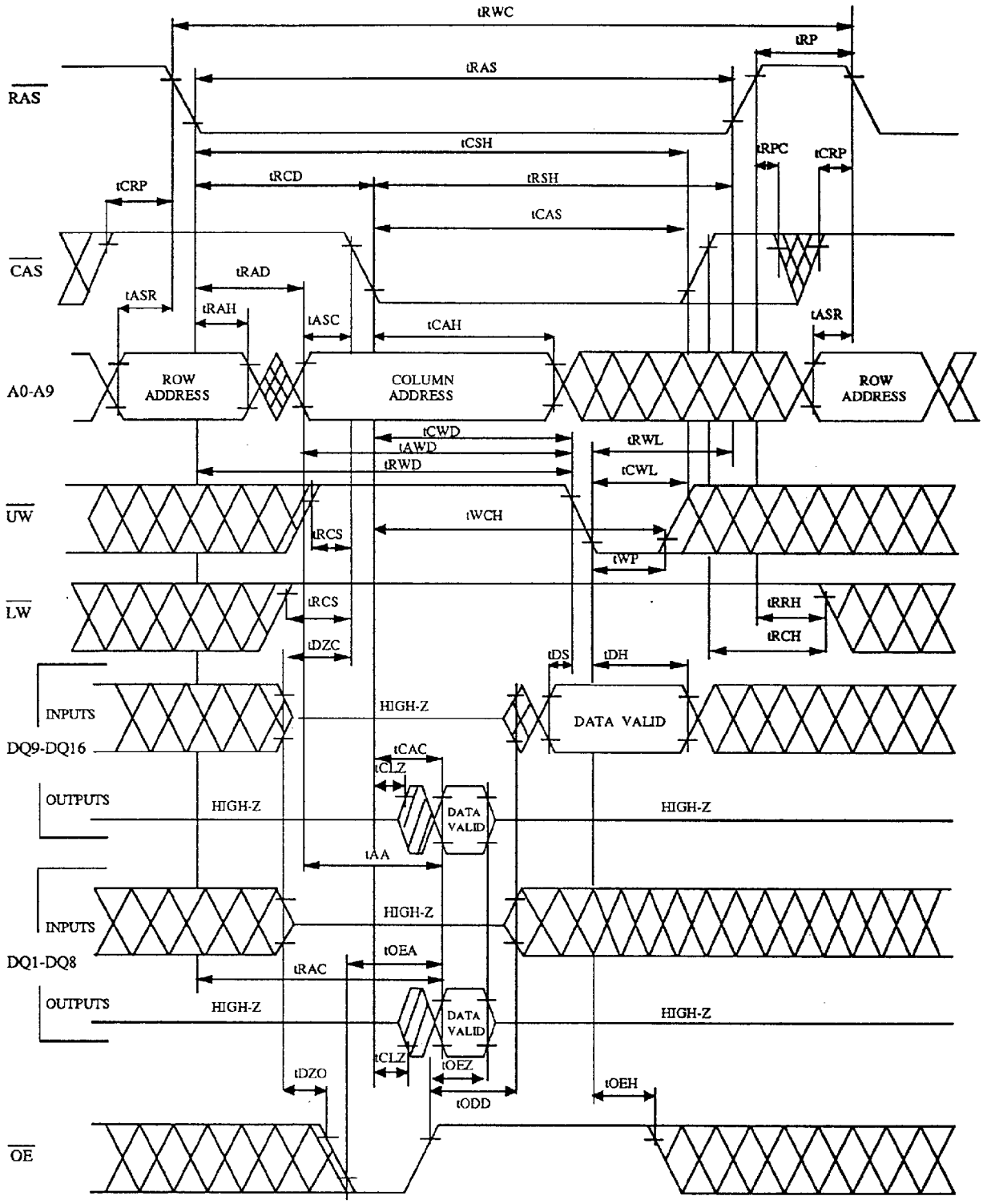
Upper/(Lower) Byte Write Cycle (Delayed write)



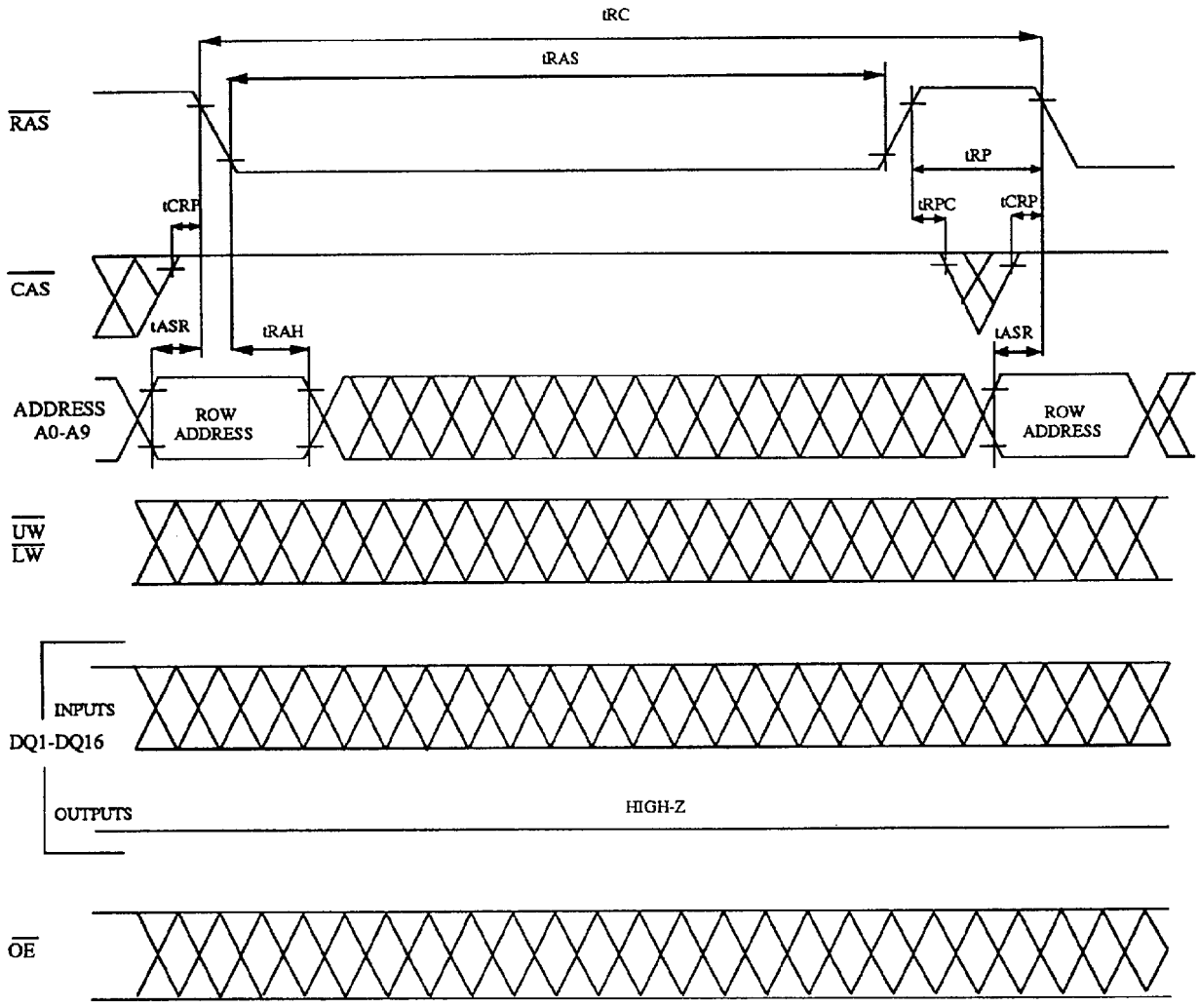
Read-Write, Read-Modify-Write Cycle



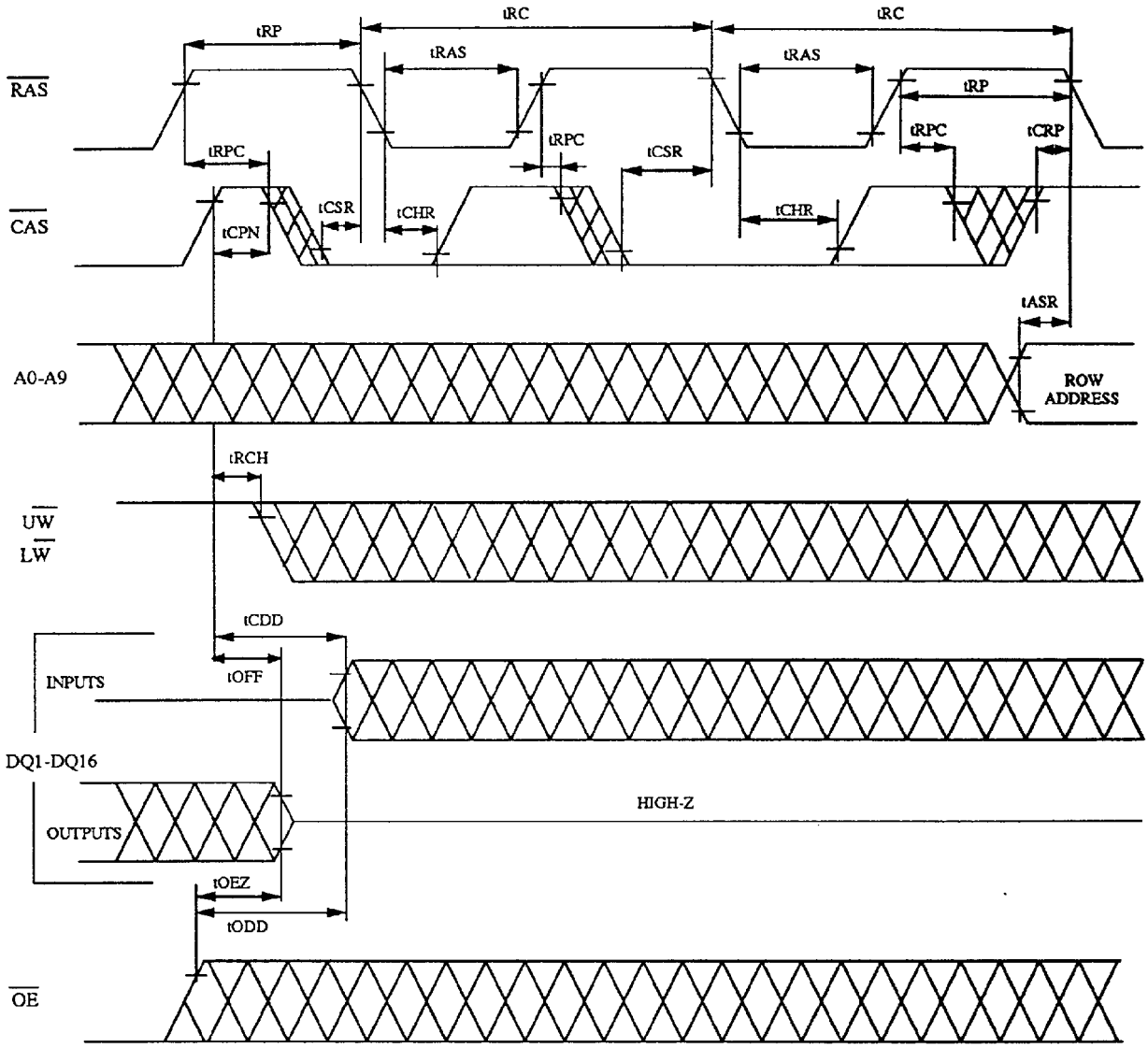
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



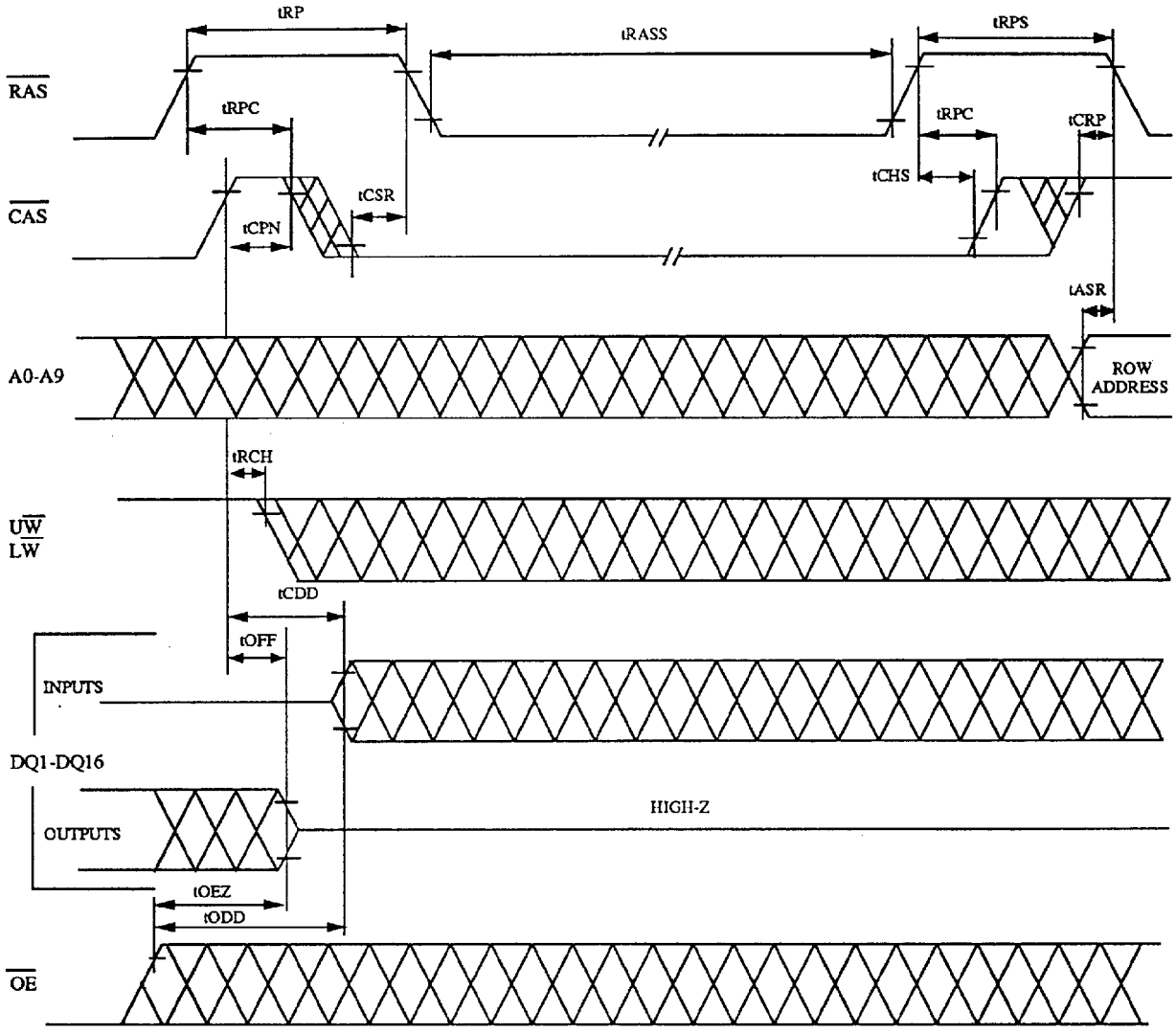
$\overline{RAS}$-only Refresh Cycle



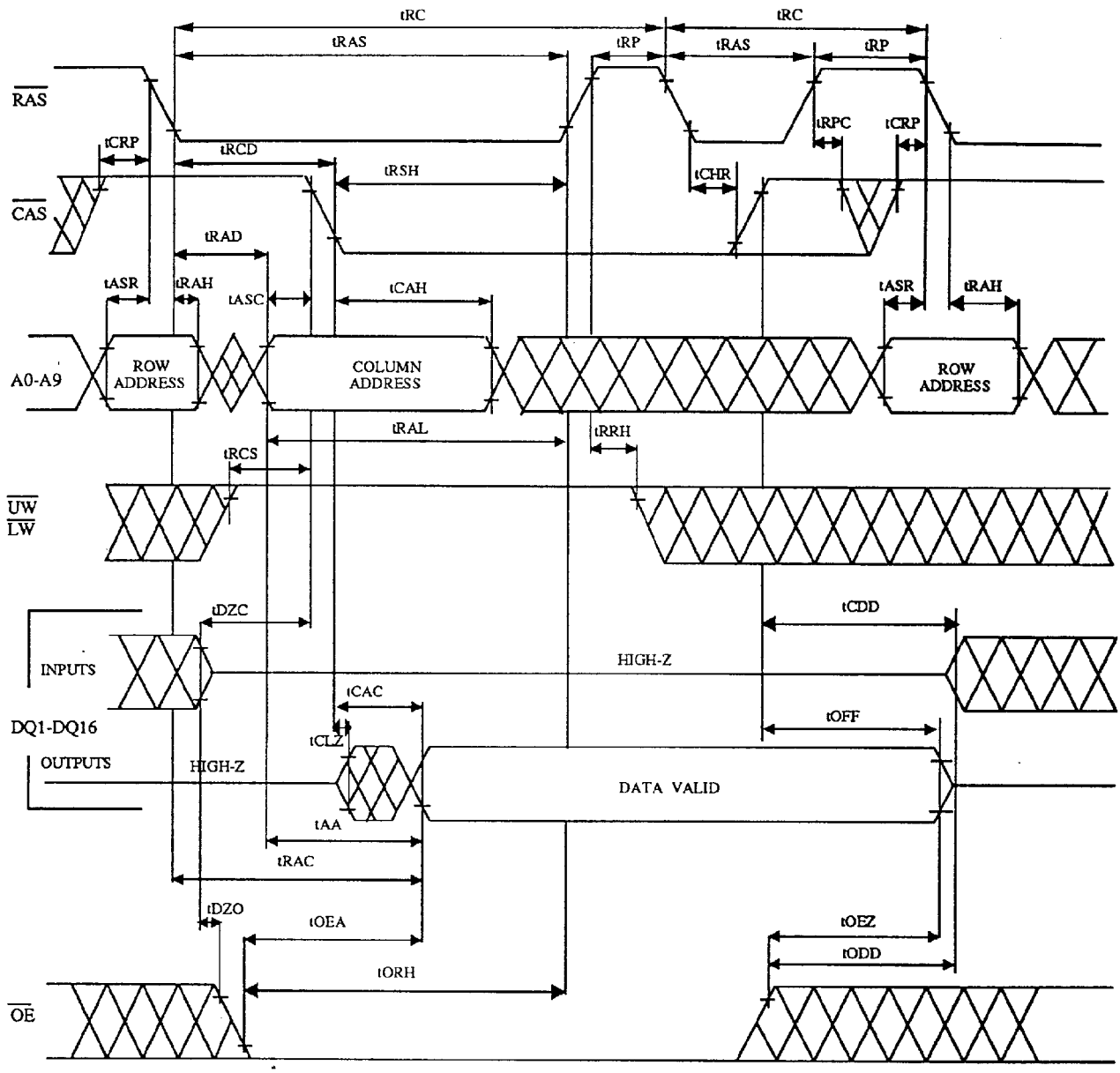
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle ,Extended Refresh Cycle *



Self Refresh Cycle * (Note 28)

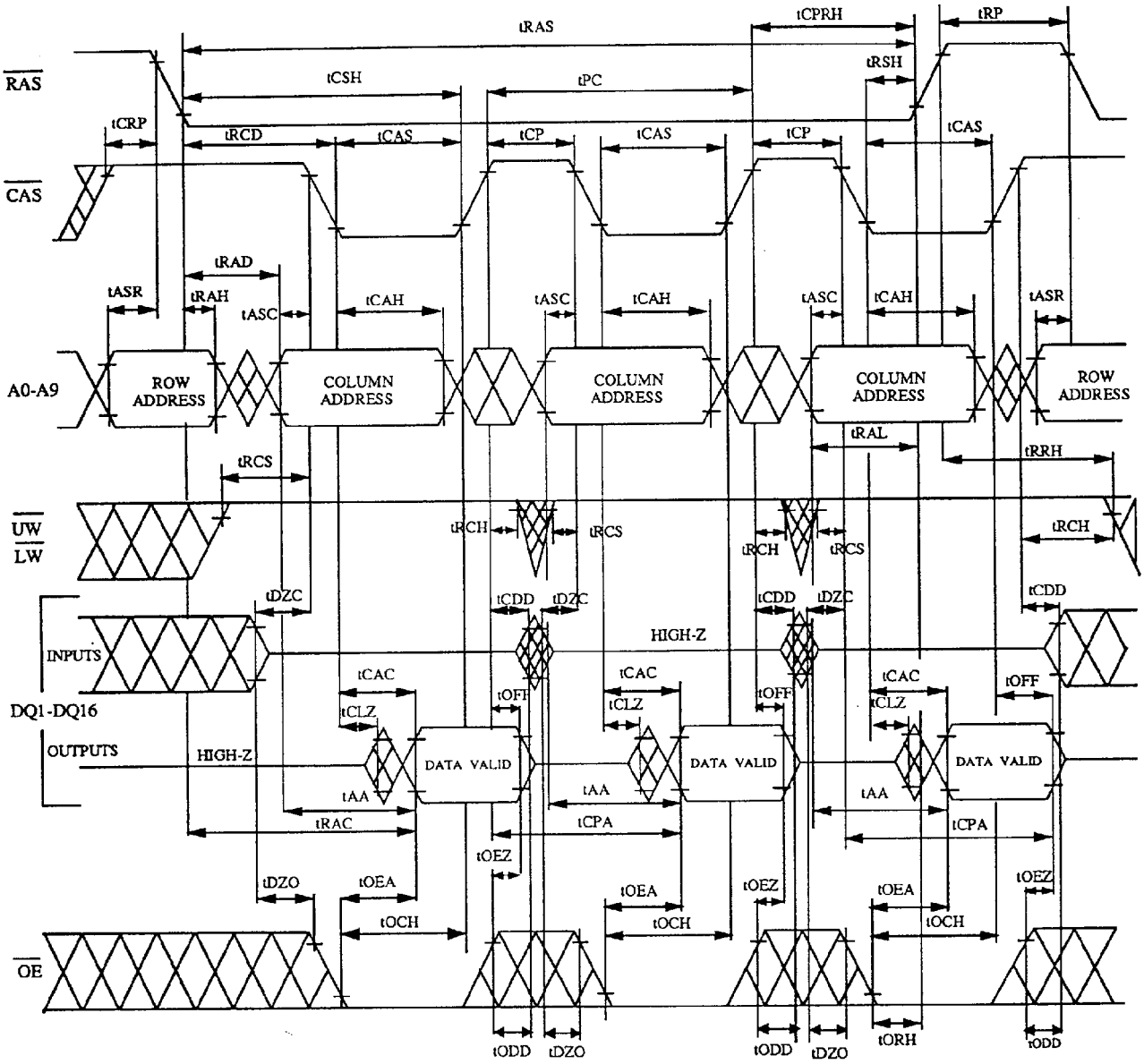


Hidden Refresh Cycle (Read) (Note 30)

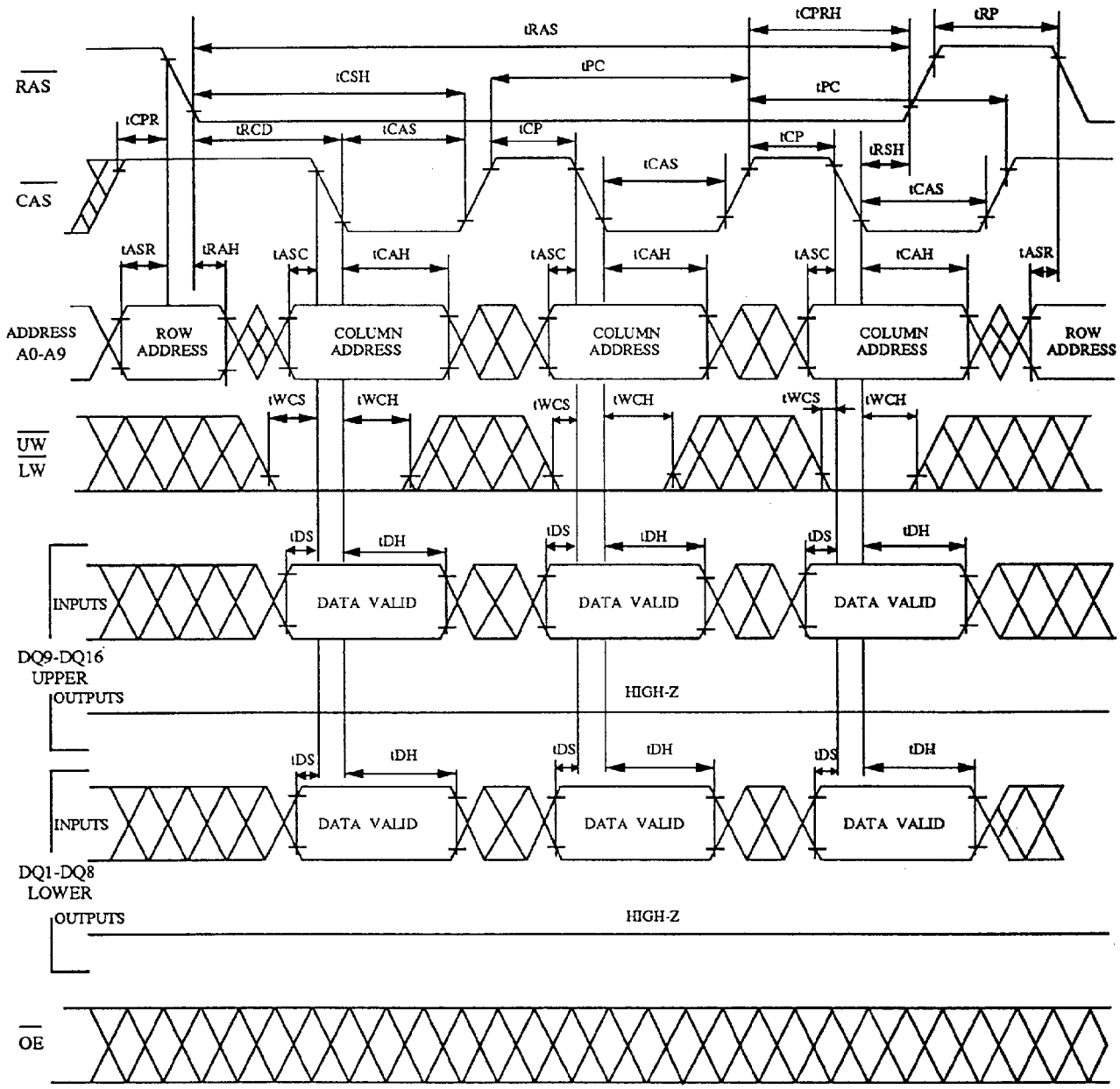


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

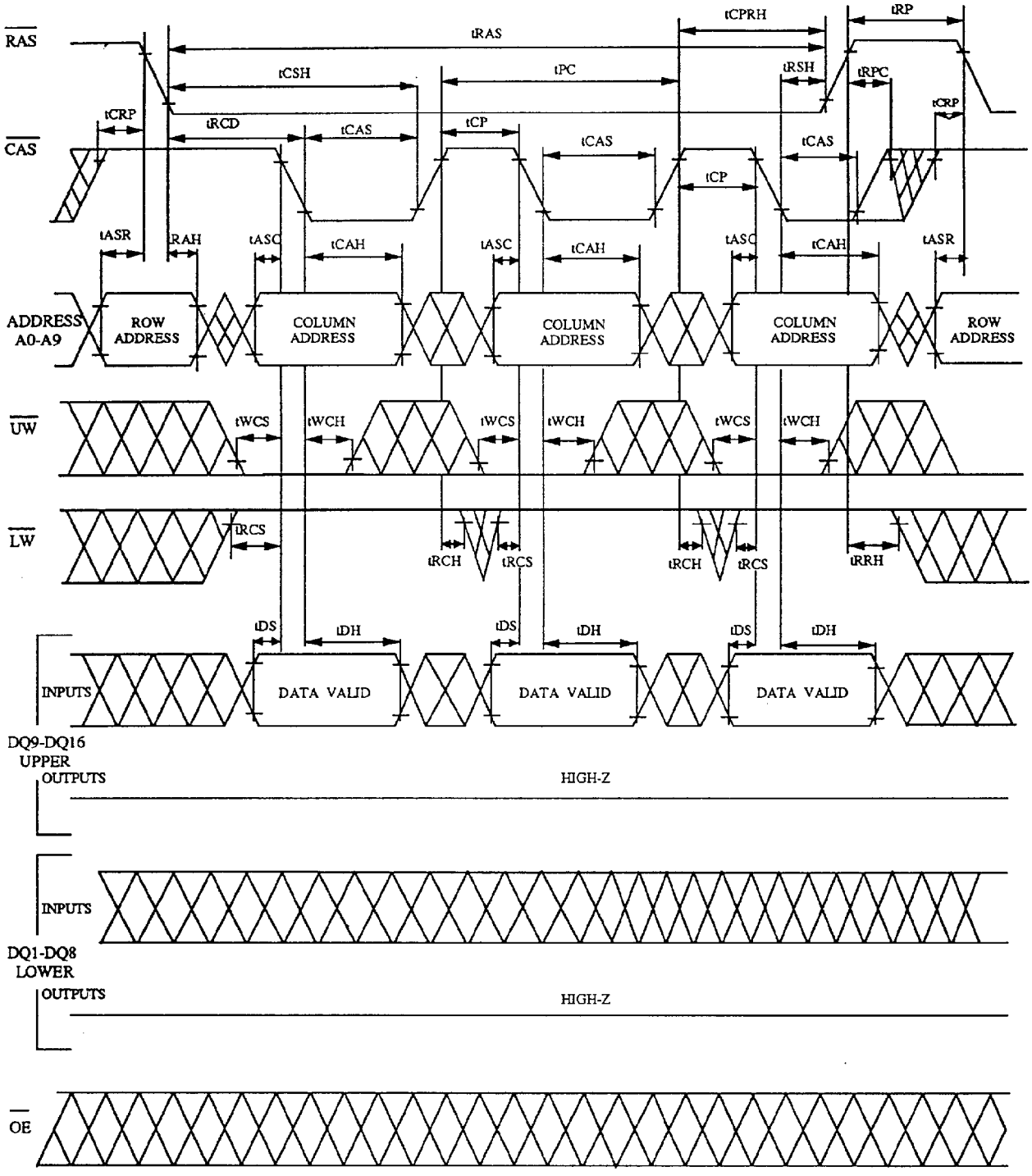
Fast Page Mode Read Cycle



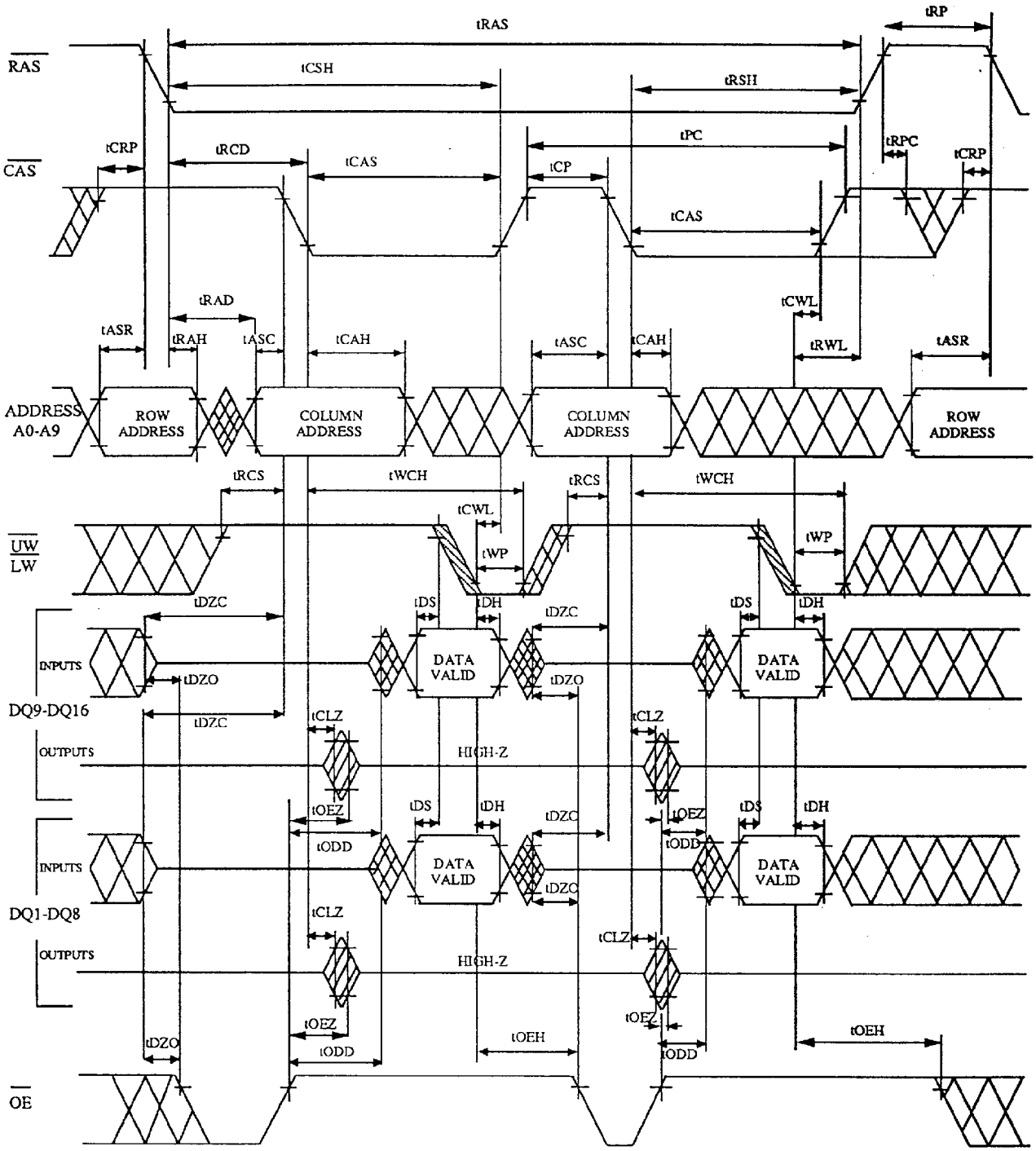
Fast Page Mode Write Cycle (Early Write)



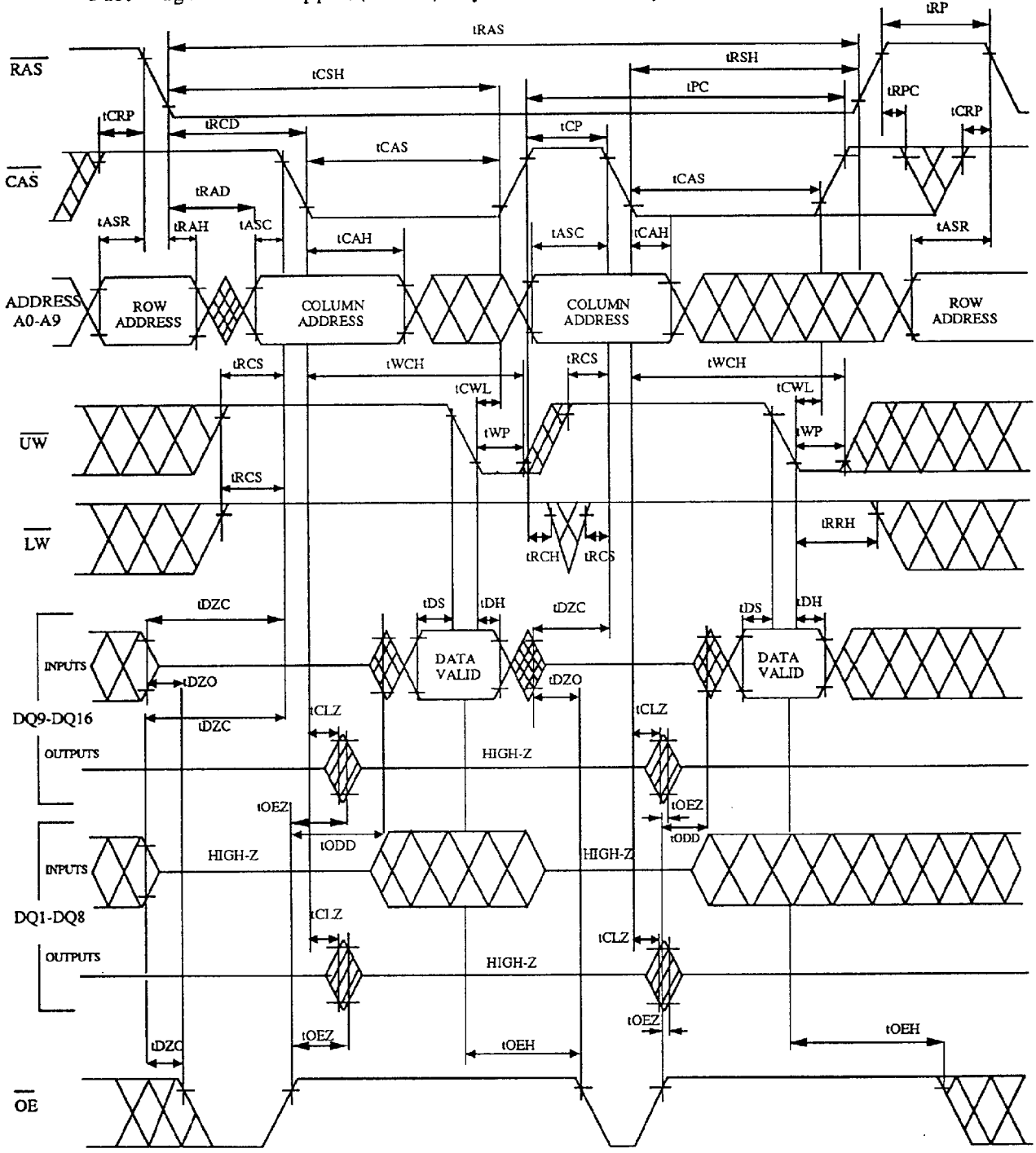
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



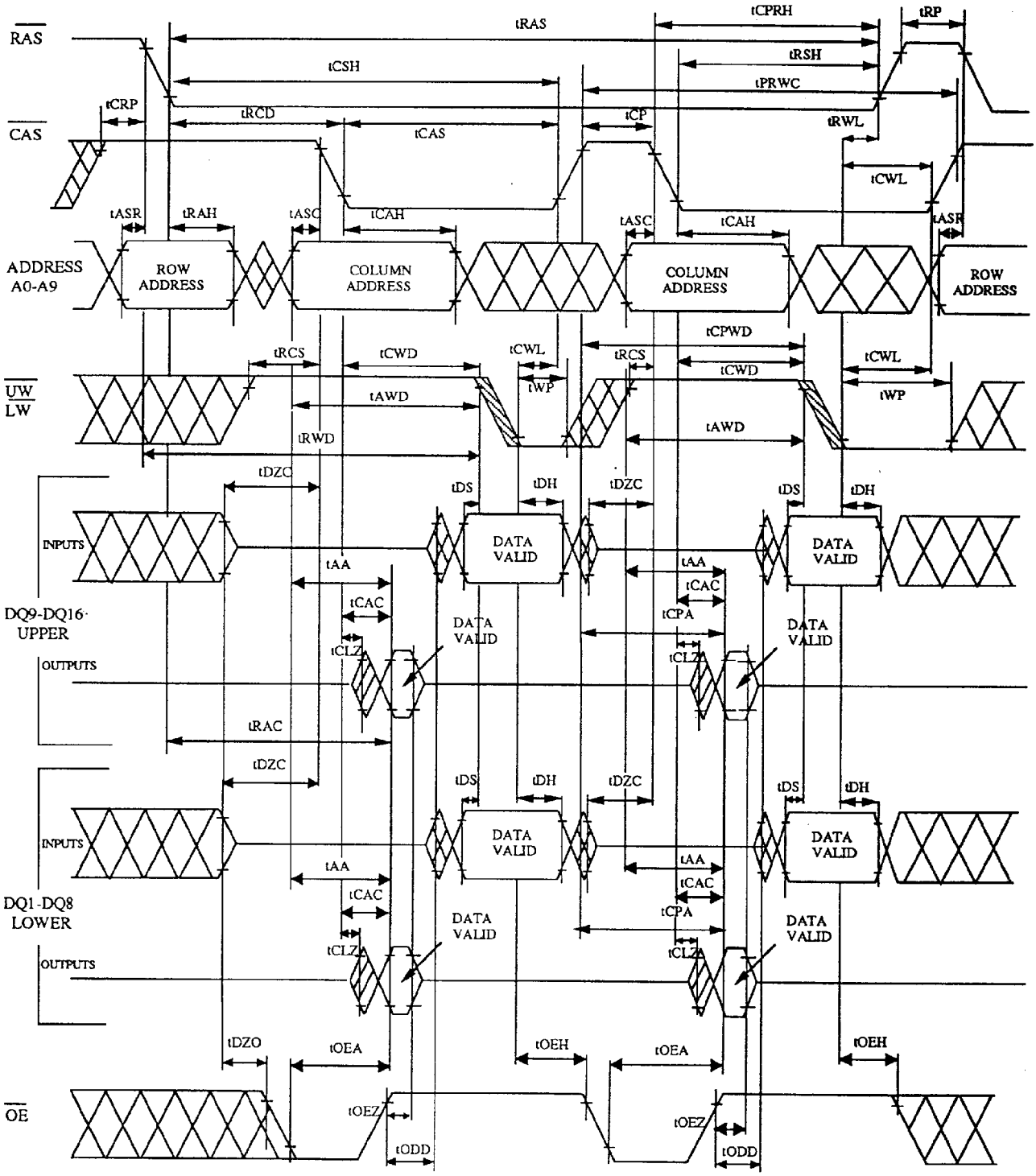
Fast Page Mode Write Cycle (Delayed Write)



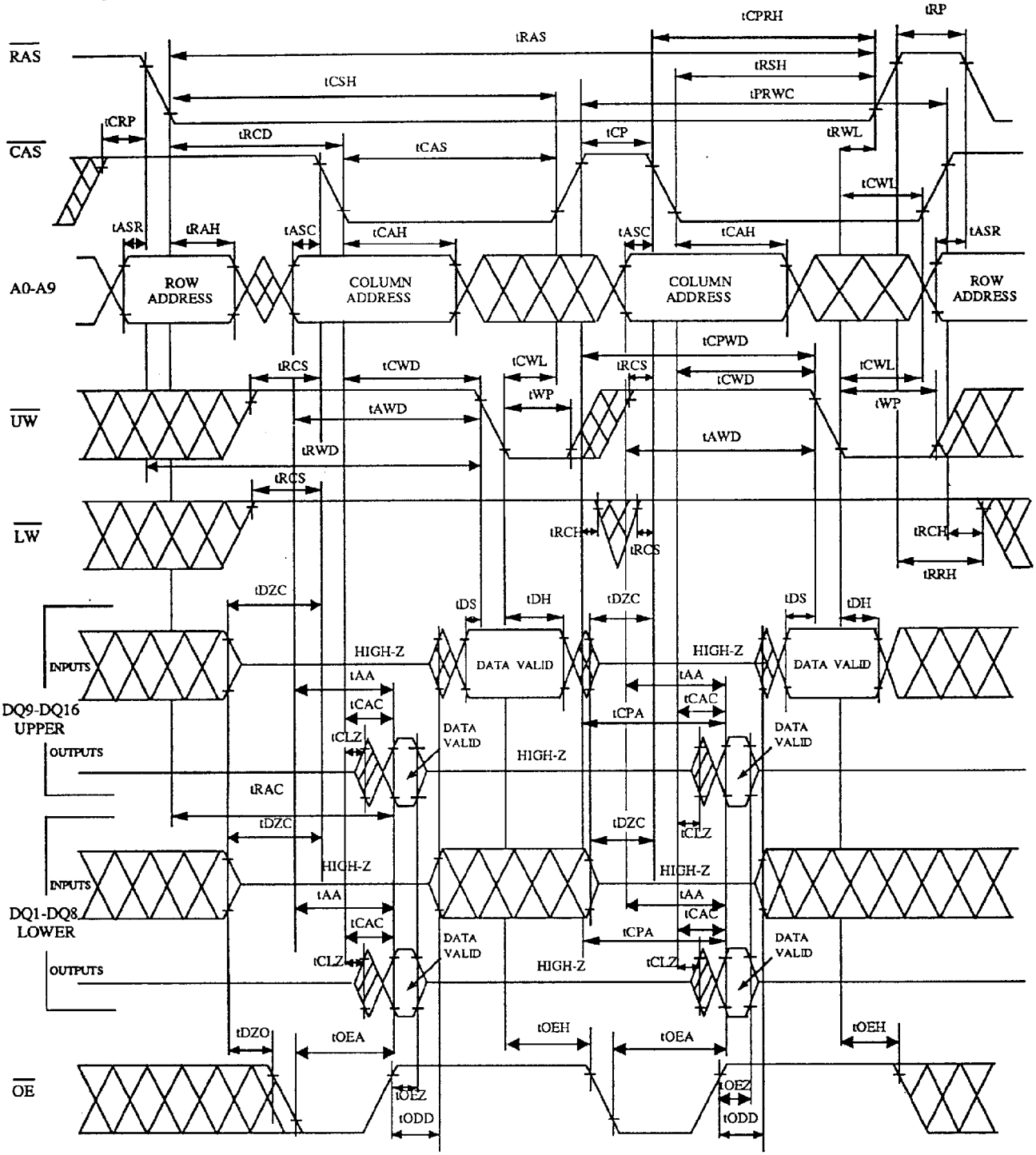
Fast Page Mode Upper/(Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



Note 2 8 Self refresh sequence MITSUBISHI (MEMORY/ASIC)

Two refreshing ways shoud be used properly depending on the low pulse width (tRASS) of $\overline{RAS}$ signal during self refresh period .

1 . In case of tRASS < 300 ms

1.1 Distriduted refresh during Read / Write operation

(A) Timing Diagrams

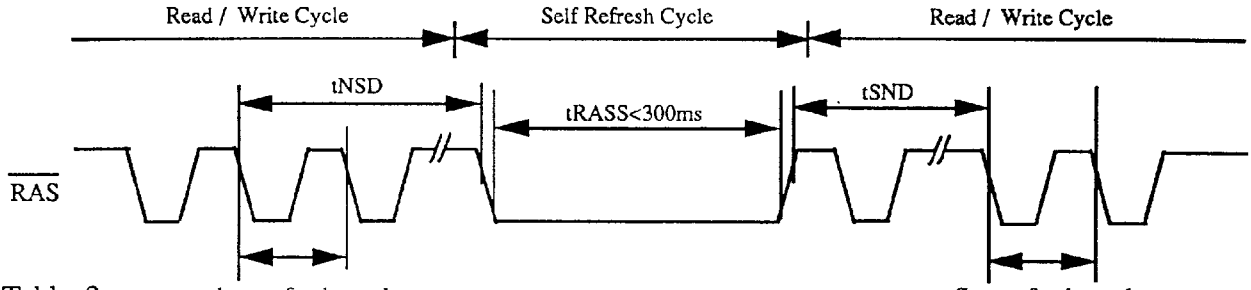


Table 2

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR distributed refresh	tNSD + tSND ≦ 16.4 m s	
$\overline{RAS}$ only distributed refresh	tNSD ≦ 16 μ s	tSND ≦ 16 μ s

(B) Definition of distributed refresh

Definition of CBR distributed refresh (Including extended refresh)

The CBR distributed refresh performs more then 1024 constant period (125 us max) CBR cycles within 128 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of nine row adress signals (A0 - A9) are selected during 1024 constant period (16 us max) $\overline{RAS}$ only refresh cycles within 16.4 ms.

Note : Hidden refresh may be used instead of CBR refresh , $\overline{RAS}$ /$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh .

1.1.1 . CBR distributed Refresh

- Switching from read / write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read / write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refres operation should be set within tNSD (shown in table 2)
- Switching from self refresh operation to read / write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read / write operation period should be set within tSND (shown in table 2)

1.1. 2 . $\overline{RAS}$ only distributed refresh

- Switching from read / write operation to self refresh operation.
  The time interval tNSD from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read / write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μ s .
- Switching from self refresh operation to read / write operation.
  The time interval tSND from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read / write operation period should be set within 16 μ s .

1.2 Burst refresh during Read / Write operation

(A) Timing diagram

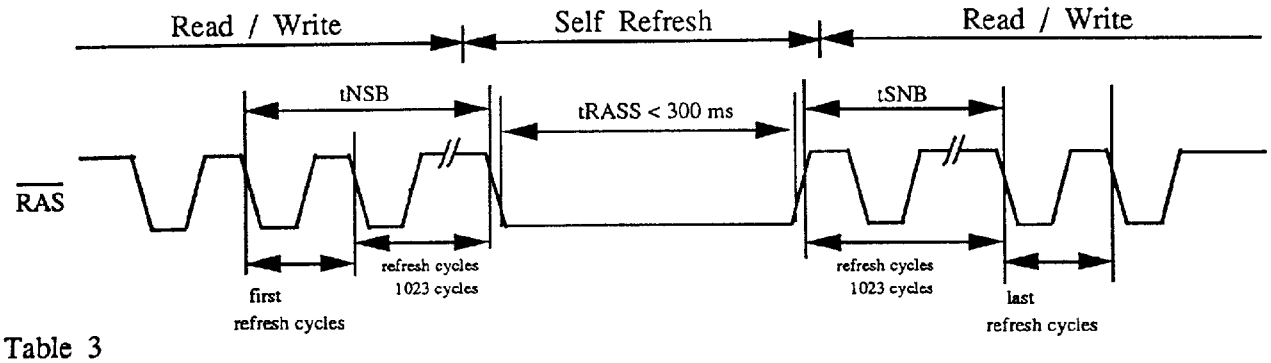


Table 3

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR burst refresh	tNSB ≦ 16.4m s	tSNB ≦ 16.4m s
$\overline{RAS}$ only burst refresh	tNSB + tSNB ≦ 16.4 m s	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row adress signals (A0 - A9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 . CBR distributed Refresh

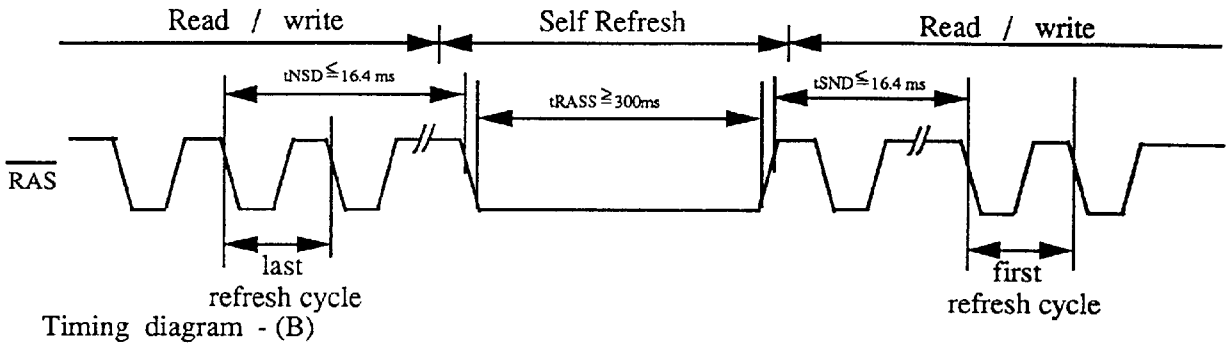
- Switching from read / write operation to self refresh operation.
  The time interval tNSB from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read / write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms .
- Switching from self refresh operation to read / write operation.
  The time interval tSNB from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read / write operation period should be set within 16.4 ms.

1.2.2 . $\overline{RAS}$ only distributed refresh

- Switching from read / write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read / write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within tNSB (shown in table 3)
- Switching from self refresh operation to read / write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read / write operation period should be set within tSNB (shown in table 3)

2. In case of tRASS ≧ 3 0 0 ms

Timing diagram - (A)



Timing diagram - (B)

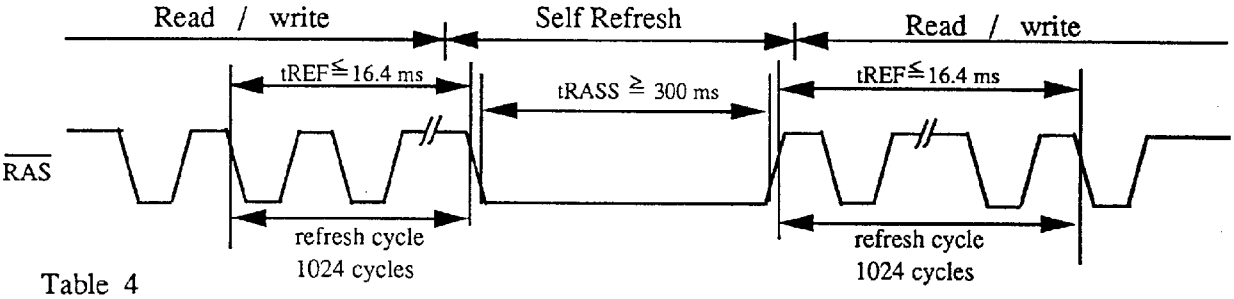


Table 4

Read / Write Cycle	Read / Write ⟶ Self Refresh	Self Refresh ⟶ Read / Write
CBR distributed refresh	Timing Diagram − A	Timing Diagram − A
$\overline{RAS}$ only distributed CBR burst refresh $\overline{RAS}$ only burst refresh	Timing Diagram − B	Timing Diagram − B

(B) Definition of refresh

The same as 1.1 - (B) and 1.2 - (B).

2.1.1 CBR distributed refresh

- Switing from read / write operation to self refresh operation .
  The time interval tNSD from the falling edge of $\overline{RAS}$ signal in the last CBR refreh cycle during read / write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms .
- Switing from self refresh operation to read / write operation .
  The time interval tSND from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read / write operation period should be set within 16.4 ms .

2.1.2 $\overline{RAS}$ only distributed , CBR burst , $\overline{RAS}$ only burst refresh

- Before and after the self refresh , 1024 refresh cycles should be executed within 16.4 ms for each refresh operation .