



3.3V CMOS 16-BIT BUS TRANSCIVER/REGISTER WITH ZERO HOLD TIME, 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC16Z646A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC16Z646A:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

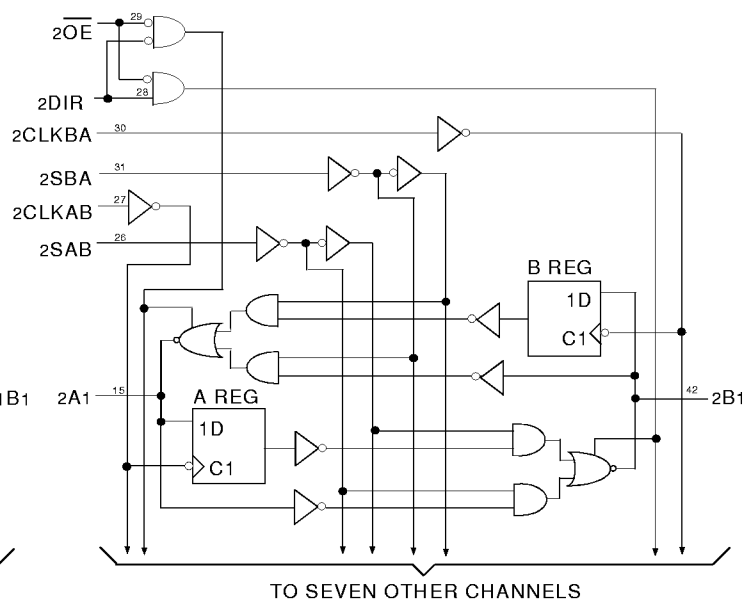
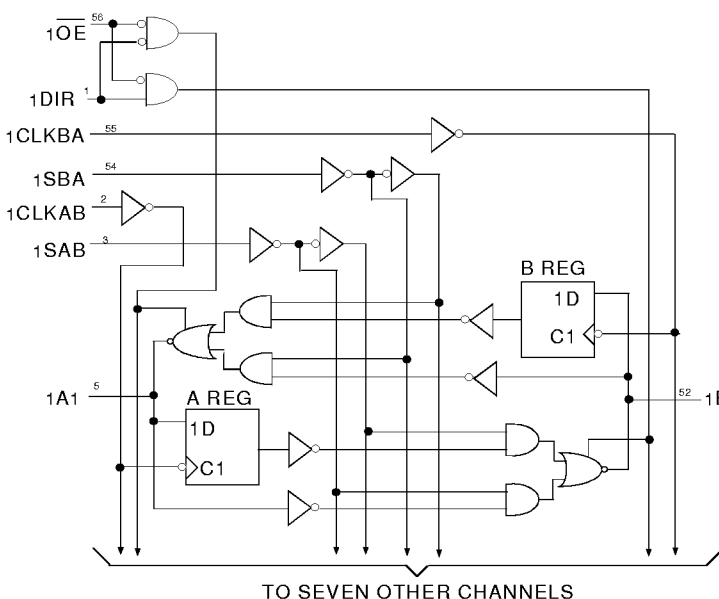
DESCRIPTION:

The LVC16Z646A 16-bit bus transceiver/register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between the A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (DIR), over-riding Output Enable control ($\overline{OE}$) and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

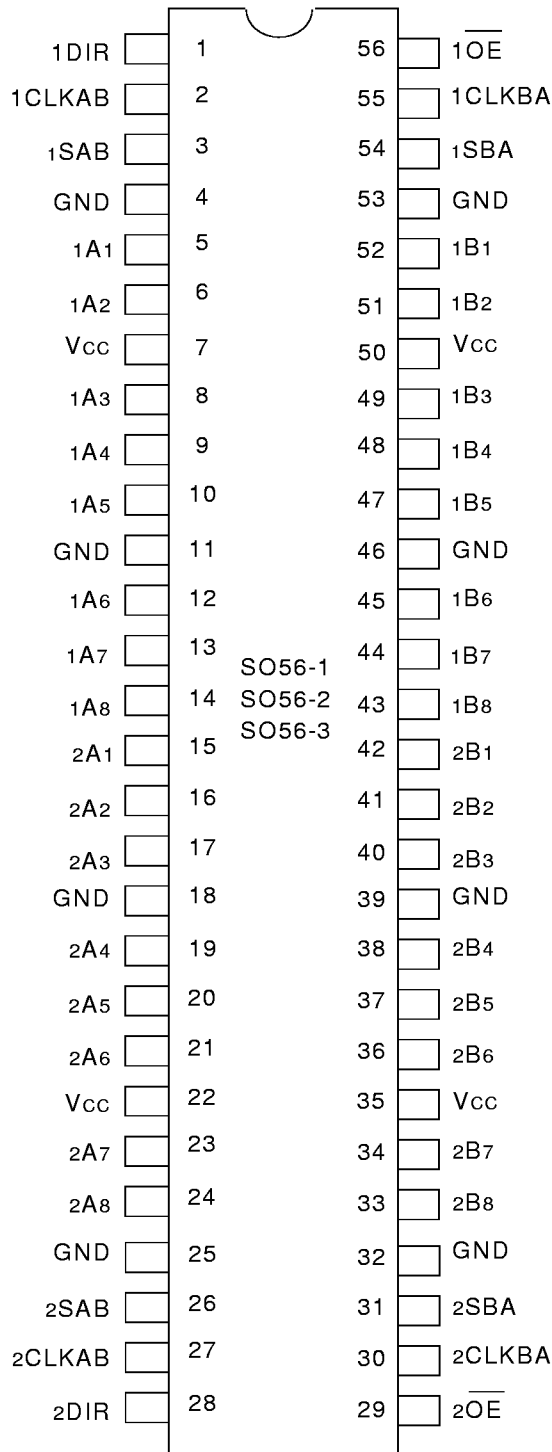
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16Z646A has been designed with a $\pm 24mA$ output driver. The driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
TSTG	Storage Temperature	– 65 to +150	°C
IOUT	DC Output Current	– 50 to +50	mA
IIK IOL	Continuous Clamp Current, VI < 0 or VO < 0	– 50	mA
ICC ISS	Continuous Current through each VCC or GND	± 100	mA

LVC Link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	6.5	8	pF
CI/O	I/O Port Capacitance	VIN = 0V	6.5	8	pF

LVC Link

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B 3-State Outputs
xBx	Data Register B Inputs Data Register A 3-State Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOE	Output Enable Inputs (Active LOW)
xDIR	Direction Control Inputs

FUNCTION TABLE (1)

Inputs						Data I/O ⁽¹⁾		Operation or Function
$\overline{xOE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
X	X	↑	X	X	X	Input	Unspecified ⁽²⁾	Store A, B unspecified ⁽²⁾
X	X	X	↑	X	X	Unspecified ⁽²⁾	Input	Store B, A unspecified ⁽²⁾
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

NOTES:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↑ = LOW-to-HIGH Transition

2. The data output functions may be enabled or disabled by various signals at the $\overline{xOE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

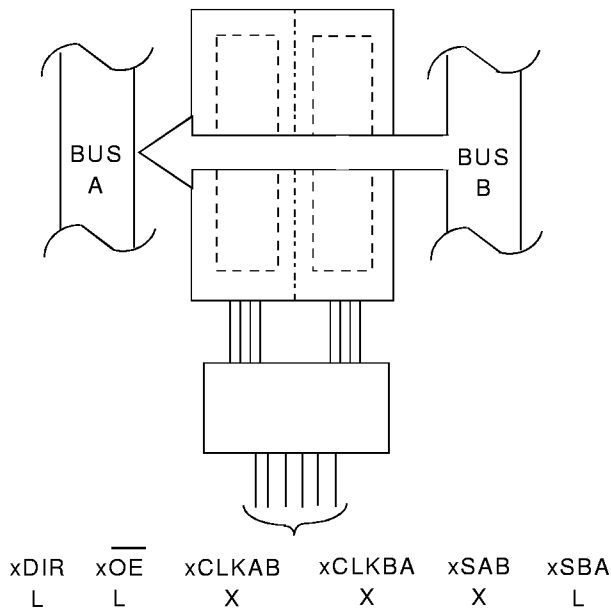
Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = − 18mA		—	− 0.7	− 1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCCL} I _{CCCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND		—	—	500	μA

LVC Link

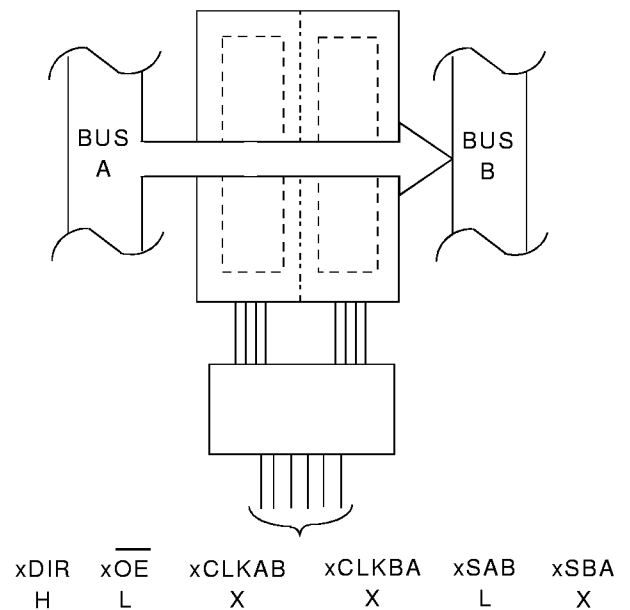
NOTES:

1. Typical values are at VCC = 3.3V, +25°C ambient.

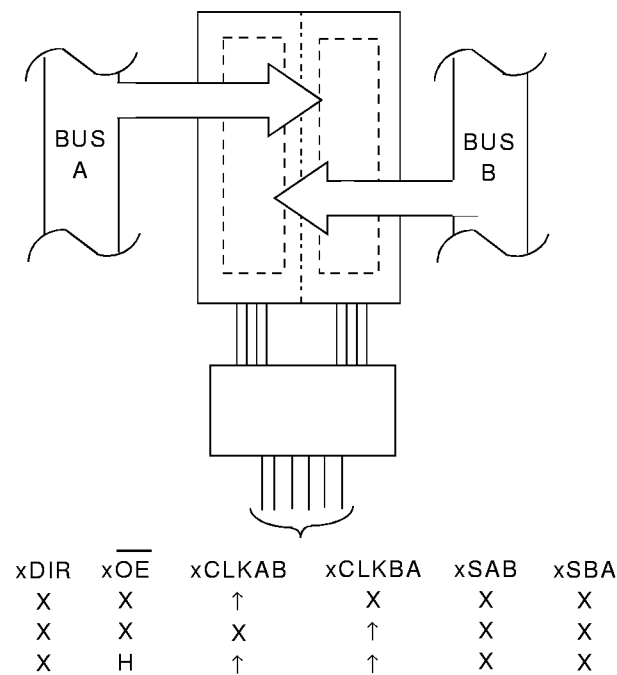
2. This applies in the disabled state only.



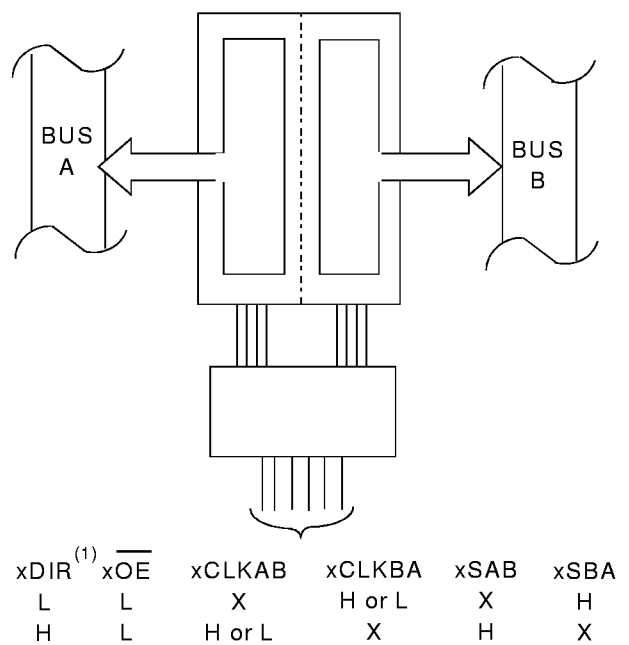
**REAL-TIME TRANSFER
 BUS B TO A**



**REAL-TIME TRANSFER
 BUS A TO B**



**STORAGE FROM
 A, B, OR A AND B**



**TRANSFER STORED
 DATA TO A AND/OR B**

NOTE:

1. Cannot transfer data to A Bus and B Bus simultaneously.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = - 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

LVC Link

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to +85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	CL = 0pF, f = 10Mhz	—	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		—	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	VCC = 2.7V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xAx to xBx or xBx to xAx	2	6	2	5	ns
tPLH tPHL	Propagation Delay CLKBA to xAx or CLKAB to xBx	2	7	2	6	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to xAx or xBx	2	7	2	6	ns
tPZH tPZL	Output Enable Time xOE to xAx or xBx	2	8.5	2	7.5	ns
tPZH tPZL	Output Enable Time xDIR to xAx or xBx	2	8.5	2	7.5	ns
tPHZ tPLZ	Output Disable Time xOE to xAx or xBx	2	7	2	6	ns
tPHZ tPLZ	Output Disable Time xDIR to xAx or xBx	2	7	2	6	ns
tsu	Set-up Time HIGH or LOW xAx or xBx before CLKAB↑ or CLKBA↑	3.5	—	3	—	ns
th	Hold Time HIGH or LOW xAx or xBx after CLKAB↑ or CLKBA↑	0	—	0	—	ns
tw	Clock Pulse Width HIGH or LOW	3	—	3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

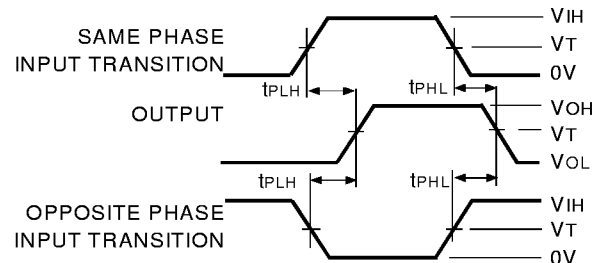
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V ±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

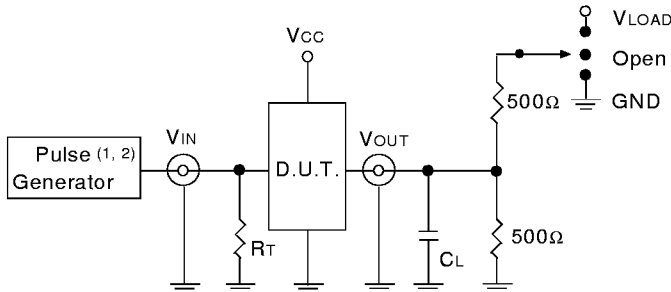
LVC Link

PROPAGATION DELAY



LVC Link

TEST CIRCUITS FOR ALL OUTPUTS



LVC Link

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

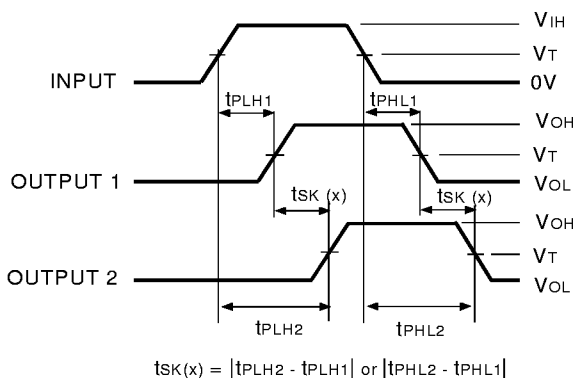
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

LVC Link

OUTPUT SKEW - t_{SK} (x)

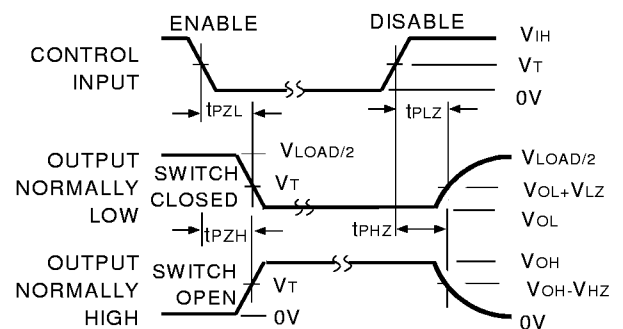


LVC Link

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

ENABLE AND DISABLE TIMES

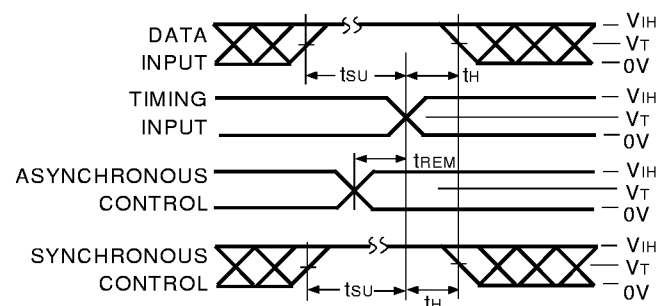


LVC Link

NOTE:

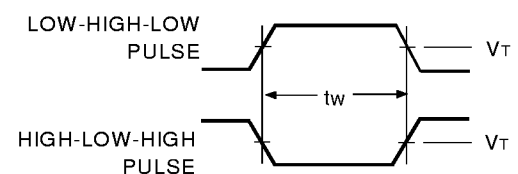
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



LVC Link

PULSE WIDTH



LVC Link

ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					646A		16-Bit Bus Transceiver/Register with Zero Hold Time, 3-State Outputs, 5V Tolerant I/O
					16Z		Double-Density with Resistors, $\pm 24\text{mA}$
						Blank	No Bus-hold
						74	-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.