HB56TW132D Series

1,048,576-word × 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-
Rev. 0.0
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Description

The HB56TW132D is a 1 M × 32 dynamic RAM Small Outline DIMM (S. O. DIMM), mounted 8 pieces of 4-Mbit DRAM (HM51W4400BTT/ BLTT) sealed in TSOP package. An outline of the HB56TW132D is 72-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56TW132D makes high density mounting possible without surface mount technology. The HB56TW132D provides common data inputs and outputs. Decoupling capacitors are mounted beside the each TSOP of its module board.

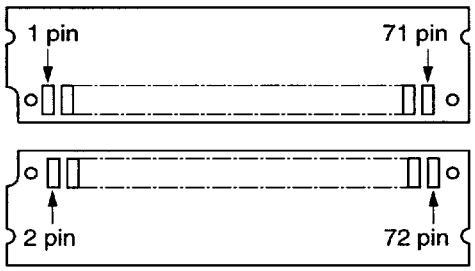
Features

- 72-pin
  - — Lead pitch: 1.27 mm
- Single 3.3 V (± 0.3 V) supply
- High speed
  - — Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode: 2.30 W/2.02 W/1.73 W (max)
  - — Standby mode: 57.6 mW (max)
    2.88 mW (max) (L-version)
- Fast page mode capability
- 1024 refresh cycle : 16 ms
  : 128 ms (L-version)
- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Self refresh (L-version)
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact Pad
HB56TW132D-6B	60 ns	72-pin Small outline DIMM	Gold
HB56TW132D-7B	70 ns		
HB56TW132D-8B	80 ns		
HB56TW132D-6BL	60 ns		
HB56TW132D-7BL	70 ns		
HB56TW132D-8BL	80 ns		

Pin Arrangement



Pin Assignment

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	37	DQ18	2	DQ0	38	DQ19
3	DQ1	39	V_{SS}	4	DQ2	40	$\overline{CE0}$
5	DQ3	41	$\overline{CE2}$	6	DQ4	42	$\overline{CE3}$
7	DQ5	43	$\overline{CE1}$	8	DQ6	44	$\overline{RE0}$
9	DQ7	45	NC	10	V_{CC}	46	NC
11	PD1	47	$\overline{WE}$	12	A0	48	NC
13	A1	49	DQ20	14	A2	50	DQ21
15	A3	51	DQ22	16	A4	52	DQ23
17	A5	53	DQ24	18	A6	54	DQ25
19	NC	55	NC	20	NC	56	DQ27
21	DQ9	57	DQ28	22	DQ10	58	DQ29
23	DQ11	59	DQ31	24	DQ12	60	DQ30
25	DQ13	61	V_{CC}	26	DQ14	62	DQ32
27	DQ15	63	DQ33	28	A7	64	DQ34
29	NC	65	NC	30	V_{CC}	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	$\overline{RE2}$	70	PD6
35	DQ16	71	PD7	36	NC	72	V_{SS}

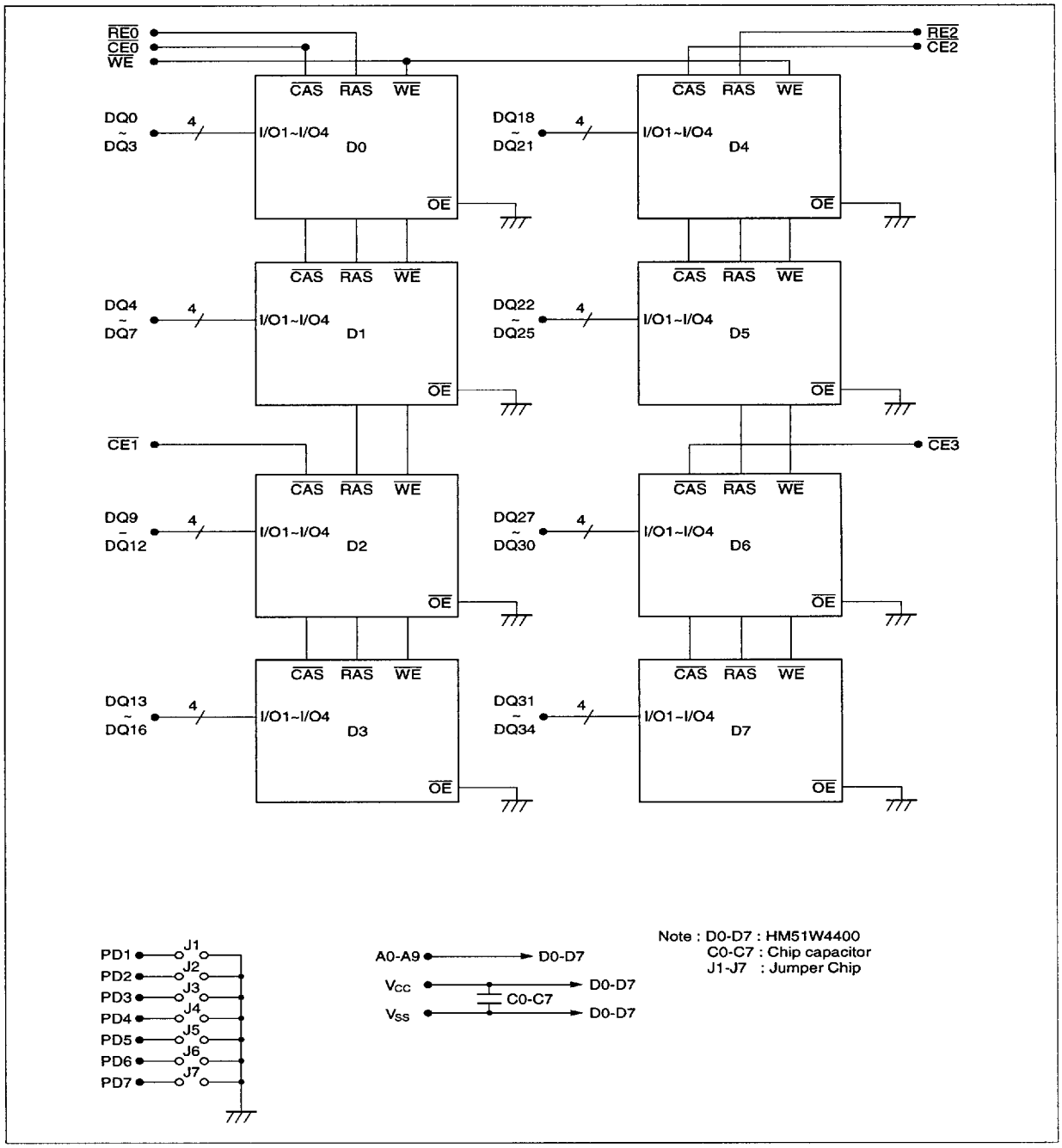
Pin Description

Pin name	Function
A0 - A9	Address input
A0 - A9	Refresh address input
DQ0 - DQ7 DQ9 - DQ16 DQ18 - DQ25 DQ27 - DQ34	Data-in/data-out
$\overline{CE0}$ - $\overline{CE3}$	Column address strobe ($\overline{CAS}$)
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{WE}$	Read/write enable
V_{cc}	Power supply
V_{ss}	Ground
PD1 - PD7	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56TW132D					
Pin name	Pin No.	-6B	-7B	-8B	-6BL	-7BL	-8BL
11	PD1	NC	NC	NC	NC	NC	NC
66	PD2	V_{ss}	V_{ss}	V_{ss}	V_{ss}	V_{ss}	V_{ss}
67	PD3	V_{ss}	V_{ss}	V_{ss}	V_{ss}	V_{ss}	V_{ss}
68	PD4	NC	NC	NC	NC	NC	NC
69	PD5	NC	V_{ss}	NC	NC	V_{ss}	NC
70	PD6	NC	NC	V_{ss}	NC	NC	V_{ss}
71	PD7	NC	NC	NC	V_{ss}	V_{ss}	V_{ss}

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	−0.5 to +4.6	V
	(Output)	Vout	−0.5 to +4.6	V
Supply voltage relative to V_{SS}		V_{CC}	−0.5 to +4.6	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	8	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltatge	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)*4

		HB56TW132D								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	640	—	560	—	480	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}-0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	0.8	—	0.8	—	0.8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, address, Din = V_{IH} or V_{IL} Dout = High-Z	4
$\overline{RAS}$-only refresh current	I_{CC3}	—	640	—	560	—	480	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	32	—	32	—	32	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC6}	—	640	—	560	—	480	mA	t_{RC} = min	
First page mode current	I_{CC7}	—	640	—	560	—	480	mA	t_{PC} = min	1, 3
Battery backup operation current (CBR refresh) (L-version)	I_{CC10}	—	1.2	—	1.2	—	1.2	mA	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL} address, Din = V_{IH} or V_{IL} Dout = High-Z	4
Self refresh mode current (L-version)	I_{CC11}	—	0.8	—	0.8	—	0.8	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IL} $\overline{WE}$, address, Din = V_{IH} or V_{IL}	4
Input leakage current	I_{LI}	−10	10	−10	10	-10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	−10	10	−10	10	-10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V_{CC}	2.4	V	High Iout = −2.0 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2.0 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} - 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	68	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

- Refer to the HM51W4400B Series data sheet.
- The HB56TW132D Series writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
  Delayed write cycle is not available ($\overline{OE}$ pin is fixed to V_{SS}).

Physical Outline

Unit: mm