PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD78F9801

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9801 is a μPD789800 sub-series product (for a USB keyboard) of the 78K/0S series.

The μPD78F9801 replaces the internal masked ROM of the μPD789800 with flash memory, which enables the writing/erasing of a program while the device is mounted on the board.

Because the device can be programmed by the user, it is ideally suited to the evaluation stages of system development, the manufacture of small batches of multiple products, and the rapid development of new products.

The functions of this microcontroller are described in the following user's manuals. Refer to these manuals when designing a system based on this microcontroller.

μPD789800 Sub-Series User's Manual: To be prepared

78K/0S Series User's Manual - Instruction: U11047E

FEATURES

- Pin-compatible with masked ROM version (excluding V_{PP} pin)
- Flash memory: 16K bytes
- Internal high-speed RAM: 256 bytes
- Operable on the same supply voltage as masked ROM version (V_{DD} = 4.0 to 5.5 V)

Remark The differences between the flash memory and masked ROM versions are summarized in **Chapter 3**.

APPLICATIONS

USB keyboards

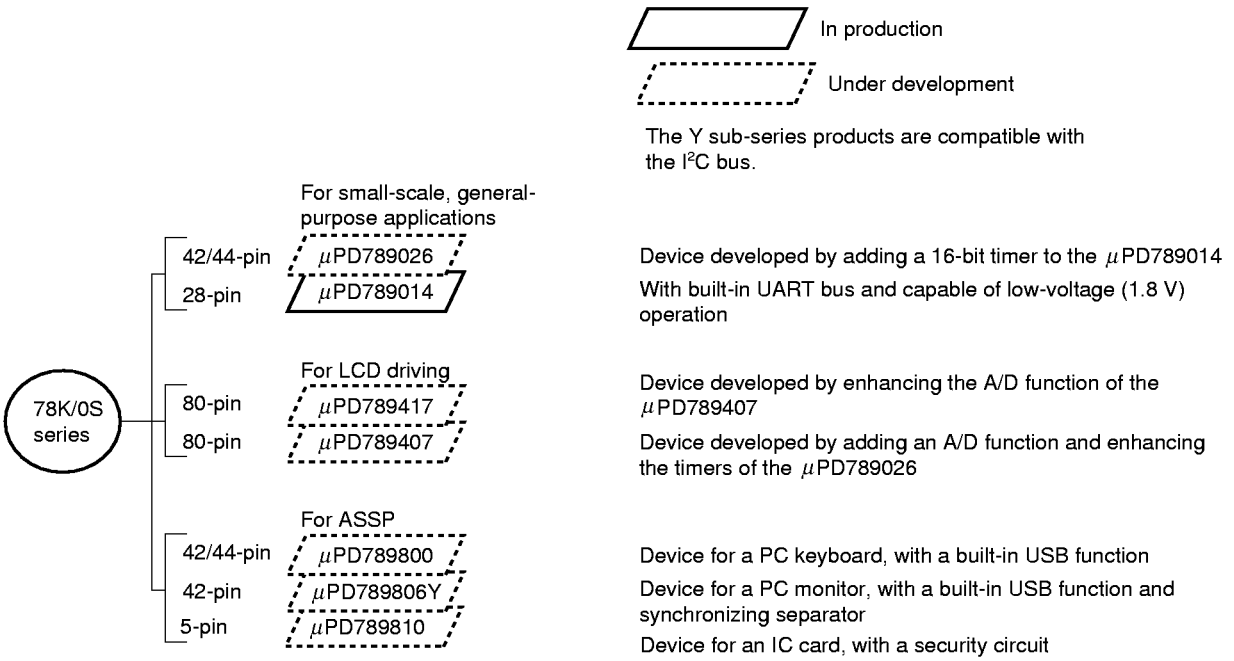
ORDERING INFORMATION

Part number	Package	Internal ROM
μPD78F9801CU	42-pin plastic shrink DIP (600 mil)	Flash memory
μPD78F9801GB-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Flash memory

Document No. U13999EJ1V0PM00 (1st edition)

78K/0S SERIES DEVELOPMENT

The 78K/0S series products are shown below. The sub-series names are indicated in frames.



The following table lists the major differences in functions between the sub-series.

Sub-series \ Function		ROM size	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	Minimum V_{DD} value
			8-bit	16-bit	Clock	WDT						
Small-scale general purpose	μPD789026	4 K-16 K	1 ch	1 ch	-	1 ch	-	-	-	1 ch (UART: 1 ch)	34 pins	1.8 V
	μPD789014	2 K-4 K	2 ch	-							22 pins	
LCD driving	μPD789417	12 K-24 K	3 ch	1 ch	1 ch	1 ch	-	7 ch	-	1 ch (UART: 1 ch)	43 pins	1.8 V
	μPD789407	12 K-24 K					7 ch	-				
ASSP	μPD789800	8 K	2 ch	-	-	1 ch	-	-	-	2 ch (USB: 1 ch)	31 pins	4.0 V
	μPD789806Y	16 K	2 ch	-	-	1 ch	-	-	-	2 ch (USB: 1 ch, I²C: 1 ch)	20 pins	4.5 V
	μPD789810	6 K	-	-	-	1 ch	-	-	-	-	1 pin	1.8 V

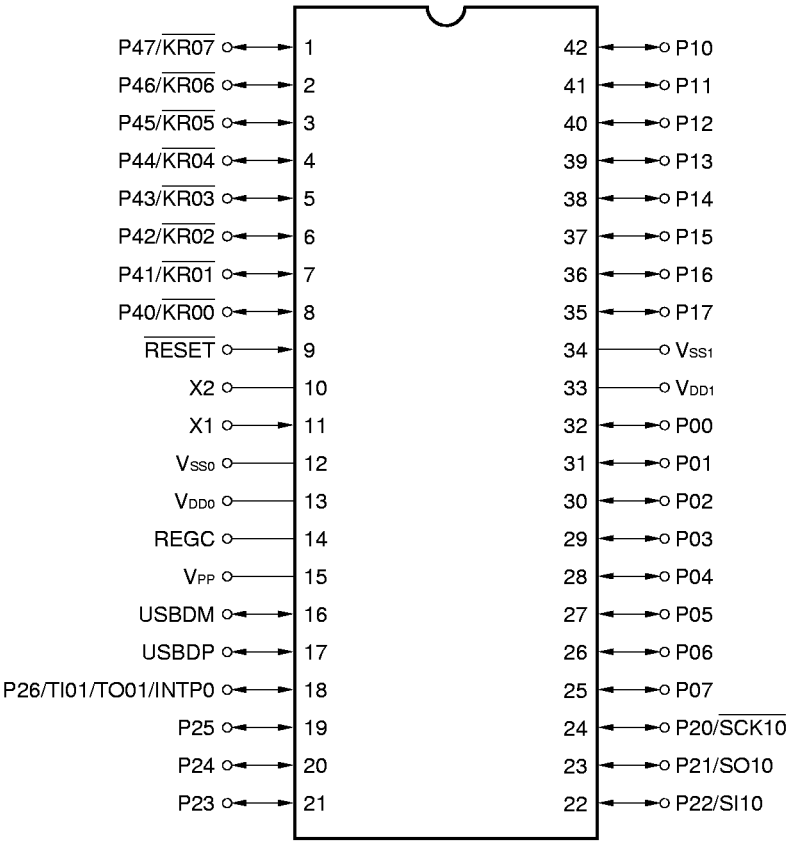
FUNCTIONS

Item		Function
Internal memory	Flash memory	16K bytes
	High-speed RAM	256 bytes
Instruction cycle		Incorporates the function that can change the instruction execution time. 0.33 μs/1.33 μs (when the main system clock operates at 6.0 MHz)
Instruction set		• 16-bit operation • Bit manipulation (set, reset, and test) etc.
I/O ports		Total 31 CMOS I/O 31 (Of the above COMS I/O ports, 18 ports can be switched to N-ch open-drain I/O ports.)
Serial interface		• USB (universal serial bus) function: 1 channel • 3-wire serial I/O mode: 1 channel
Timer		• 8-bit timer 00: 1 channel • 8-bit timer/event counter 01: 1 channel • Watchdog timer: 1 channel
Regulator		Incorporated (V_{REG} = 3.3 ± 0.3 V)
Vector interrupt source	Maskable	Internal: 9, external: 1
	Nonmaskable	Internal: 1
Power supply voltage		V_{DD} = 4.0 to 5.0 V
Operating ambient temperature		• T_A = -40 to +85 °C (when the USB is not operating) • T_A = 0 to +70 °C (when the USB is operating) • T_A = 0 to +50 °C (when a flash memory is written)
Package		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)

CONTENTS

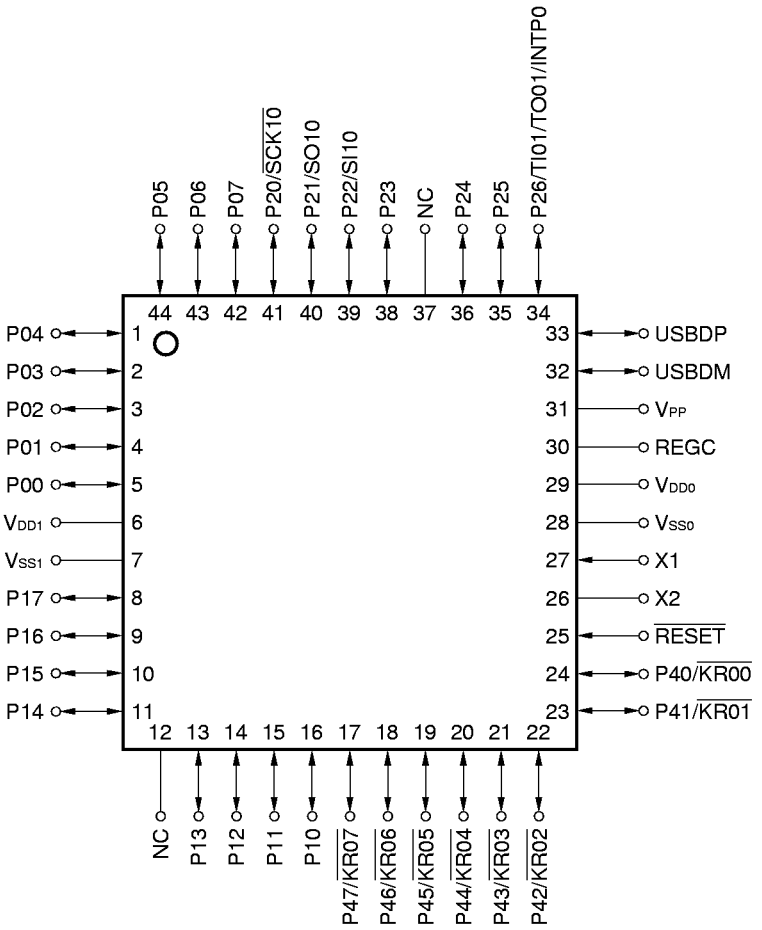
1. PIN CONFIGURATION (TOP VIEW)

- 42-pin plastic shrink DIP (600 mil)
  μPD78F9801CU



Caution In normal operation mode, connect the V_{PP} pin directly to the V_{SS0} pin.

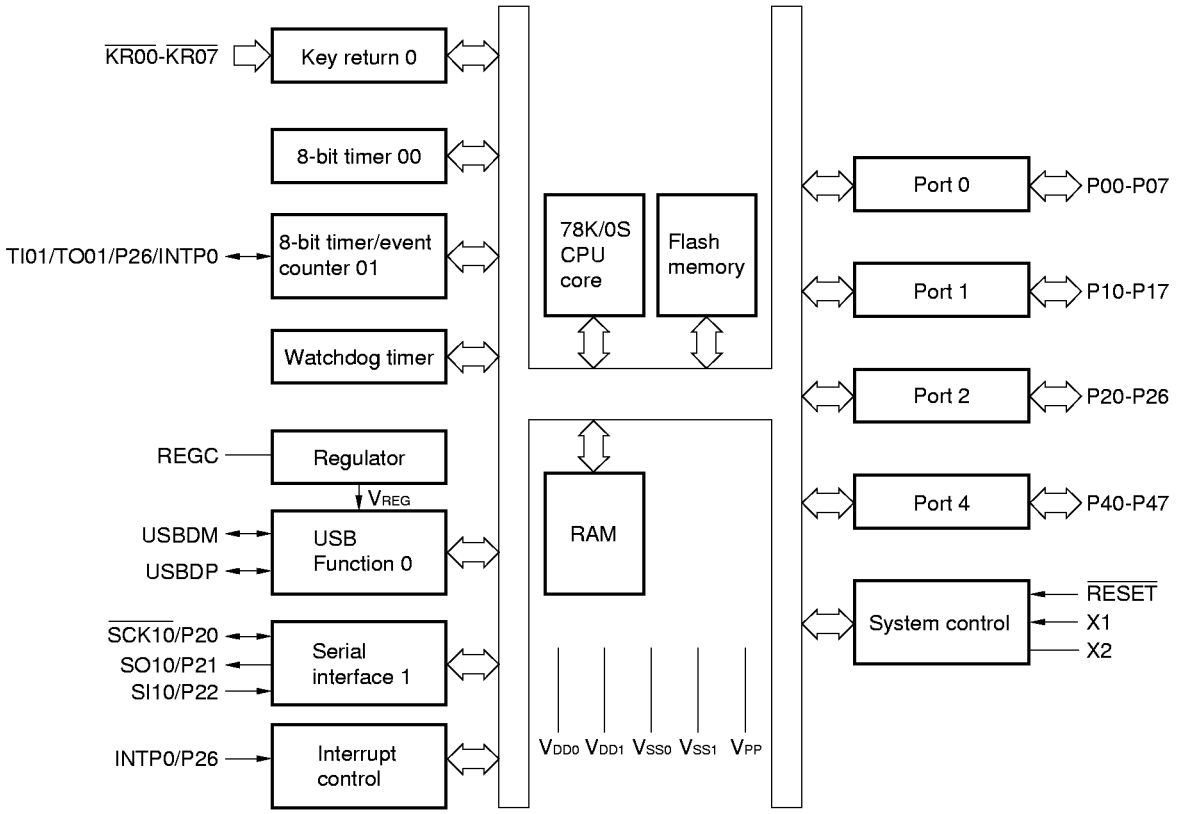
- 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)
  μPD78F9801GB-3BS-MTX



Caution In normal operation mode, connect the V_{PP} pin directly to the V_{SS0} pin.

INTP0	: Interrupt from peripherals	SO10	: Serial data output
KR00 - KR07	: Key return	TI01	: Timer input
NC	: No connection	TO01	: Timer output
P00-P07	: Port 0	USBDM, USBDP	: Universal serial bus data
P10-P17	: Port 1	V_{DD0}	: Port power supply
P20-P26	: Port 2	V_{DD1}	: Power supply
P40-P47	: Port 4	V_{PP}	: Programming power supply
RESET	: Reset	V_{SS0}	: Port ground
REGC	: Voltage regulator for USB function	V_{SS1}	: Ground
SCK10	: Serial clock input/output	X1, X2	: Crystal
SI10	: Serial data input		

2. BLOCK DIAGRAM



3. DIFFERENCES BETWEEN THE μPD78F9801 AND MASKED ROM VERSION

The μPD78F9801 incorporates flash memory which enables the writing/erasing of a program while the device is mounted on the board.

Table 3-1 lists the differences between the μPD78F9801 and masked ROM version.

Table 3-1. Differences between the μPD78F9801 and Masked ROM Version

Item	μPD78F9801	Masked ROM version
ROM type	Flash memory	Masked ROM
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
Electrical characteristics (target values)	Refer to the Preliminary Product Information supplied for individual products.	

4. PIN FUNCTIONS

4.1 Port Pins

Pin name	I/O	Function	When reset	Also used as
P00-P07	I/O	Port 0 8-bit input/output port Can be set to either input or output in 1-bit units. When being used as an input port, whether the built-in pull-up resistor is to be used can be specified by software. Can be set to either CMOS output or N-ch open-drain output in 8-bit units.	Input	-
P10-P17	I/O	Port 1 8-bit input/output port Can be set to either input or output in 1-bit units. When being used as an input port, whether the built-in pull-up resistor is to be used can be specified by software. Can be set to either CMOS output or N-ch open-drain output in 8-bit units.	Input	-
P20	I/O	Port 2 7-bit input/output port Can be set to either input or output in 1-bit units. When being used as an input port, whether the built-in pull-up resistor is to be used can be specified by software. Only P25 and P26 can be set to either CMOS output or N-ch open-drain output in 1-bit units.	Input	$\overline{SCK10}$
P21				SO10
P22				SI10
P23-P25				-
P26				INTP0/TI01/TO01
P40-P47	I/O	Port 4 8-bit input/output port Can be set to either input or output in 1-bit units. When being used as an input port, whether the built-in pull-up resistor is to be used can be specified by software.	Input	$\overline{KR00}$ - $\overline{KR07}$

4.2 Non-Port Pins

Pin name	I/O	Function	When reset	Also used as
INTP0	Input	External interrupt request input for which effective edges (rising and/or falling edges) can be specified	Input	P26/TI01/TO01
$\overline{KR00}$ - $\overline{KR07}$	Input	Input for detecting key return signals	Input	P40-P47
NC	-	No connection. Can be left open.	-	-
REGC	-	Internally generated power supply for driving USB driver/receiver. Connect this pin to V_{SS} through a 0.1-μF capacitor.	-	-
$\overline{RESET}$	Input	System reset input	Input	-
$\overline{SCK10}$	I/O	Serial clock input/output for serial interface	Input	P20
SI10	Input	Serial data input for serial interface	Input	P22
SO10	Output	Serial data output for serial interface	Input	P21
TI01	Input	External count clock input to 8-bit timer TM01	Input	P26/INTP0/TO01
TO01	Output	Output from 8-bit timer TM01	Input	P26/INTP0/TI01
USBDM	I/O	Serial data input/output (negative side) for USB function. The pull-up resistor (1.5 kΩ) for the USBDM pin must be connected to the REGC pin.	Input	-
USBDP	I/O	Serial data input/output (positive side) for USB function	Input	-
V_{DD0}	-	Positive supply voltage for ports	-	-
V_{DD1}	-	Positive supply voltage for circuits other than ports	-	-
V_{PP}	-	Pin for setting flash memory programming mode. Apply a high voltage to write or verify a program.	-	-
V_{SS0}	-	Ground potential for ports	-	-
V_{SS1}	-	Ground potential for circuits other than ports	-	-
X1	Input	Connected to crystal for main system clock oscillator	Input	-
X2	-		-	

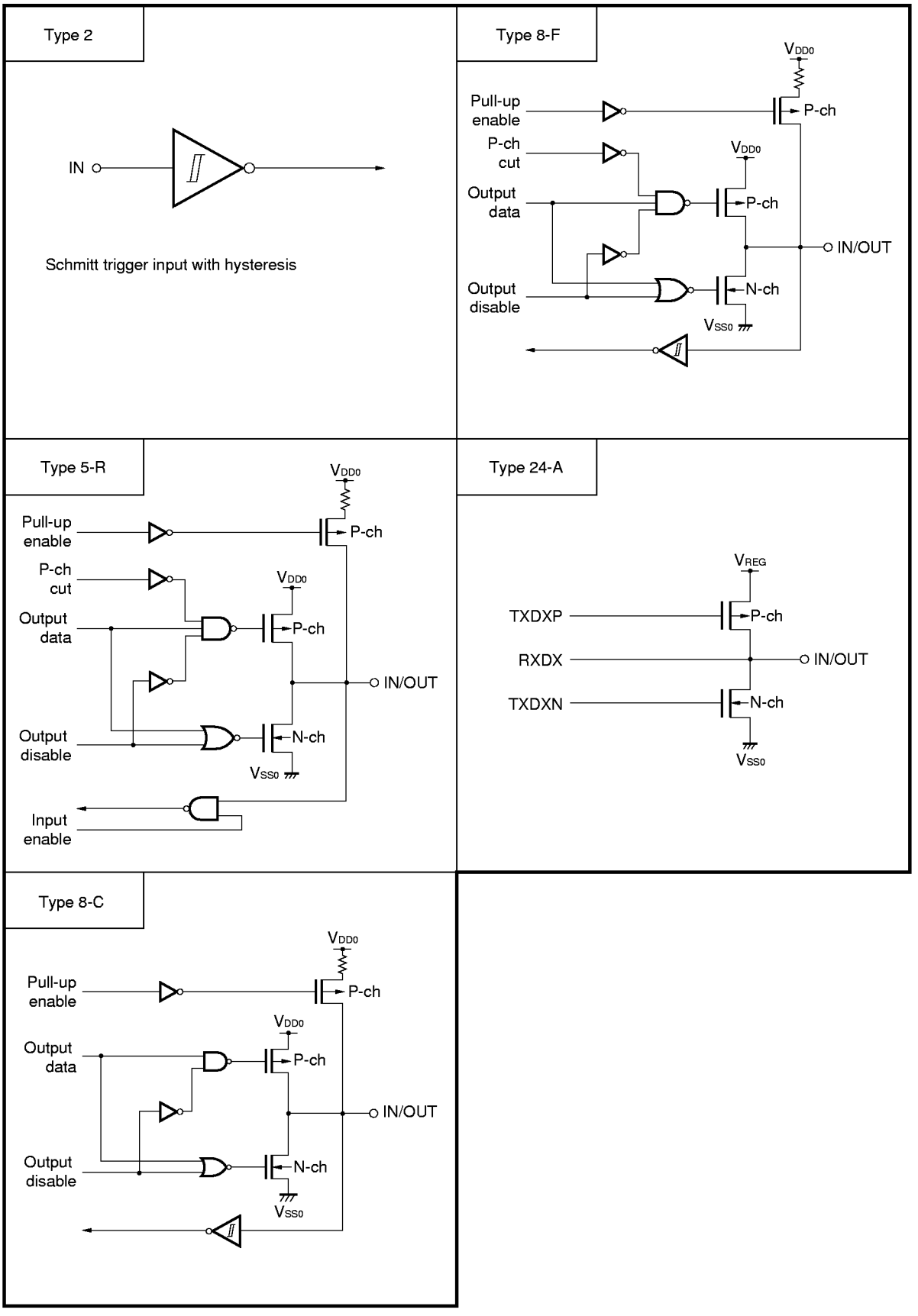
4.3 Pin Input/Output Circuits and Handling of Unused Pins

Table 4-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.
Figure 4-1 shows the configuration of each type of input/output circuit.

Table 4-1. Type of Input/Output Circuit for Each Pin

Pin name	I/O circuit type	I/O	Recommended connection of unused pins
P00-P07	5-R	I/O	Separately connected to V_{DD} or V_{SS} via respective resistors
P10-P17			
P20/$\overline{SCK10}$	8-C		
P21/SO10			
P22/SI10			
P23, P24			
P25	8-F		
P26/INTP0/TI01/TO01			Separately connected to V_{SS} via respective resistors
P40/$\overline{KR00}$ -P47/$\overline{KR07}$	8-C		Separately connected to V_{DD} or V_{SS} via respective resistors
USBDM	24-A		Connected to REGC pin
USBDP			Separately connected to V_{SS} via respective resistors
$\overline{RESET}$	2	Input	-
NC	-	-	Open
REGC	-	-	Connected to USBDM pin
V_{PP}	-	-	Connected directly to V_{SS}

Figure 4-1. Pin Input/Output Circuits



5. FLASH MEMORY PROGRAMMING

Flash memory is used as the built-in program memory of the μPD78F9801.

The flash memory can be written even while the device is installed in the target system (on-board write). To write a program into the flash memory, connect the dedicated flash writer (Flashpro II) to both the host machine and target system.

Remark The Flashpro II (formerly, Flashpro) is manufactured by Naito Densei Machida Seisakusho Co., Ltd.

5.1 Selecting the Transmission Method

The Flashpro II writes into flash memory by means of serial transmission. The transmission method to be used for writing is selected from those listed in Table 5-1. To select a transmission method, use the format shown in Figure 5-1, according to the number of V_{PP} pulses listed in Table 5-1.

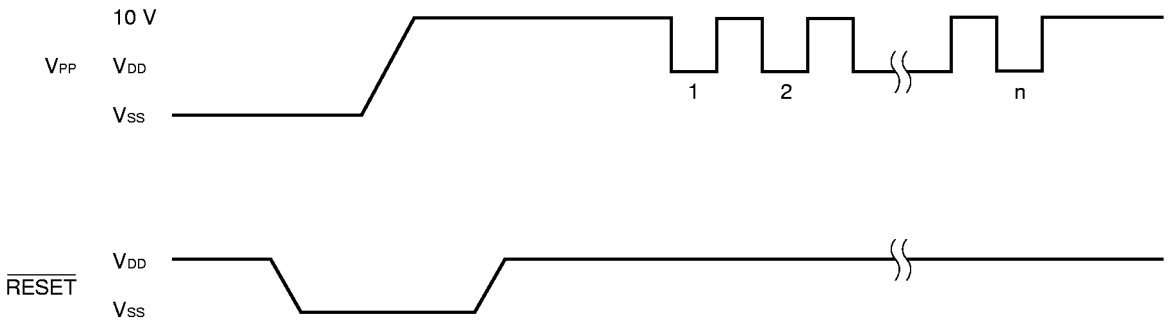
Table 5-1. Transmission Methods

Transmission method	Number of channels	Pins	Number of V_{PP} pulses
3-wire serial I/O	1	$\overline{SCK10}$ /P20 SO10/P21 SI10/P22	0
Pseudo 3-wire mode[Note]	2	P15 (serial clock input) P16 (serial data output) P17 (serial data input)	12
		P45/$\overline{KR05}$ (serial clock input) P46/$\overline{KR06}$ (serial data output) P47/$\overline{KR07}$ (serial data input)	13

Note Serial transfer by controlling the ports using software

Caution To select a transmission method, always use the corresponding number of V_{PP} pulses listed in Table 5-1.

Figure 5-1. Transmission Method Selection Format



5.2 Flash Memory Programming Functions

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected transmission method. Table 5-2 lists the main flash memory programming functions.

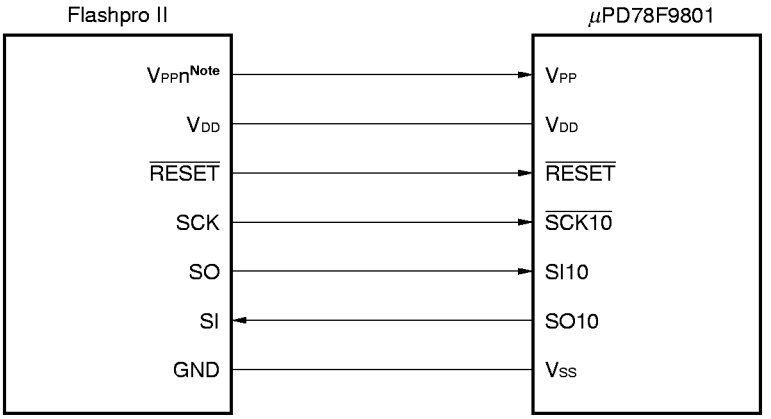
Table 5-2. Main Flash Memory Programming Functions

Function	Description
Batch erase	Erases the entire contents of memory.
Batch blank check	Checks that the entire contents of memory have been erased.
Data write	Write to the flash memory according to the specified write start address and number of bytes of data to be written.
Batch verify	Compares the entire contents of memory with the input data.

5.3 Connecting the Flashpro II

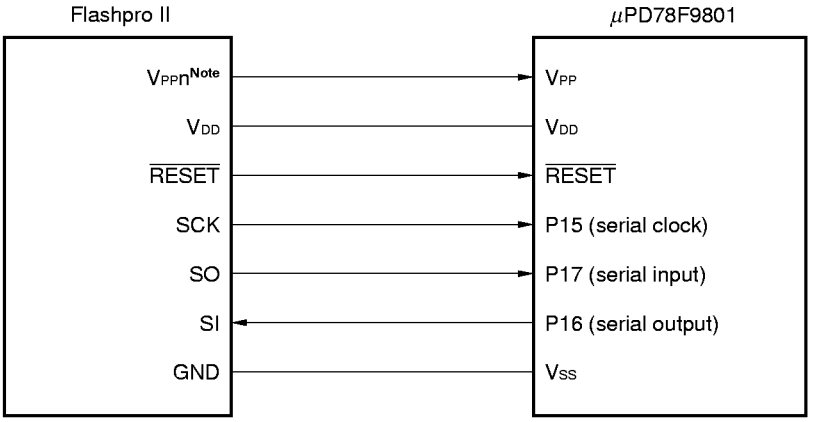
The connection between the Flashpro II and μPD78F9801 varies with the transmission method (3-wire serial I/O or pseudo 3-wire). Figures 5-2 and 5-3 show the connection for each transmission method.

Figure 5-2. Flashpro II Connection in 3-Wire Serial I/O Mode



Note n: 1 or 2

Figure 5-3. Flashpro II Connection in Pseudo 3-Wire Mode (When Port 1 Is Used)



Note n: 1 or 2

6. ELECTRICAL CHARACTERISTICS (TARGET VALUES)

Caution The ratings listed below are target values for the product.
When designing an application system, refer to the following data sheet, which details the formal electrical characteristics:
μPD78F9801 Data Sheet: To be prepared

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}	V_{DD0}, V_{DD1}		-0.3 to +7.0	V
	V_{PP}			-0.3 to +10.8	V
Input voltage	V_{I1}	Pins other than USBDM and USBDP		-0.3 to V_{DD} + 0.3	V
	V_{I2}	USBDM, USBDP		-0.3 to V_{REG} Note + 0.3	V
Output voltage	V_{O1}	Pins other than USBDM and USBDP		-0.3 to V_{DD} + 0.3	V
	V_{O2}	USBDM, USBDP		-0.3 to V_{REG} Note + 0.3	V
Output high current	I_{OH} Note 2	Each pin	Peak value	-10	mA
			rms	-5	mA
		Total for all pins	Peak value	-30	mA
			rms	-15	mA
Output low current	I_{OL} Note 2	Each pin	Peak value	30	mA
			rms	15	mA
		Total for all pins	Peak value	160	mA
			rms	80	mA
Operating ambient temperature	T_A			-40 to +85	°C
Storage temperature	T_{stg}			-65 to +150	°C

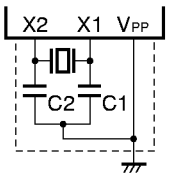
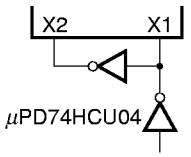
Notes 1. Voltage output to the REGC pin (V_{REG} = 3.0 to 3.6 V)
2. Calculate rms with [rms] = [peak value] × $\sqrt{\text{duty cycle}}$.

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATION CIRCUIT

(T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillator frequency (f_X)[Note 1]			6.0[Note 3]		MHz
		Oscillation settling time[Note 2]				30	ms
External clock		X1 input frequency (f_X)[Note 1]			6.0[Note 3]		MHz
		X1 input high/low level width (t_{XH}, t_{XL})		70		85	ns

Notes 1. Only the characteristics of the oscillation circuit are indicated. See the description of the AC characteristics for the instruction execution time.

2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected.

3. This product has been designed to operate at 6 MHz.

Caution When using the main system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH1}	P00-P07, P10-P17		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P20-P26, P40-P47, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} - 0.1		V_{DD}	V
	V_{IH4}	USBDM, USBDP		2.0		V_{REG}[Note]	V
Input low voltage	V_{IL1}	P00-P07, P10-P17		0		0.3V_{DD}	V
	V_{IL2}	P20-P26, P40-P47, $\overline{\text{RESET}}$		0		0.3V_{DD}	V
	V_{IL3}	X1, X2		0		0.1V_{DD}	V
	V_{IL4}	USBDM, USBDP T_A = 0 to +70 °C		0		0.8	V
Output high voltage	V_{OH1}	Pins other than USBDM and USBDP	I_{OH} = -1 mA	V_{DD} - 1.0			V
			I_{OH} = -100 μA	V_{DD} - 0.5			V
	V_{OH2}	USBDM, USBDP T_A = 0 to +70 °C		2.8			V
Output low voltage	V_{OL1}	Pins other than USBDM and USBDP	I_{OL} = 10 mA			1.0	V
			I_{OL} = 400 μA			0.5	V
	V_{OL2}	USBDM, USBDP T_A = 0 to +70 °C				0.3	V
High-level input leakage current	I_{LIH1}	P00-P07, P10-P17, P20-P26, P40-P47, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	USBDM, USBDP T_A = 0 to +70 °C	0 V ≤ V_{IN} < V_{REG}[Note]			10	μA
Low-level input leakage current	I_{LIL1}	P00-P07, P10-P17, P20-P26, P40-P47, $\overline{\text{RESET}}$	V_{IN} = 0 V			-3	μA
	I_{LIL2}	X1, X2				-20	μA
	I_{LIL3}	USBDM, USBDP T_A = 0 to +70 °C	0 V ≤ V_{IN} < V_{REG}[Note]			-10	μA
High-level output leakage current	I_{LOH1}		V_{OUT} = V_{DD}			3	μA
Low-level output leakage current	I_{LOL1}		V_{OUT} = 0 V			-3	μA
Software pull-up resistance	R_1		V_{IN} = 0 V	50	100	200	kΩ

Note Voltage output to the REGC pin (V_{REG} = 3.0 to 3.6 V)

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Note 1, 2]	I_{DD1}	6-MHz crystal oscillation (operating mode)			9	27	mA
			When the USB function is operating T_A = 0 to +70 °C		19	47	mA
	I_{DD2}	6-MHz crystal oscillation (HALT mode)			4.5	13.5	mA
			When the USB function is operating T_A = 0 to +70 °C		14.5	33.5	mA
	I_{DD3}	STOP mode	When the USB function is disabled		14.5	34.5	μA
			When the USB function is enabled T_A = 0 to +70 °C		64.5	105	μA

Notes 1. The power supply current does not include the current flowing through the built-in pull-up resistor.

2. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H.)

AC CHARACTERISTICS

(1) Basic operations (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock f_X = 6 MHz	PCC = 02 H		1.333		μs
			PCC = 00 H		0.333		μs
TI01 input frequency	t_{TI}			0		4	MHz
TI01 input high/low level width	t_{TIH}, t_{TIL}			0.1			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INTP0		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

(2) Serial interface

(a) USB function (T_A = 0 to +70 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USBDM and USBDP rise time	t_R	C = 50 pF[Note]	75			ns
		C = 350 pF[Note]			300	ns
USBDM and USBDP fall time	t_F	C = 50 pF[Note]	75			ns
		C = 350 pF[Note]			300	ns
Rise/fall time matching	t_{RFM}	t_R/t_F	80		120	%
Differential output signal cross-over point	V_{CRS}		1.3		2.0	V
Data transfer rate	t_{DRATE}	Average bit rate 1.5 Mbps ± 1.5 %	1.4775	1.5000	1.5225	MHz
Transmission differential signal jitter	t_{UDJ1}	Upon transferring the next bit	-95	0	95	ns
	t_{UDJ2}	Upon transferring the bit following the next bit	-150	0	150	ns
Transmission EOP width	t_{EOPT1}		1.25	1.33	1.50	μs
Reception EOP width	t_{EOPR1}	EOP width to be eliminated			300	ns
	t_{EOPR2}	EOP width to be detected	675			ns
Reception USB reset width	t_{URES1}	USB reset width to be eliminated			2.5	μs
	t_{URES2}	USB reset width to be detected	5.5			μs

Note C is the capacitance of the USBDM and USBDP output lines.

(b) Serial interface SIO1 (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

(i) Three-wire serial I/O mode ($\overline{SCK10}$ ...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY1}		667			ns
$\overline{SCK10}$ high/low level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 - 50			ns
SI10 setup time (relative to $\overline{SCK10}$ ↑)	t_{SIK1}		150			ns
SI10 hold time (relative to $\overline{SCK10}$ ↑)	t_{KSI1}		400			ns
Delay between $\overline{SCK10}$ ↓ and SO10 output	t_{KSO1}	C =100 pF[Note], R = 1 kΩ[Note]	0		200	ns

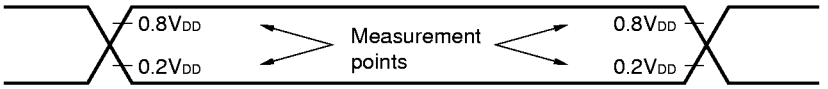
Note C and R are the capacitance and resistance of the SO10 output line, respectively.

(ii) Three-wire serial I/O mode ($\overline{SCK10}$ ...External clock output)

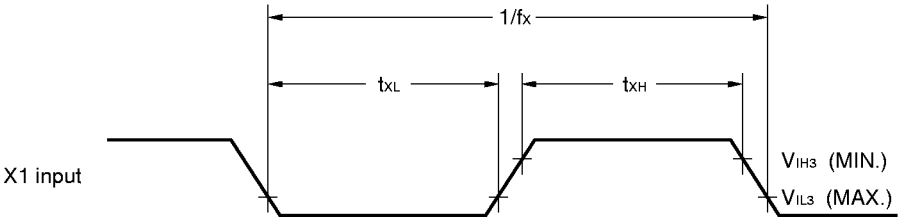
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY2}		667			ns
$\overline{SCK10}$ high/low level width	t_{KH2}, t_{KL2}		400			ns
SI10 setup time (relative to $\overline{SCK10}$ ↑)	t_{SIK2}		100			ns
SI10 hold time (relative to $\overline{SCK10}$ ↑)	t_{KSI2}		400			ns
Delay between $\overline{SCK10}$ ↓ and SO10 output	t_{KSO2}	C =100 pF[Note], R = 1 kΩ[Note]	0		250	ns

Note C and R are the capacitance and resistance of the SO10 output line, respectively.

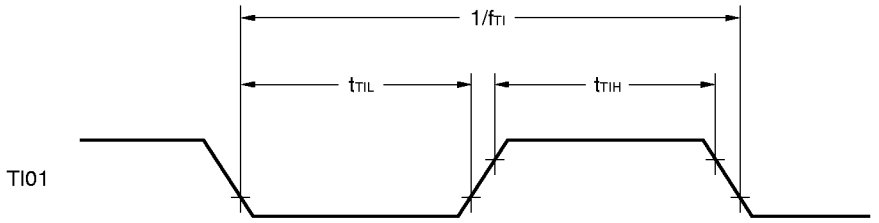
AC TIMING MEASUREMENT POINTS (except the X1 input)



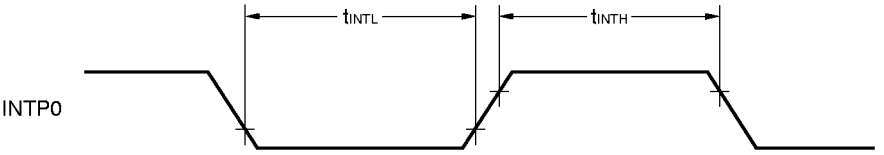
CLOCK TIMING



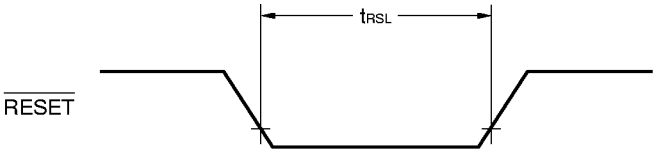
TI TIMING



INTERRUPT INPUT TIMING

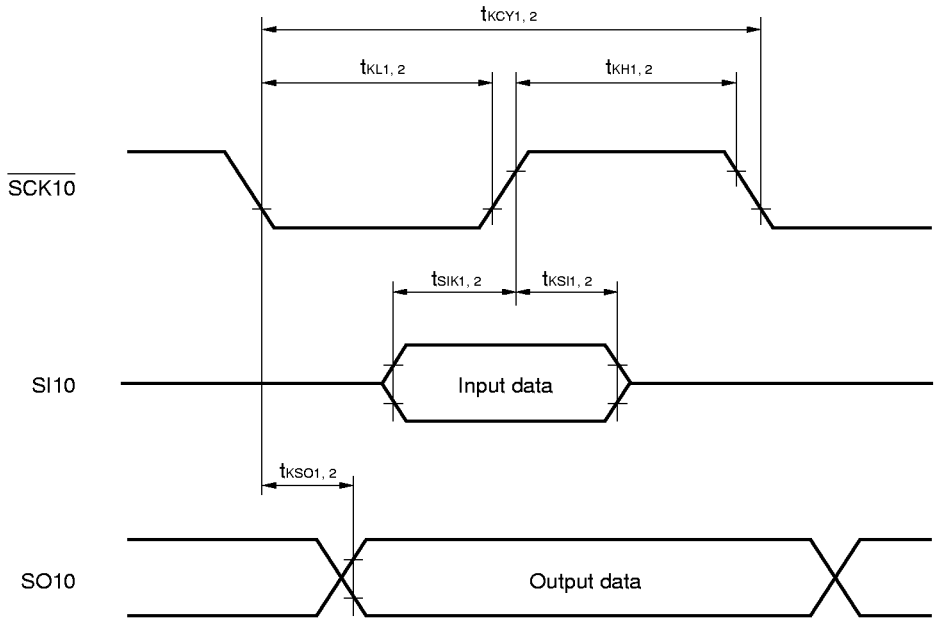


$\overline{\text{RESET}}$ INPUT TIMING



SERIAL TRANSFER TIMING

Three-Wire Serial I/O Mode:



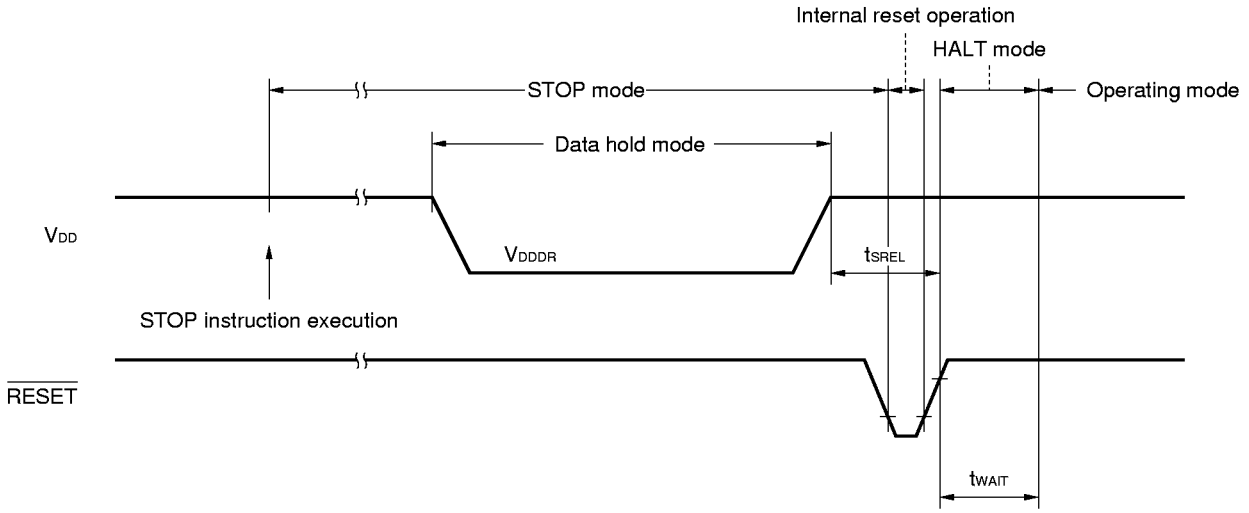
DATA HOLD CHARACTERISTICS OF DATA MEMORY AT LOW VOLTAGE IN STOP MODE
(T_A = -40 to +85 °C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{DDR}		4.0		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation settling time	t_{WAIT}	Reset by $\overline{RESET}$		5.46		ms
		Reset by interrupt		**Note**		ms

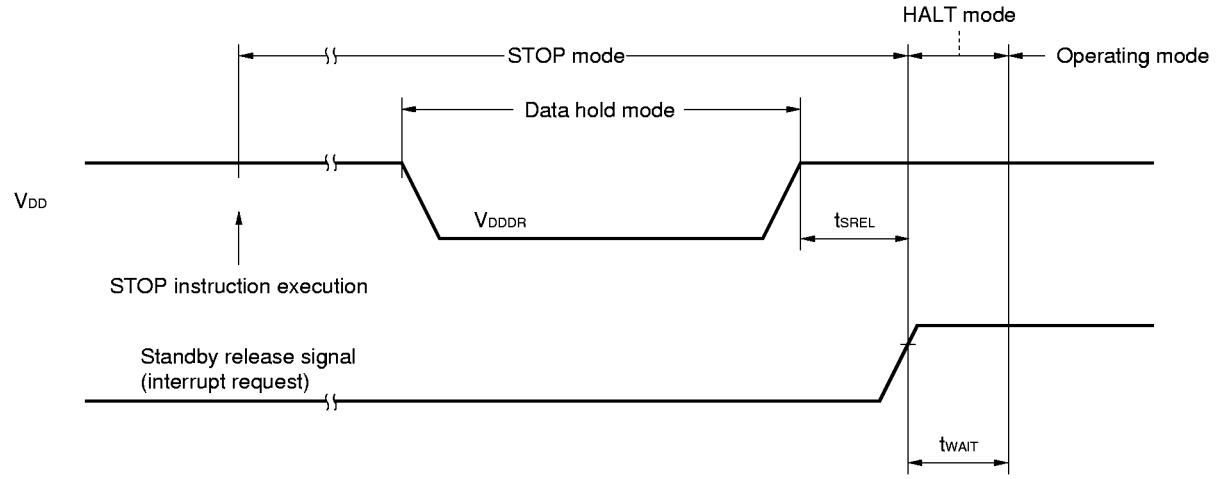
Note 2^{12}/fx, 2^{15}/fx, or 2^{17}/fx can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register (OSTS).

Remark fx: Main system clock oscillation frequency

DATA HOLD TIMING (STOP mode release by $\overline{RESET}$)



DATA HOLD TIMING (standby release signal: STOP mode release by interrupt signal)



FLASH MEMORY PROGRAMMING CHARACTERISTICS

Basic Characteristics (T_A = 0 to +50 °C, V_{DD} = 4.0 to 5.5 V)

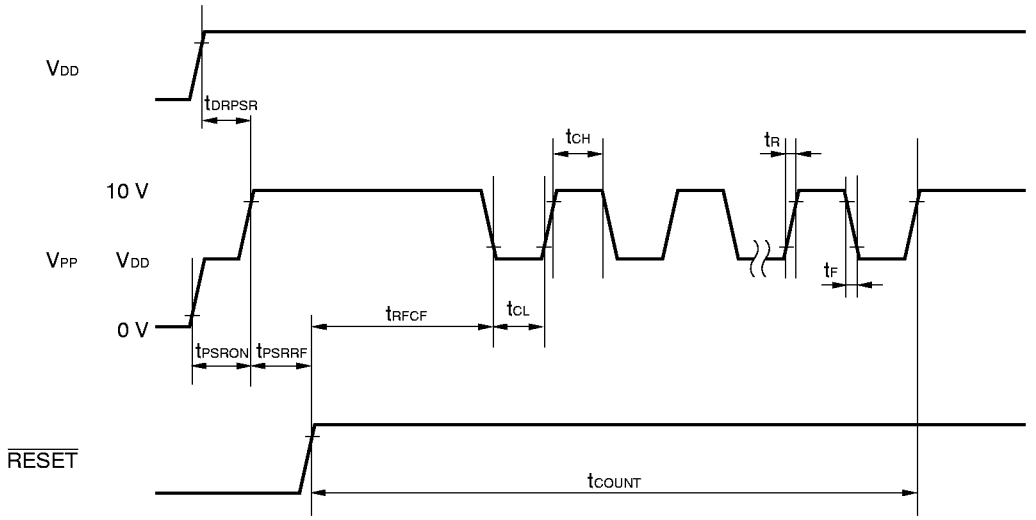
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.0		5.5	V
	V_{PPL}	When GND level is detected	0		$0.2V_{DD}$	V
	V_{PPH}	When V_{DD} level is detected	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PP}	When high voltage is detected	9.7	10.0	10.3	V
Write time	T_{PW}	1 byte	40	50	To be determined	μs
Erase time	T_{EW}		2			s
Number of times flash memory can be rewritten					20	times
Main clock frequency	f_X			6		MHz

AC CHARACTERISTICS (T_A = 0 to +50 °C, V_{DD} = 4.0 to 5.5 V)

Flash memory write mode

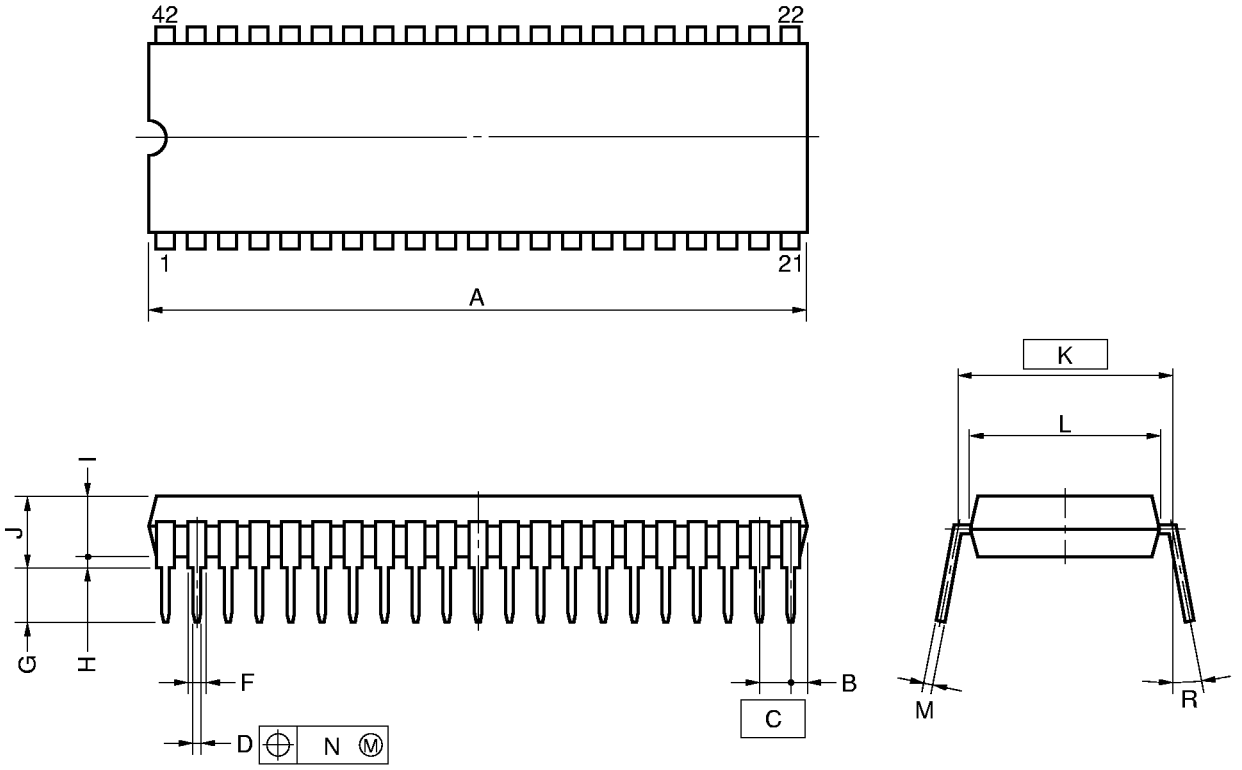
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} setup time	t_{PSRON}		0		5.5	μs
Setup time between V_{DD}↑ and V_{PP}↑	t_{DRPSR}		0			μs
Setup time between $\overline{\text{RESET}}$ ↑ and V_{PP}↑	t_{PSRRF}		1			μs
Delay between $\overline{\text{RESET}}$ ↑ and V_{PP} count start	t_{RFCF}		1			μs
Count execution time	t_{COUNT}				1	ms
V_{PP} pulse high/low level width	t_{CH}, t_{CL}		8			μs
V_{PP} pulse rise/fall time	t_R, t_F				To be determined	μs

FLASH MEMORY WRITE MODE



7. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

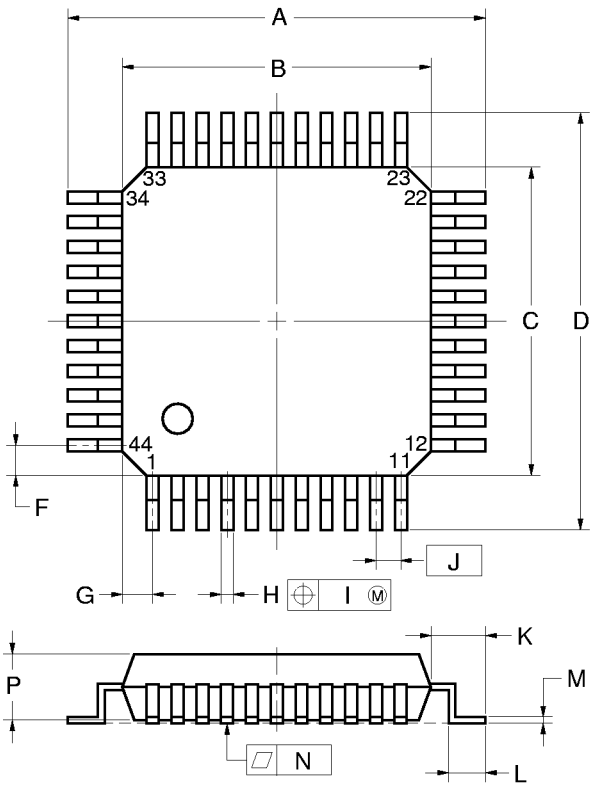
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

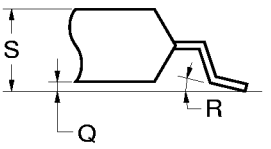
ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

44 PIN PLASTIC QFP (□10)



detail of lead end



NOTE

Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78F9801.

LANGUAGE PROCESSING SOFTWARE

RA78K0S[Notes 1, 2, 3]	Assembler package common to the 78K/0S series
CC78K0S[Notes 1, 2, 3]	C compiler package common to the 78K/0S series
DF789800[Notes 1, 2, 3, 7]	Device file for the μPD789800 sub-series
CC78K0S-L[Notes 1, 2, 3, 7]	C compiler library source file common to the 78K/0S series

FLASH MEMORY WRITE TOOLS

Flashpro II[Note 4]	Dedicated flash writer (formerly, Flashpro)
FA-42CU[Note 4]	Flash memory write adapter
FA-44GB[Note 4]	

DEBUGGING TOOLS

ND-K980[Notes 4, 7]	In-circuit emulator for the μPD789800 sub-series The ND-K980 incorporates the NS-78K9 screen debugger.
IF-98D[Note 4]	This is an interface board, required when a PC-9800 series (other than a notebook type) are used as the host machine for the ND-K980.
IF-PCD[Note 4]	This is an interface board, required when an IBM PC/AT or compatible (other than a notebook type) is used as the host machine for the ND-K980.
IF-CARD[Note 4]	This is an interface board, required when a PC-9800 notebook, IBM PC/AT notebook, or compatible is used as the host machine for the ND-K980.
NP-42CU[Note 4]	Emulator probe for the 42-pin plastic shrink DIP (CU type)
NP-44GB[Note 4]	Emulator probe for the 44-pin plastic QFP (GB-3BS type)
NJ-535[Note 4]	100/120 VAC adapter
NJ-550W[Note 4]	100 to 240 VAC adapter
SM78K0S[Notes 5, 6]	System emulator common to all 78K/0S series units
DF789800[Notes 5, 6, 7]	Device file for the μPD789800 sub-series

REAL-TIME OS

MX78K0S[Notes 1, 2, 7]	OS for the 78K/0S series

Notes 1. Based on the PC-9800 series (MS-DOS™)

2. Based on the IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and NEWS™ (NEWS-OS™)

4. Product manufactured by and available from Naito Densei Machida Seisakusho Co., Ltd. (044-822-3813).

5. Based on the PC-9800 series (MS-DOS + Windows™)

6. Based on the IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows)

7. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789800.

APPENDIX B RELATED DOCUMENTS

DOCUMENTS RELATED TO DEVICES

Document name	Document No.	
	Japanese	English
μPD789800 Preliminary Product Information	U12627J	To be prepared
μPD78F9801 Preliminary Product Information	U12626J	This manual
μPD789800 Sub-Series User's Manual	To be prepared	To be prepared
78K/0 Series User's Manual - Instruction	U11047J	U11047E
78K/0S Series Instruction Summary Sheet	To be prepared	-
78K/0S Series Instruction Set	To be prepared	-
μPD789800 Sub-Series Special Function Registers	To be prepared	-

DOCUMENTS RELATED TO DEVELOPMENT TOOLS (USER'S MANUAL)

Document name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K/0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows Base	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E

DOCUMENTS RELATED TO SOFTWARE TO BE INCORPORATED INTO THE PRODUCT (USER'S MANUAL)

Document name	Document No.	
	Japanese	English
OS for 78K/0S Series MX78K0S	To be prepared	To be prepared

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

OTHER DOCUMENTS

Document name	Document No.	
	Japanese	English
IC PACKAGE MANUAL	C10943X	
SMD Surface Mount Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	-
Guide to Quality Assurance for Semiconductor Device	C11893J	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	U11416J	-

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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SPARCstation is a trademark of SPARC International, Inc.

SunOS is a trademark of Sun Microsystems, Inc.

NEWS and NEWS-OS are trademarks of SONY Corporation.

Regional Information

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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