P54/74PCT827A/B
P54/74PCT828A/B
BUFFERS

PRELIMINARY

T-52-07

FEATURES

- Equivalent to Am29827-28 Bipolar Buffers
- Full CMOS Implementation
- Low Power Operation
- High Speed Buffers
- Fully TTL Compatible Input and Output Levels
- I_{OL} = 48mA (Commercial) and 32mA (Military)
- Clamp Diodes on all Inputs for Ringing Suppression
- Produced with PACE Technology™
- Compact Pinout
  –24-Pin 300 mil DIP, SOIC
  –28-Pad 450 mil sq. LCC

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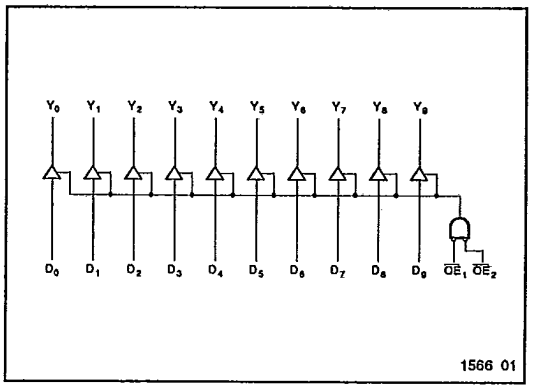
DESCRIPTION

The P54/74PCT827A/B and P54/74PCT828A/B 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200mV minimum input hystersis to provide improved noise rejection. The P54/74PCT827A/B and P54/74PCT828A/B family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The P54/74PCT827A/B and P54/74PCT828A/B is manufacturered using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V

LOGIC BLOCK DIAGRAM



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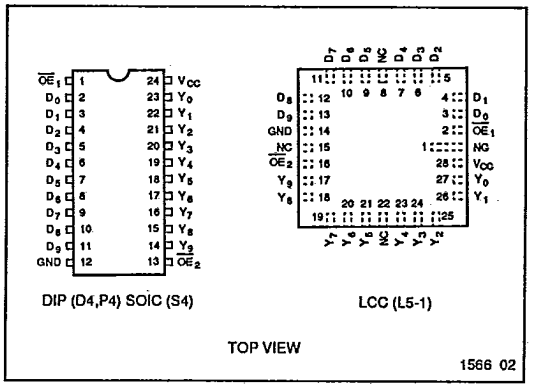
PIN CONFIGURATIONS



DIP (D4,P4) SOIC (S4) LCC (L5-1)

TOP VIEW

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−65 to +150	°C
T_A	Ambient Temperature Under Bias	−55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	−0.5 to +7.0	V
I_{IN}	Input Current	−30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	−0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	−55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		−0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				−1.2	V	MIN	I_{IN} = −18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} − 0.2V	V_{CC} − 0.2			V		I_{OH} = −32µA
		Military/Commercial (CMOS)	V_{CC} − 0.2			V	MIN	I_{OH} = −300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = −15mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = −24mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} − 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				−5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				−5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied				−10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied[3]				−10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		−60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l Mil	.003 .003	0.3 0.5	mA mA	V_{CC} = MAX, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open, $T/\overline{R}$ = V_{CC} or GND
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
			6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLES

P54/74PCT827A/B (Non-Inverting)

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

Note: 1566 Tbl 07

H = High, L = Low, X = Don't Care, Z = High Impedance

P54/74PCT828A/B (Inverting)

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

Note: 1566 Tbl 08

H = High, L = Low, X = Don't Care, Z = High Impedance

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AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	P54/74PCT827A/828A				P547PCT827B/828B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'PCT827A/B	C_L = 50pF R_L = 500Ω	– –	10.0 10.0	– –	8.0 8.0	– –	6.5 6.5	– –	5.0 5.0	ns ns	1 3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'PCT827A/B	C_L = 300pF[2] R_L = 500Ω	– –	17.0 17.0	– –	15.0 15.0	– –	14.0 14.0	– –	13.0 13.0	ns ns	1 3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'PCT828A/B	C_L = 50pF R_L = 500Ω	– –	9.5 9.5	– –	7.5 7.5	– –	6.5 6.5	– –	5.5 5.5	ns ns	1 2
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'PCT828A/B	C_L = 300pF[2] R_L = 500Ω	– –	16.0 16.0	– –	14.0 14.0	– –	14.0 14.0	– –	13.0 13.0	ns ns	1 2
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	– –	17.0 17.0	– –	15.0 15.0	– –	9.0 9.0	– –	8.0 8.0	ns ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 300pF[2] R_L = 500Ω	– –	25.0 25.0	– –	23.0 23.0	– –	16.0 16.0	– –	15.0 15.0	ns ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 5pF[2] R_L = 500Ω	– –	10.0 10.0	– –	9.0 9.0	– –	7.0 7.0	– –	6.0 6.0	ns ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	– –	19.0 19.0	– –	17.0 17.0	– –	8.0 8.0	– –	7.0 7.0	ns ns	1, 7, 8

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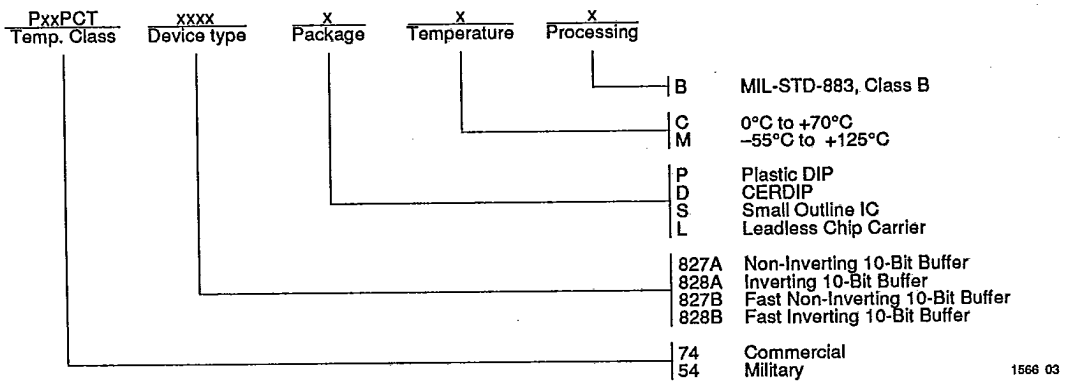
Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

ORDERING INFORMATION



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