P54/74PCT157A/B—P54/74PCT158A/B DATA SELECTOR/MULTIPLEXER

PRELIMINARY

T-67-21-51

FEATURES

- Quad 2-Input Data Selector/ Multiplexer
- Full CMOS Implementation
- Low Power Operation
- I_{OL} = 48 mA (commercial) and 32mA (military)
- Three-State Outputs
- Fully TTL Compatible Input and Output Levels
- Produced with PACE Technology™
- Compact Pinout
  – 16 Pin 300 mil DIP, SOIC

DESCRIPTION

The P54/74PCT157A/B and P54/74PCT158A/B are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data Select input (S). The Enable input ($\overline{E}$) is active-low. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 'PCT157A/B and 'PCT158A/B. The state of the Select input determines the particular register from which the data comes, It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

These devices are the logic implementation of a 4-pole, 2-positon switch where the position of the switch is determined by the logic levels supplied to the Select input. The outputs of the 'PCT157 are Non-inverting whereas the 'PCT158 has inverting outputs.

The P54/74PCT157/158 is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

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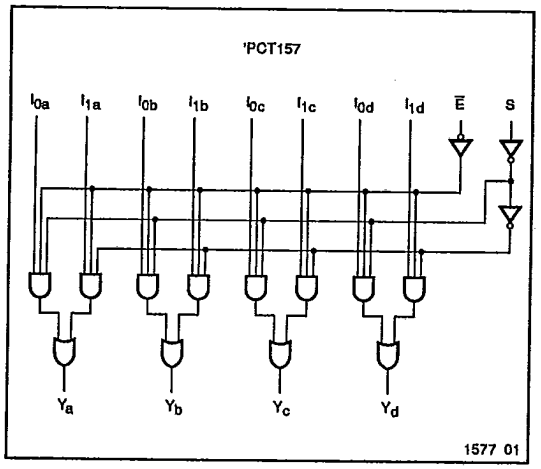
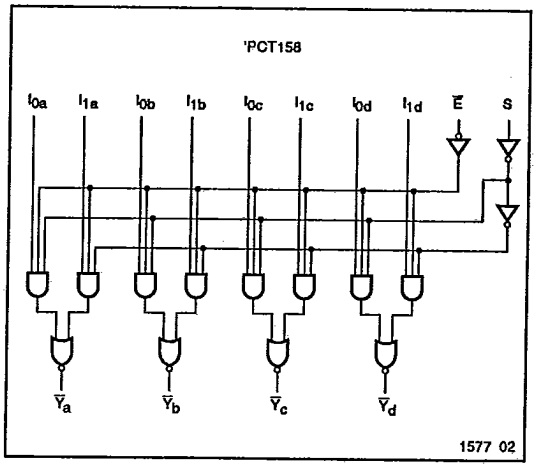
FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



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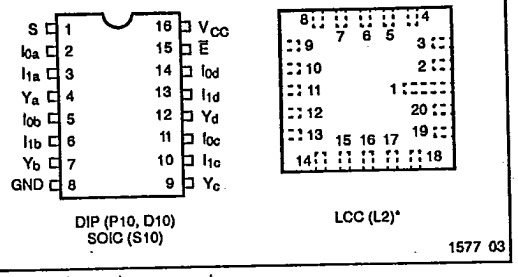
PIN CONFIGURATIONS

'PCT157 A/B



DIP (P10, D10)
SOIC (S10)

LCC (L2)*

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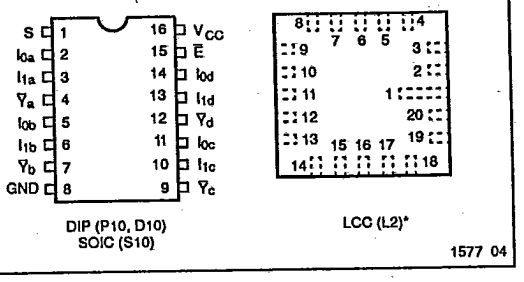
* Future – Pinout to be announced.

PIN CONFIGURATIONS

'PCT158 A/B



DIP (P10, D10)
SOIC (S10)

LCC (L2)*

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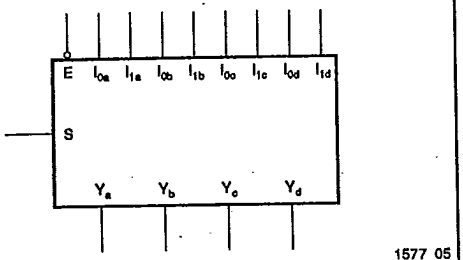
LOGIC SYMBOL

'PCT157 A/B



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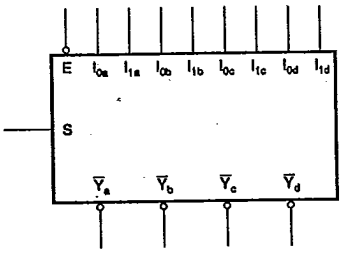
LOGIC SYMBOL

'PCT158 A/B



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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

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RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l / Mil	.003 / .003	0.3 / 0.5	mA / mA	V_{CC} = MAX, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 5MHz, $\overline{E}$ = GND, S = GND, and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			6.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 5MHz, $\overline{E}$ = GND, S = GND and V_{IN} = 3.4V or V_{IN} = GND
			7.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, 4 Inputs Toggling at f_1 = 5MHz, $\overline{E}$ = GND, S = GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			16.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, 4 Inputs Toggling at f_1 = 5MHz, $\overline{E}$ = GND, S = GND and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE, 'PCT157A/B

Enable	Select Input	Data Inputs		Output
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

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H = HIGH Voltage Level
h = HIGH Voltage Level
X = Don't care

FUNCTION TABLE, 'PCT158A/B

Enable	Select Input	Data Inputs		Output
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

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PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
$\overline{E}$	Enable Input (Active LOW)
$I_{0A} - I_{0D}$	Data Input from Source 0
$I_{1A} - I_{1D}$	Data Inputs from Source 1
$Y_A - Y_D$	Non – Inverted Output
$Y_A - Y_D$	Inverted Output

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AC CHARACTERISTICS

Symbol	Parameter	P54/74PCT157A/158A					P54/74PCT157B/158B					Units	Fig. No.
		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L			
		Typ.	Min.	Max.	Min.	Max.	Typ.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation delay I_n to Y 'PCT157	4.5 3.5			3.0 1.5	7.0 6.0						ns ns	1 3
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y 'PCT157	7.5 5.0			5.5 4.0	10.5 7.0						ns ns	1 5
t_{PLH} t_{PHL}	Propagation delay S to Y 'PCT157	7.5 6.0			5.4 4.0	11.0 8.5						ns ns	1 3
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$ 'PCT158	4.0 2.5			2.5 1.0	7.0 4.5						ns ns	1 2
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$ 'PCT158	5.5 6.0			4.0 5.0	7.5 8.0						ns ns	1 5
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$ 'PCT158	6.5 5.5			4.0 3.5	9.5 8.0						ns ns	1 2

Note: Minimum limits are guaranteed but not tested on Propagation Delays.

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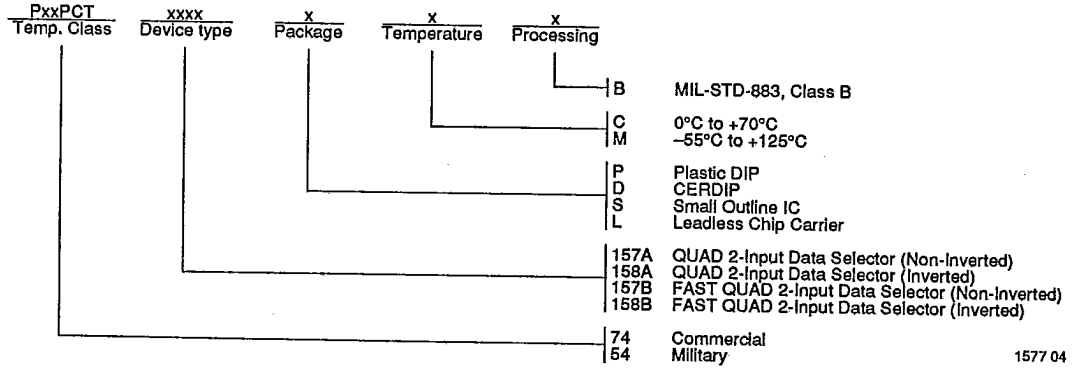
ORDERING INFORMATION



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