MAS9090B

LOW VOLTAGE 14-BIT LINEAR CODEC

- **14-bit linear analog to digital and digital to analog converters**
- **8-bit A-law or μ-law companded analog to digital and digital to analog converters**

DESCRIPTION

The MAS9090 is a high performance low power PCM CODEC and filter device tailored to implement the audio front-end functions required by the low voltage/low power consumption digital terminals.

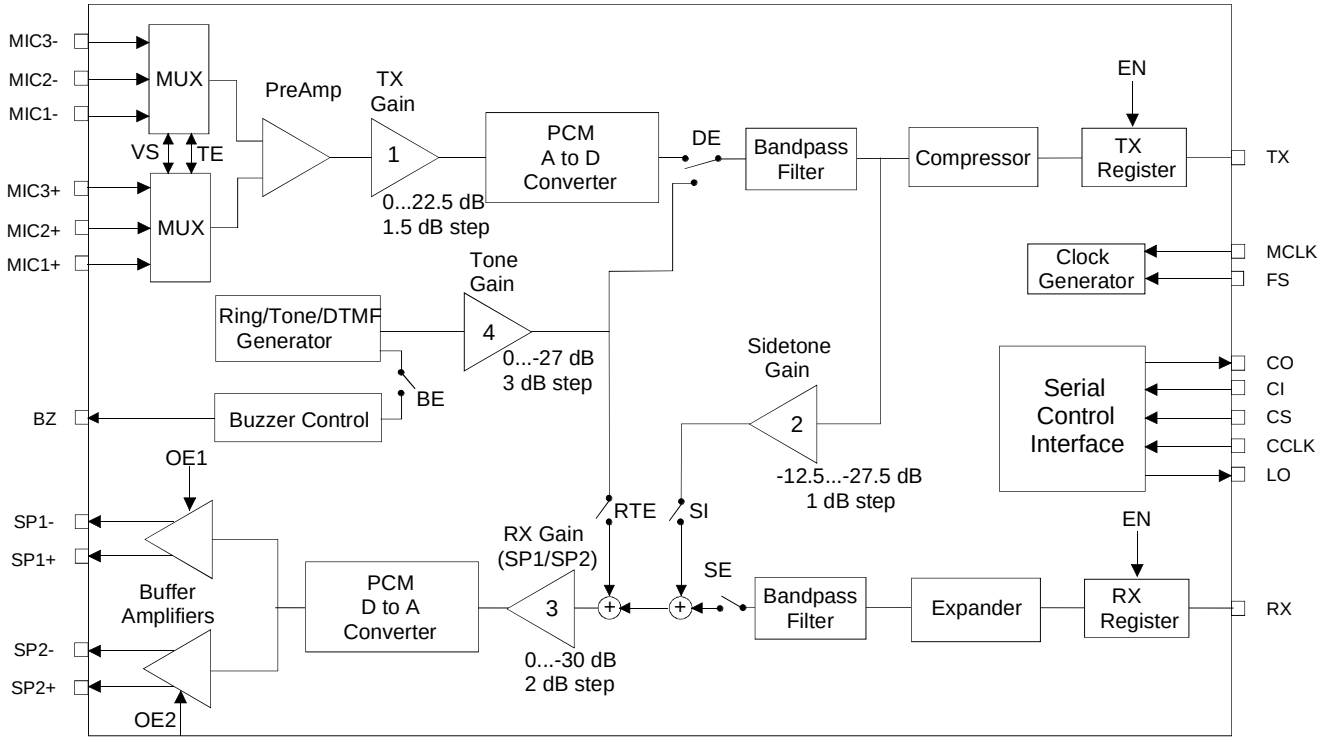
FEATURES

- Single 2.7-3.6 V or 4.5-5.5 V supply selectable
- -30°C to 85°C temperature operation range
- 11 mW operating power (typ. at 2.7V)
- 15 mW operating power (typ. at 3.0V)
- 27 mW operating power (typ. at 3.6V)
- 38 mW operating power (typ. at 5.0V)
- Digital bandpass filters
- ±0.5 dB absolute gain accuracy (untrimmed)
- 28-pin SO and 44-pin TQFP packages
- Pin compatible with ST5090 and ST5092

APPLICATIONS

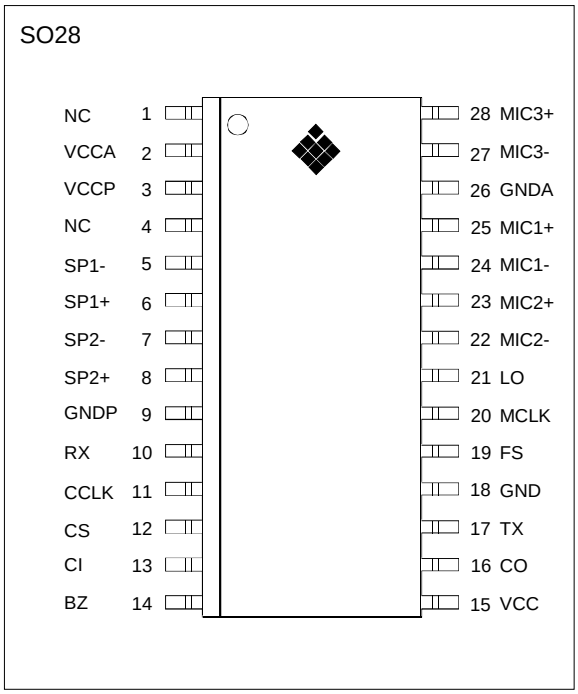
- GSM digital cellular telephones
- Battery operated audio front-ends for DSPs
- ISDN Terminals
- CT2 and DECT digital cordless telephones

BLOCK DIAGRAM

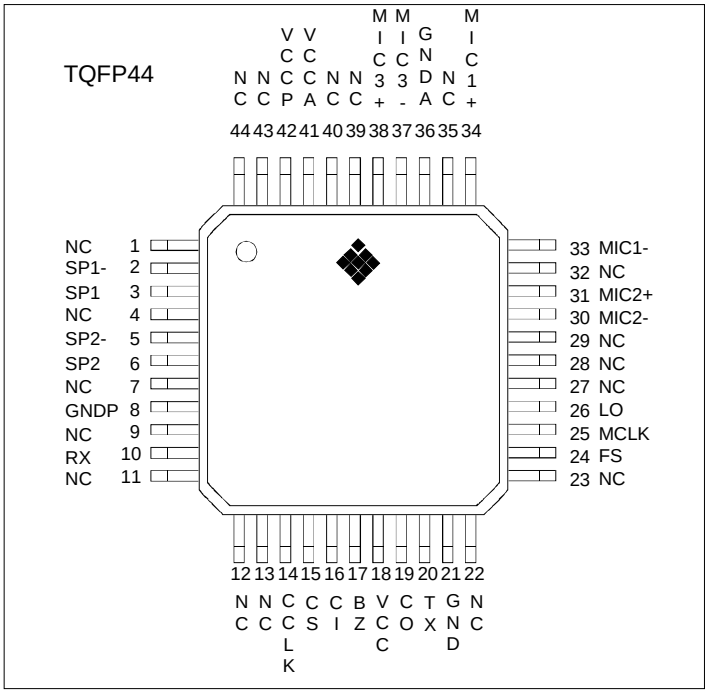


PIN CONFIGURATION

SO28



TQFP44



PIN DESCRIPTION

Pin Name	Pin Number		Type	Function
	SO28	TQFP44		
	1,4	1,4,7,9 11,12,13 22,23,27 28,29,32 35,39,40, 43,44		No connection.
VCCA	2	41	P	Positive power supply input for analog section.
VCCP	3	42	P	Positive power supply input for speaker amplifiers.
SP1-	5	2	AO	Speaker 1 amplifier negative output.
SP1+	6	3	AO	Speaker 1 amplifier positive output.
SP2-	7	5	AO	Speaker 2 amplifier negative output.
SP2+	8	6	AO	Speaker 2 amplifier positive output.
GNDP	9	8	G	Speaker amplifier.
RX	10	10	DI	Receive data input.
CCLK	11	14	DI	Control clock input. Shifts serially into CI and CO when CS is low. CCLK is asynchronous with other system clocks.
CS	12	15	DI	Chip select input.
CI	13	16	DI	Control data input.
BZ	14	17	AO	Buzzer driver output.
VCC	15	18	P	Positive power supply input for the digital section. VCCA, VCCP AND VCC must be connected together.
CO	16	19	DO	Control data output.
TX	17	20	DO	Transmit data output. Data is shifted out on this during the assigned transmit slots. Otherwise, TX is on high impedance state.
GND	18	21	G	Ground for the digital section.
FS	19	24	DI	Frame sync input. This 8kHz signal defines the start of the TX and RX frames.

PIN DESCRIPTION

Pin Name	Pin Number		Type	Function
MCLK	20	25	DI	Master clock input. Must be 512, 1536, 2048 or 2560 kHz
LO	21	26	DO	Value of bit DO of CR1.
MIC2-	22	30	AI	Negative differential input for MIC2.
MIC2+	23	31	AI	Positive differential input for MIC2.
MIC1-	24	33	AI	Negative differential input for MIC1.
MIC1+	25	34	AI	Positive differential input for MIC1.
GNDA	26	36	G	GNDA analog ground.
MIC3-	27	37	AI	Negative differential input for MIC3.
MIC3+	28	38	AI	Positive differential input for MIC3.

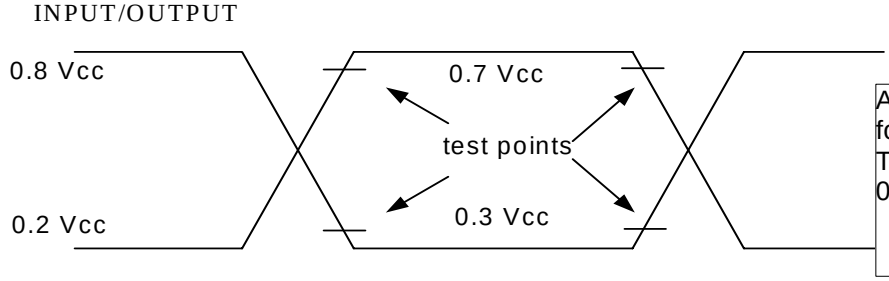
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{CC}			7.0	V
Voltage at MIC		V_{CC} < 5.5V	-1	V_{CC}+1	V
Current at any digital output				50	mA
Voltage at any digital input		V_{CC} < 5.5V	-1	V_{CC}+1	V
Storage Temperature	T_S		-55	+125	°C

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0V mode (SV=0)	2.7	3.0	3.6	V
		5.0V mode (SV=1)	4.5	5.0	5.5	v
Operating Temperature	T_A		-30		+85	°C

AC, TESTING INPUT, OUTPUT WAVEFORM



AC testing: inputs are driven at 0.8Vcc for a logic '1' and 0.2Vcc for a logic '0'. Timing measurements are made at 0.7Vcc for a '1' and 0.3 Vcc for a '0'.

ELECTRICAL CHARACTERISTICS

◆ Digital Inputs/Outputs

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage	VIL	All digital inputs DC All digital inputs AC			$0.3V_{CC}$ $0.2V_{CC}$	V
Input high voltage	VIH	All digital inputs DC All digital inputs AC	$0.7V_{CC}$ $0.8V_{CC}$			V
Output low voltage	VOL	All digital outputs, IL = 10µA All digital outputs, IL = 2mA			0.1 0.4	V
Output high voltage	VOH	All digital outputs, IL = 10µA All digital outputs, IL = 2mA	V_{CC}-0.1 V_{CC}-0.4			V
Input low current	IIL	Any digital input, GND < V_{IN} < V_{IL}	-10		10	µA
Input high current	IIH	Any digital input, V_{IH} < V_{IN} < V_{CC}	-10		10	µA
Output current in high impedance	IOZ	TX and CO	-10		10	µA

◆ Analog Inputs/Outputs

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input leakage	I_{MIC}	GND < V_{MIC} < V_{CC} (active mic)	-100	±20	+100	µA
Input resistance	R_{MIC}	GND < V_{MIC} < V_{CC}	50			kΩ
Load resistance	R_{LSP1}	SP1+ to SP1-	30			Ω
Load capacitance	C_{LSP1}	SP1+ to SP1-		50		nF
Output resistance	R_{OSP1}	Steady zero PCM code applied to RX, I = 1mA		1.0		Ω
Differential offset voltage from SP1+ to SP1-	V_{OSP1}	Alternating zero PCM code applied to RX, R_L = 30 ohms	-100	0	+100	mV
Load resistance	R_{LSP2}	SP2+ to SP2-	30			Ω
Load capacitance	C_{LSP2}	SP2+ to SP2-		50		nF
Input resistance	R_{MIC}	GND < V_{MIC} < V_{CC}	50			kΩ
Output resistance	R_{OSP2}	Steady zero PCM code applied to RX, I = 1mA		1.0		Ω
Differential offset voltage from SP2+ to SP2-	V_{OSP2}	Alternating zero PCM code applied to RX, R_L = 30 ohms	-100	0	+100	mV

◆ Power Dissipation

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power down current at 3.0V	I_{CC0}	CCLK, CI = 0.1V CS = VCC - 0.1V		0.08	10	µA
Power down current at 5V	I_{CC0}	CCLK, CI = 0.1V CS = VCC - 0.1V		0.08	10	µA
Power up current at 2.7V	I_{CC1}	SP1 and SP2 not loaded		4	6	mA
Power up current at 3.0V	I_{CC1}	SP1 and SP2 not loaded		5	8	mA
Power up current at 3.6V	I_{CC1}	SP1 and SP2 not loaded		7.5	12	mA
Power up current at 5V	I_{CC1}	SP1 and SP2 not loaded		7.5	20	mA
SP1 short circuit current	I_{SHORT}			130		mA

TIMING SPECIFICATIONS

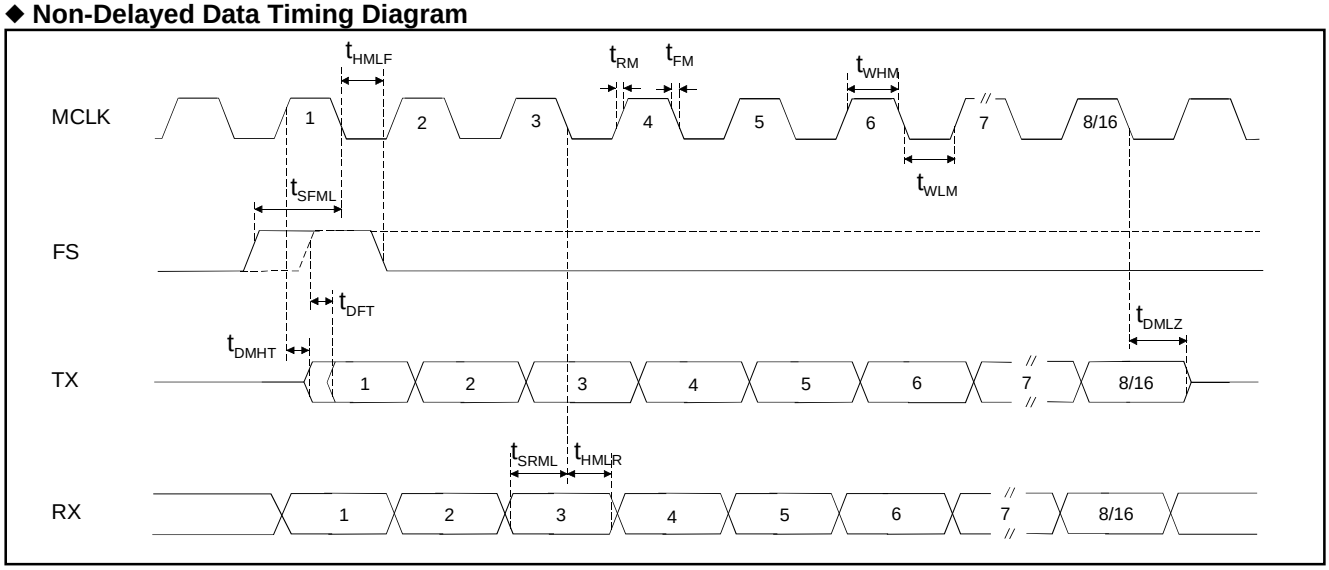
◆ Master Clock Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency of MCLK	f_{MCLK}	programmable		512 1536 2048		kHz
Period of MCLK high/low f_{MCK} = 512	t_{WHM} t_{WLM}	Measured from V_{IH} to V_{IH}	878		1074	ns
Period of MCLK high f_{MCK} = 1536, 2048	t_{WHM}	Measured from V_{IH} to V_{IH}	80			ns
Period of MCLK low f_{MCK} = 1536, 2048	t_{WLM}	Measured from V_{IL} to V_{IL}	80			ns
Rise time of MCLK	t_{RM}	Measured from V_{IL} to V_{IH}			30	ns
Fall time of MCLK	t_{FM}	Measured from V_{IH} to V_{IL}			30	ns

◆ PCM Interface Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hold time, MCLK low to FS low	t_{HMLF}		17			ns
Setup time, FS high to MCLK low	t_{SFML}		30			ns
Delay time, MCLK high to valid TX data	t_{DMHT}	Load = 100pF			100	ns
Delay time, MCLK low to TX disabled	t_{DMLZ}		10		100	ns
Delay time, FS high to valid TX data	t_{DFT}	Load = 100pF non-delayed mode only			100	ns
Setup time, RX data valid to MCLK low	t_{SRML}		20			ns
Hold time, MCLK low to invalid RX data	t_{HMLR}		10			ns
Hold time, MCLK high to FS low	t_{HMHF}		30			ns
Setup time, FS high to MCLK high	t_{SFMH}		30			ns
Delay time, MCLK low to valid TX data	t_{DMLT}	Load = 100pF			100	ns
Delay time, MCLK high to TX disabled	t_{DMHZ}		10		100	ns
Hold time, MCLK high to invalid RX data	t_{HMHR}		20			ns

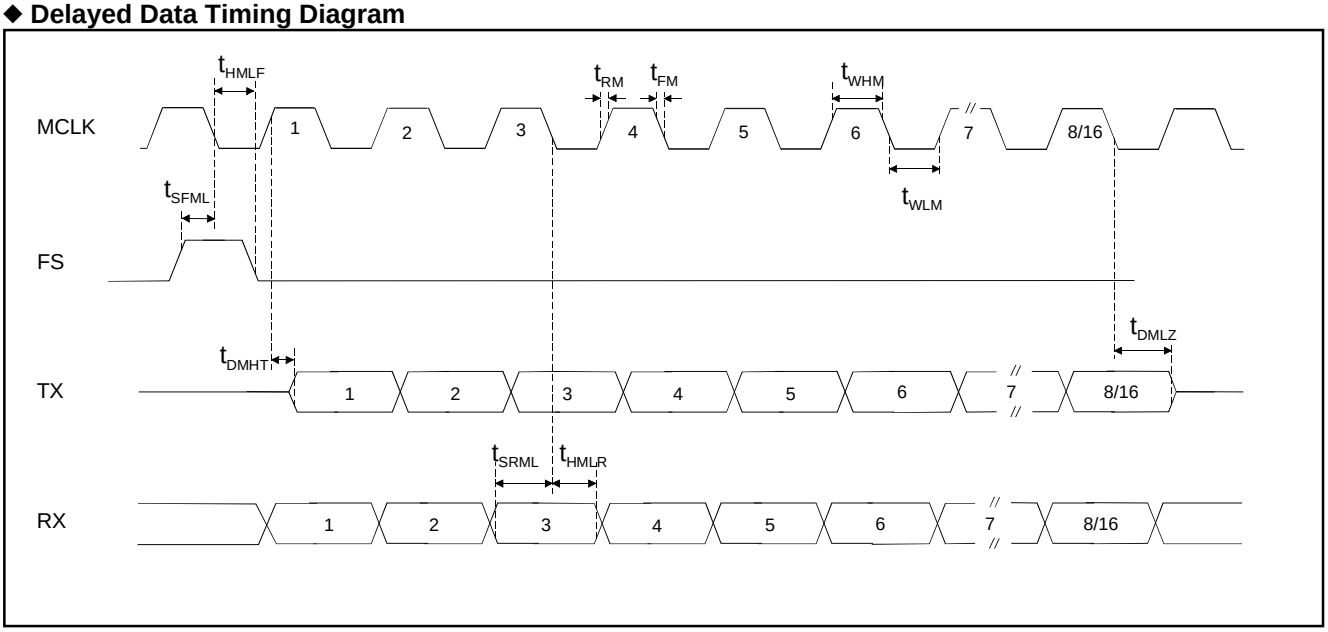
◆ Non-Delayed Data Timing Diagram



In companded mode the timing is applied to 8 bits instead of 16 bits.

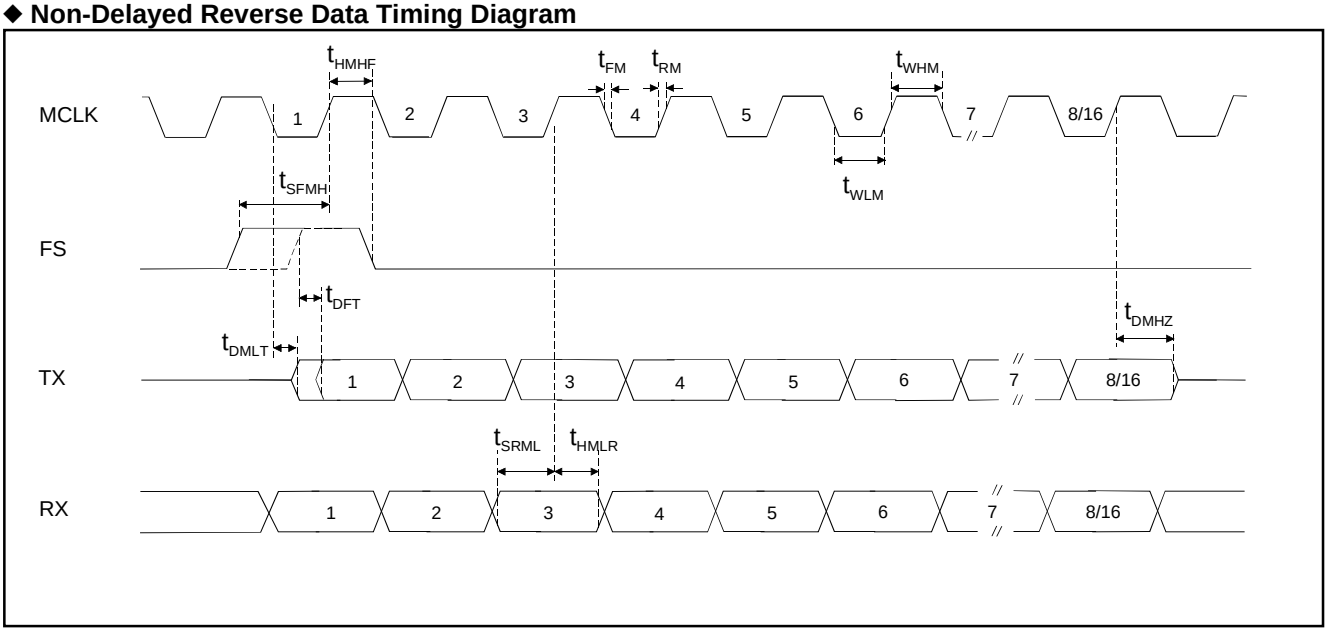
TIMING SPECIFICATIONS

◆ Delayed Data Timing Diagram



In companded mode the timing is applied to 8 bits instead of 16 bits.

◆ Non-Delayed Reverse Data Timing Diagram



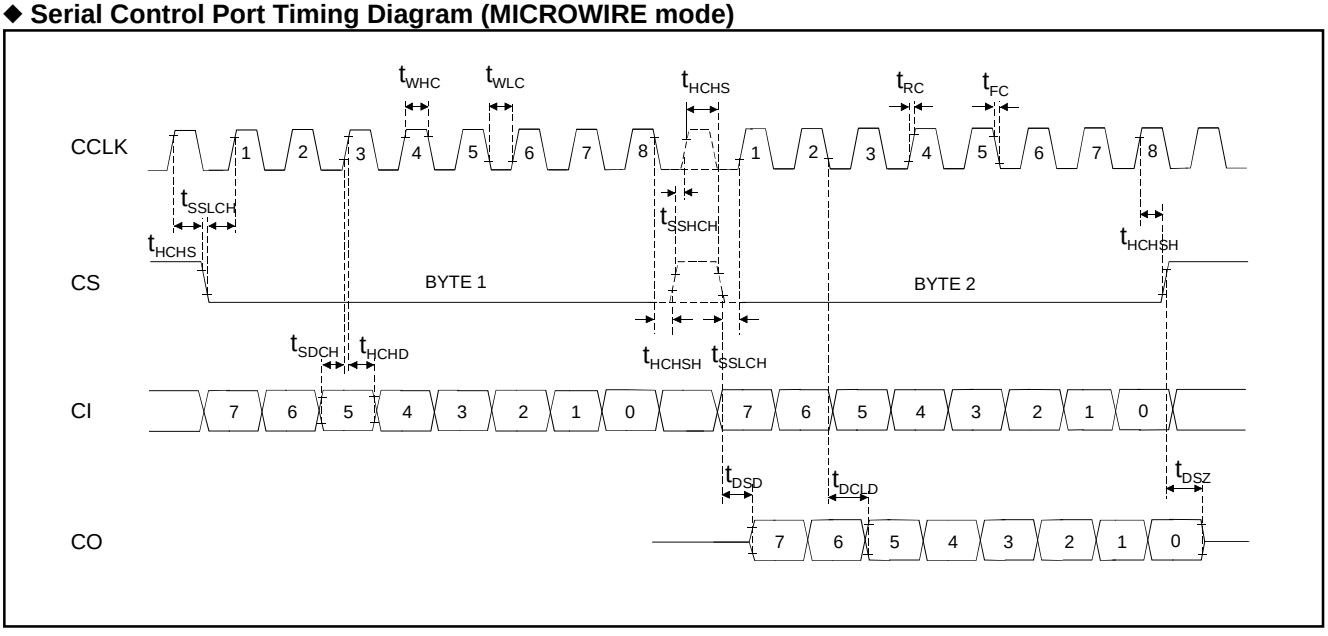
In companded mode the timing is applied to 8 bits instead of 16 bits.

TIMING SPECIFICATIONS

◆ Serial Control Port Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency of CCLK	f_{CCLK}				2.048	MHz
Period of CCLK high	t_{WHC}	Measured from V_{IH} to V_{IH}	160			ns
Period of CCLK low	t_{WLC}	Measured from V_{IL} to V_{IL}	160			ns
Rise time of CCLK	t_{RC}	Measured from V_{IL} to V_{IH}			50	ns
Fall time of CCLK	t_{FC}	Measured from V_{IH} to V_{IL}			50	ns
Hold time, CCLK high to CS low	t_{HCHS}		10			ns
Setup time, CS low to CCLK high	t_{SSLCH}		50			ns
Setup time, valid CI data to CCLK high	t_{SDCH}		50			ns
Hold time, CCLK high to invalid CI data	t_{HCHD}		50			ns
Delay time, CCLK low to valid CO data	t_{DCLD}	Load = 100 pF			80	ns
Delay time, CS low to valid CO data	t_{DSD}				50	ns
Delay time, CS high or 8th CCLK low to CO high impedance	t_{DSZ}		10		80	ns
Hold time, 8th CCLK high to CS high	t_{H8CHS}		100			ns
Setup time, CS high to CCLK high	t_{SSHCH}		100			ns

◆ Serial Control Port Timing Diagram (MICROWIRE mode)



TRANSMISSION CHARACTERISTICS

◆ Absolute levels at MIC1/MIC2/MIC3

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Unit
0 dBm0 level	Transmit amps connected for 20 dB gain		49.26		mV_{RMS}
Overload level			70.71		mV_{RMS}
0 dBm0 level	Transmit amps connected for 42.5 dB gain		3.694		mV_{RMS}
Overload level			5.302		mV_{RMS}

◆ Absolute levels at SP1 / SP2 (differentially measured)

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Unit
0 dBm0 level	Receive gains = 0 dB		1.965		V_{RMS}
0 dBm0 level	Receive gains = -30 dB		61.85		mV_{RMS}

◆ Transmit path amplitude response

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transmit gain absolute accuracy, HPT = 0 HPT = 1	G_{XA}	TX gain set to maximum, measure deviation of digital PCM code from ideal 0 dBm0 PCM code at TX	-0.5 -0.4	0 0.1	0.5 0.6	dB
Transmit gain variation with programmed gain	G_{XAG}	Measure TX gain over the range (from max to min). Calculate the deviation from the programmed gain relative to G_{XA}, i.e. $G_{XAG} = G_{actual} - G_{prog} - G_{XA}$	-0.5		0.5	dB
Transmit gain variation with temperature	G_{XAT}	Measured relative to G_{XA} min. gain < G_X < max. gain	-0.1		0.1	dB
Transmit gain variation with supply	G_{XAV}	Measured relative to G_{XA} G_X = maximum gain	-0.1		0.1	dB
Transmit gain variation with frequency	G_{XAF}	Relative to 1.015625 kHz, multitone test technique used min. gain < G_X < max. gain				
HPT=0		f = 60 Hz		-34	-33	dB
		f = 100 Hz		-36	-35	
		f = 200 Hz		-11	-10	
		f = 300 Hz	-1.5	-0.7	0.5	
		f = 400 Hz to 3000 Hz	-0.5		0.5	
		f = 3400 Hz	-1.5	-1.3	0.0	
		f = 4000 Hz		-17	-16	
		f = 4600 Hz		-62	-61	
		f = 8000 Hz		-68	-67	
HPT=1		f = 60 Hz to 3000 Hz f = 3000 to 8000 Hz, see HPT=0	-0.5		0.5	dB
Transmit gain variation with signal level	G_{XAL}	Sinusoidal test method reference level = -10 dBm0				
		V_{MIC} = -40 dBm0 to +3.0 dBm0 V_{MIC} = -50 dBm0 to -40 dBm0 V_{MIC} = -55 dBm0 to -50 dBm0	-0.5 -0.5 -1.2		0.5 0.5 1.2	dB
Tone Generator gain absolute accuracy	G_{XTONE}	Measure deviation of digital PCM code from ideal 0dBm0 PCM code at TX	-0.3		0.6	dB

TRANSMISSION CHARACTERISTICS

◆ Receive path amplitude response

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Receive gain absolute accuracy, HPX = 0 HPX = 1	G_{RA1}	RX gain programmed to maximum, apply -6dBm0 PCM code to RX, measure SP1+ to SP1-	-0.5 -0.4	0 0.1	0.5 0.6	dB
Receive gain absolute accuracy, HPX = 0 HPX = 0	G_{RA2}	RX gain programmed to maximum, apply -6dBm0 PCM code to RX, measure SP2+ to SP2-	-0.5 -0.4	0 0.1	0.5 0.6	dB
Receive gain variation with programmed gain	G_{RAG1}	Measure SP1 gain over the range from maximum to minimum setting, calculate the deviation from the programmed gain relative to G_{RA1}, i.e. $G_{RAG1} = G_{actual}-G_{prog}-G_{RA1}$	-0.5		0.5	dB
Receive gain variation with programmed gain	G_{RAG2}	Measure SP2 gain over the range from maximum to minimum setting, calculate the deviation from the programmed gain relative to G_{RA2}, i.e. $G_{RAG2} = G_{actual}-G_{prog}-G_{RA2}$	-0.5		0.5	dB
Receive gain variation with temperature	G_{RAT}	Measured relative to G_{RA1} or G_{RA2} min. gain < G_R < max. gain	-0.1		0.1	dB
Receive gain variation with supply	G_{RAV}	Measured relative to G_{RA1} or G_{RA2} G_R = maximum gain	-0.1		0.1	dB
Receive gain variation with frequency (SP1 and SP2)	G_{RAF}	Relative to 1.015625 kHz, multitone test technique used. min. gain < G_R < max. gain.				
HPR = 0		f = 60 Hz		-34	-33	dB
		f = 100 Hz		-38	-35	
		f = 200 Hz		-12	-10	
		f = 300 Hz	-1.5	-0.5	0.5	
		f = 400 Hz to 3000 Hz	-0.5		0.5	
		f = 3400 Hz	-1.5	-1.3	0.0	
		f = 4000 Hz		-15	-14	
HPR = 1		f = 60 Hz to 3000 Hz f = 3000 to 4000 Hz, see HPR=0	-0.5		0.5	
Receive gain variation with signal level (SP1)	G_{RAL1}	Sinusoidal test method, reference level = -10 dBm0				
		RX = -40 dBm0 to -3 dBm0	-0.5		0.5	dB
		RX = -50 dBm0 to -40 dBm0	-0.5		0.5	
		RX = -55 dBm0 to -50 dBm0	-1.2		1.2	
Receive gain variation with signal level (SP2)	G_{RAL2}	Sinusoidal test method, reference level = -10 dBm0				
		RX = -40 dBm0 to -3 dBm0	-0.5		0.5	dB
		RX = -50 dBm0 to -40 dBm0	-0.5		0.5	
		RX = -55 dBm0 to -50 dBm0	-1.2		1.2	
Tone Generator gain absolute accuracy	G_{RTONE}	Measure signal level at SP1	-1		1	dB

TRANSMISSION CHARACTERISTICS

◆ Envelope delay distortion with frequency

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TX delay, absolute	D_{TXA}	f = 1600 Hz		800		µs
TX delay, relative	D_{TXR}	f = 500 - 600 Hz		15		µs
		f = 600 - 800 Hz		20		
		f = 800 - 1000 Hz		5		
		f = 1000 - 1600 Hz		-15		
		f = 1600 - 2600 Hz		-40		
		f = 2600 - 2800 Hz		-50		
		f = 2800 - 3000 Hz		-50		
RX delay, absolute	D_{RXA}	f = 1600 Hz		800		µs
RX delay, relative	D_{RXR}	f = 500 - 600 Hz		15		µs
		f = 600 - 800 Hz		20		
		f = 800 - 1000 Hz		5		
		f = 1000 - 1600 Hz		-15		
		f = 1600 - 2600 Hz		-40		
		f = 2600 - 2800 Hz		-50		
		f = 2800 - 3000 Hz		-50		

◆ Noise

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TX noise, P weighted	N_{TXP}	V_{MIC} = 0V, DE = 0, TX gain set to 15 dB		-72*	-68*	dBm0
RX noise, A weighted (max. gain)	N_{RXA}	Receive PCM code = positive zero SI = 0, RTE = 0		140*	190*	μV_{RMS}
Noise, single frequency	N_S	MIC = 0V, loop around measurement from f = 0 Hz to 100 kHz		-76	-50	dBm0
PSRR, TX	$PPSR_{TX}$	MIC = 0V V_{CC} = 3.3V_{DC} + 50 mV_{RMS} f = 0 Hz to 50 kHz	30	44		dB
PSRR, RX	$PPSR_{RX}$	PCM code equals positive zero V_{CC} = 3.3 V_{DC} + 50 mV_{RMS}				
		f = 0 Hz to 4 kHz	30	54		dB
		f = 4 kHz to 50 kHz	30			
Spurious out-band signal at the output (relative to signal)	S_{OS}	RX input set to -6 dBm0 PCM code, 300 Hz 3400 Hz input PCM code applied at RX				
		4600 Hz - 5600 Hz			-45	dB
		5600 Hz - 7600 Hz			-45	
		7600 Hz - 8400 Hz			-50	
		8400 Hz - 20000 Hz			-50	
Common mode rejection ratio	$CMRR_X$	MIC = -6dBm0, max. gain		-74	-45	dB
Tone generator noise	N_{TONE}	DTMF frequencies, TX/SP output		-36	-28	dBm0

*Limit is used to speed up automatic testing. True value is less.

TRANSMISSION CHARACTERISTICS

◆ Distortion

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal to total distortion TX (up to 35 dB gain)	S_{TDTX}	Sinusoidal test method (Linear 300 Hz to 3400 Hz weighting).				
Typical values measured with 35 dB gain		Level = 0 dBm0	56	64		dB
		Level = -6 dBm0	50	60		
		Level = -10 dBm0	48	57		
		Level = -20 dBm0	43	53		
		Level = -30 dBm0	38	44		
		Level = -45 dBm0	24	29		
		Level = -55 dBm0	15	19		
Single frequency distortion transmit	S_{DTX}	0 dBm0 input signal		-70	-56	dB
Signal to total distortion SP1/SP2 (up to 20 dB attenuation)	S_{TDSP1} S_{TDSP2}	Sinusoidal test method (Linear 300 Hz to 3400 Hz weighting). Load is 1000 or 30 Ω.				
		Level = -6 dBm0	45* 50	60		dB
		Level = -10 dBm0	45* 48	60		
		Level = -20 dBm0	43* 43	55		
		Level = -30 dBm0	38* 38	50		
		Level = -45 dBm0	24* 24	40		
		Level = -55 dBm0	15* 15	28		
Single frequency distortion receive SP1/SP2	S_{DSP1} S_{DSP2}	-6 dBm0 input signal		-62	-45	dB
Signal to distortion of tone generator signals	S_{TONE}	DTMF frequencies Linear 300 Hz to 3400 Hz weighting.	28	42		dB
Intermodulation	IMD	Loop around measurement voltage at MIC = -10 dBm0 to -27 dBm0, 2 frequencies in the range 300 Hz to 3400 Hz		-61	-46	dB

*max. load (30Ω) and min. V_{CC} (2.7V)

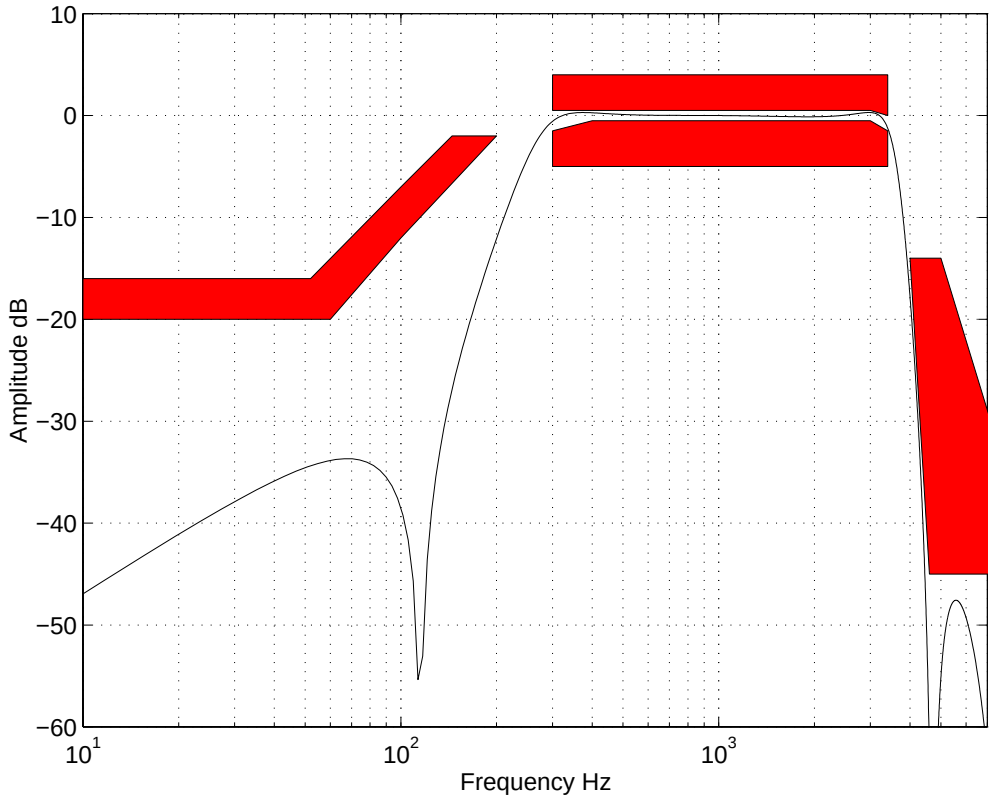
◆ Crosstalk

(V_{CC} = 2.7-3.6V or 4.5-5.5V, T_A = -30°C to +85°C, unless otherwise specified)

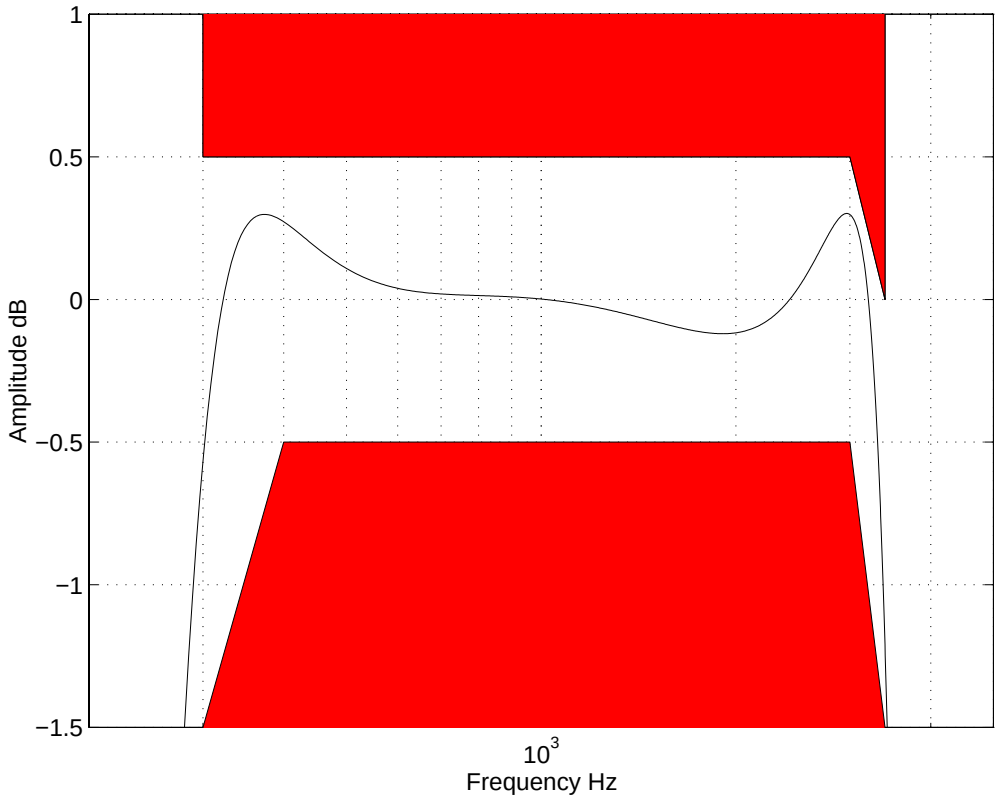
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transmit to receive	C_{TX-RX}	Transmit level = 0 dBm0 f = 300 Hz to 3400 Hz RX = quiet PCM code		-82	-65	dB
Receive to transmit	C_{RX-TX}	Receive level = -6 dBm0 f = 300 Hz to 3400 Hz MIC = 0V		-75	-60	dB

RESPONSES

◆ RX frequency response

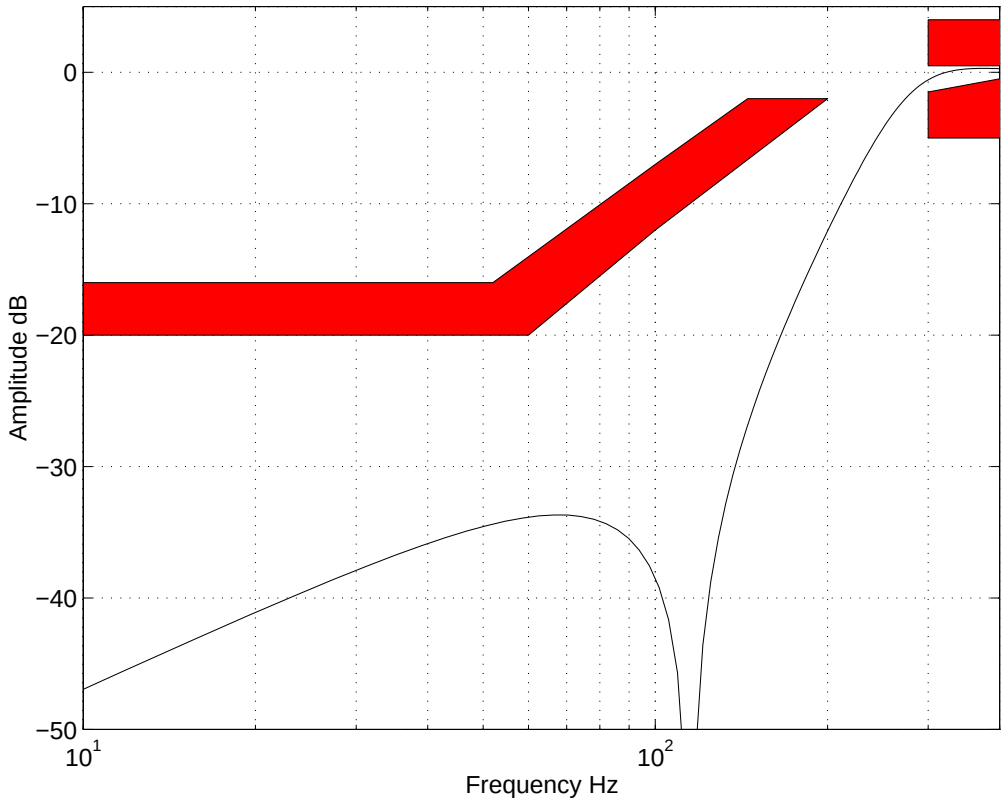


◆ RX frequency response (passband)

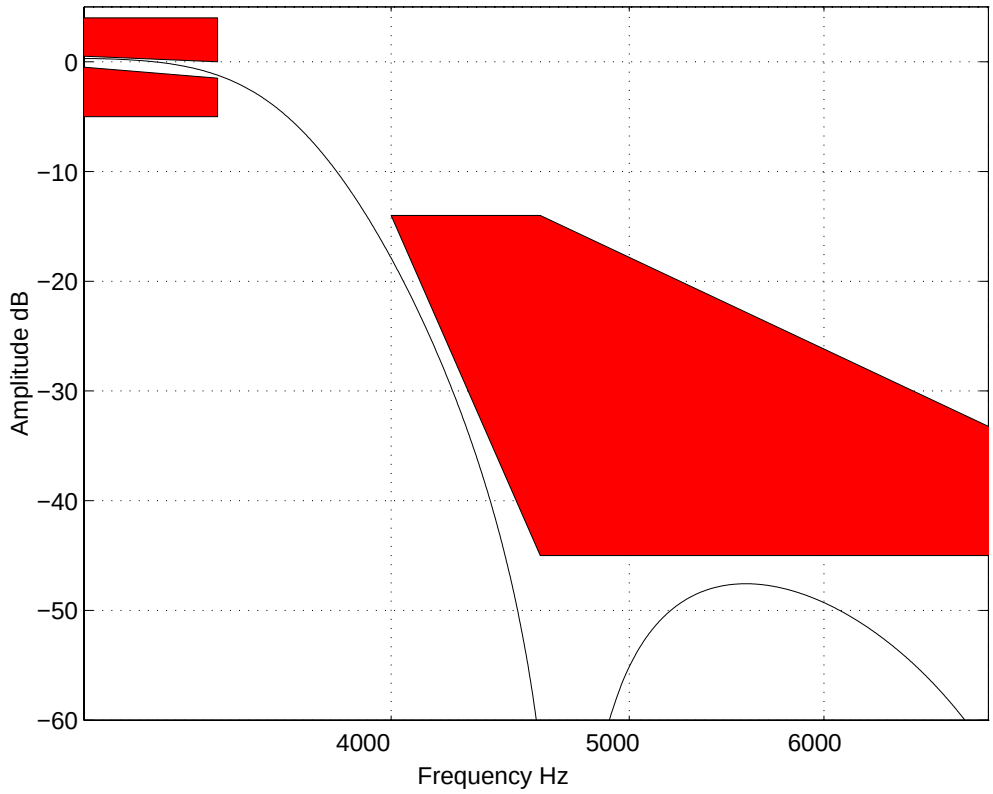


RESPONSES

◆ **RX frequency response (stopband low)**

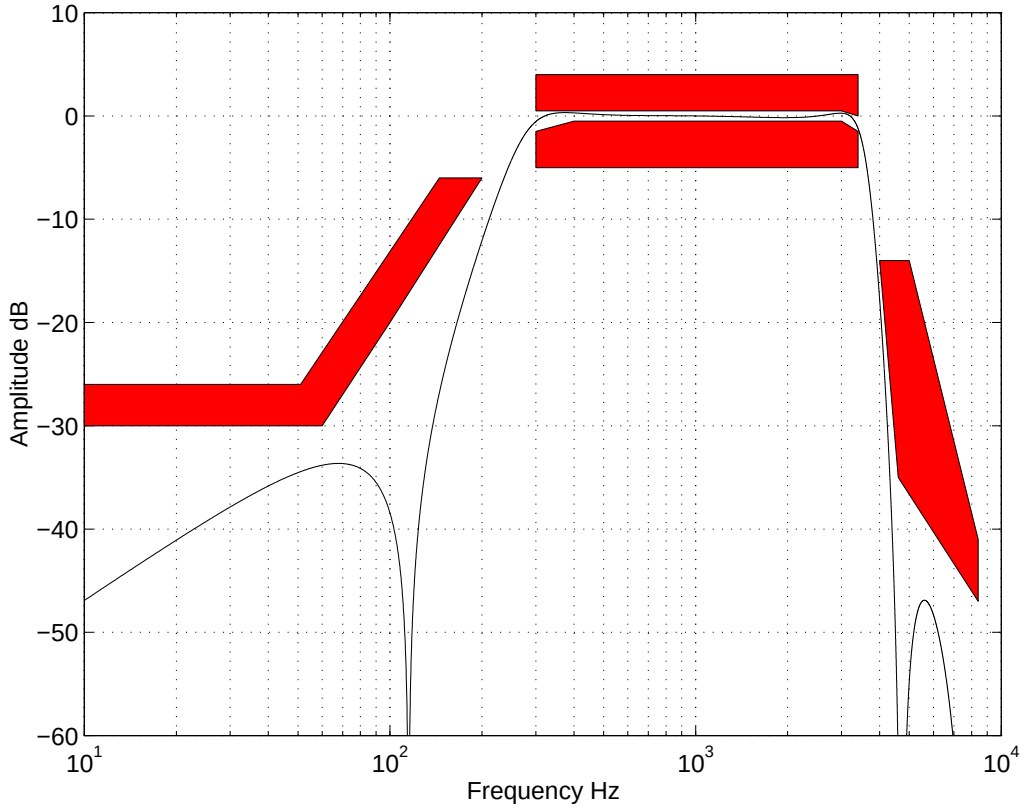


◆ **RX frequency response (stopband high)**

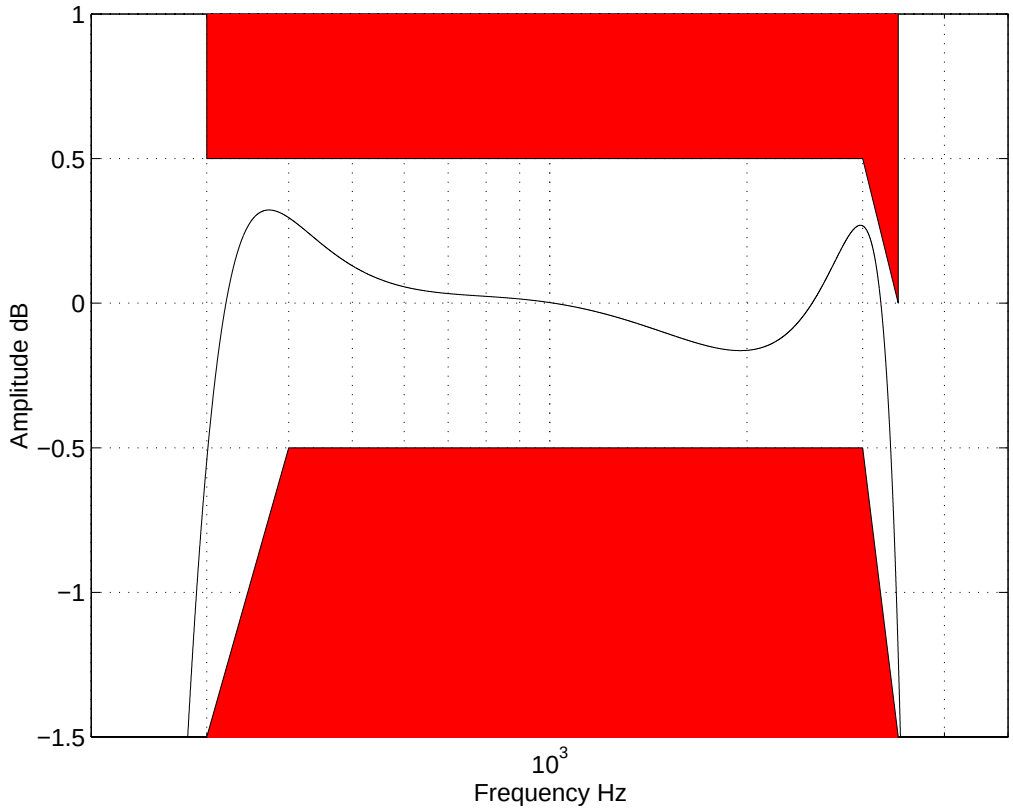


RESPONSES

◆TX frequency response

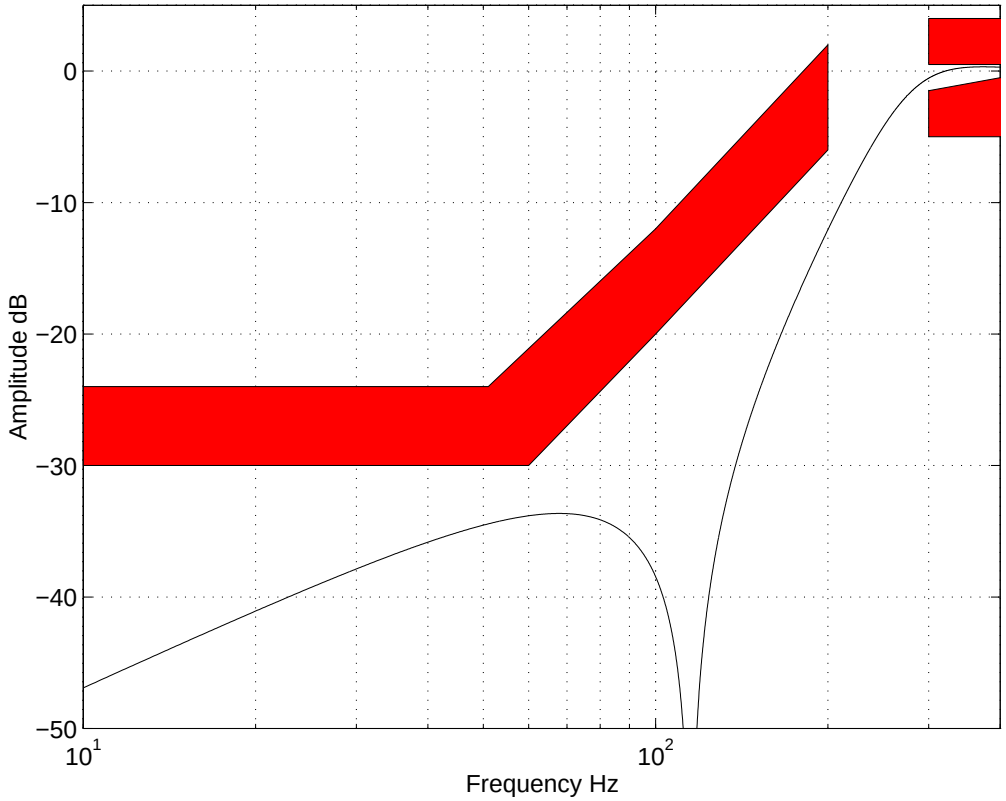


◆TX frequency response (passband)

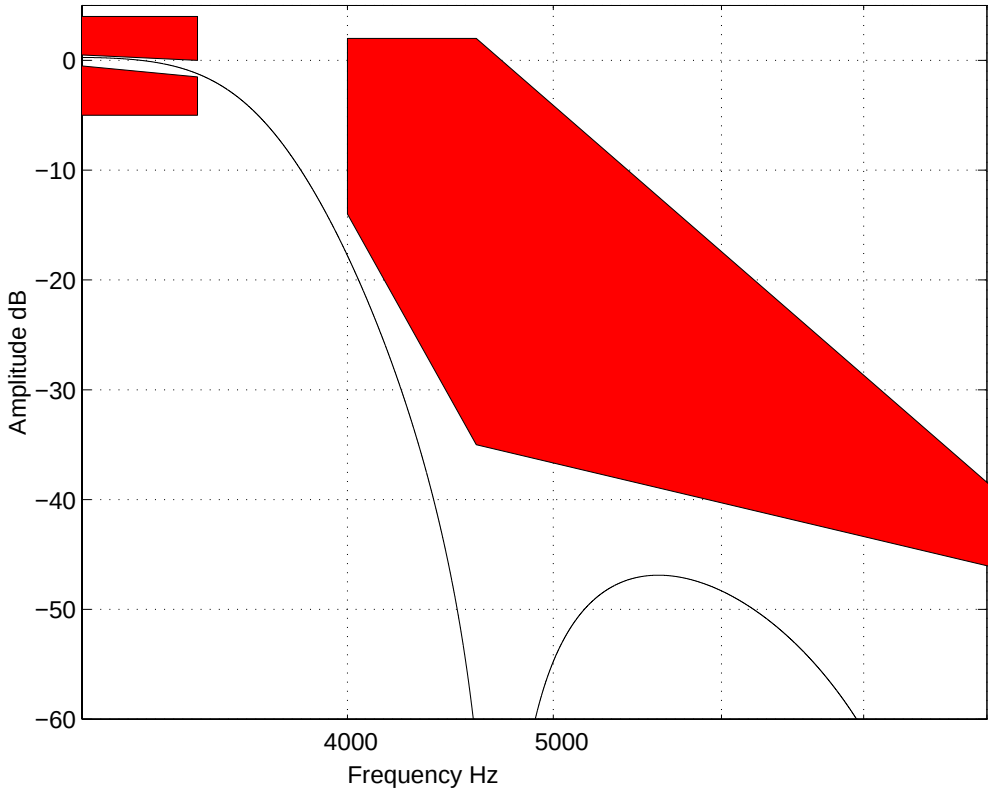


RESPONSES

◆TX frequency response (stopband low)



◆TX frequency response (stopband high)

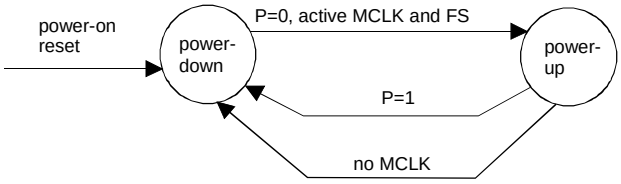


FUNCTIONAL DESCRIPTION

◆ Operating Modes

When power is first applied, power-on reset circuit initializes control and data registers of MAS9090 and puts it into a power-down state. During power-down state, control registers retain their initial state until they are written via the serial interface. Master clock (MCLK) can be inactive.

The power up/down control is accomplished by changing the P-bit of the address byte of the serial interface ("0" means active and "1" power-down) or by stopping the master clock.



◆ Control Interface

Control information or data is written into or read-back from the internal registers of MAS9090 via the serial control port. Serial control port consists of control output CO, control input CI, chip select CS- and control clock CCLK and supports the MICROWIRE™*) communication protocol. All control instructions, except the single byte power up/down command require two bytes of data**.**

To shift the data into MAS9090, CCLK must be pulsed eight times (CS is low). Data on the CI input is shifted into the serial input register on the rising edges of CCLK pulses. After 8 bit address data is shifted in, the content of the shift register is decoded and may indicate that 8 bit control word will follow. Control word may start immediately after the address byte or after a single CS pulse. It is not mandatory for the CS signal to return high in between the address and the data. After the second byte is shifted in, the CS signal must return to a high state.

The same process takes place for reading-back status information during the next CS low state. CS will remain low for eight CCLK pulses. The data is shifted out on the CO output from the serial output register on the falling edges of CCLK. When CS is high, the CO pin is in a high impedance state, which enables CO pins of other devices to be multiplexed together.

◆ Digital Data Interface

Digital data is shifted in/out from RX/TX using master clock (MCLK) and Frame Sync (FS) signals. FS determines the beginning of frame and its duration can vary from single cycle of MCLK to squarewave.

Three different modes between FS and the first time slot of a data frame can be used: non-delayed normal data timing, non-delayed reverse data timing and delayed data timing. These modes are set with bits DM0 and DM1 of control register CR1.

In non-delayed timing modes the first time slot begins coincident with the rising edge of the FS. In delayed timing mode the FS must be active at least one half cycle of MCLK before the beginning of the first time slot.

Bit EN of control register CR1 enables the voice data transfer on TX and RX pins. Data is shifted out from TX output on the rising edge of MCLK and shifted into RX on falling edge of MCLK on assigned time slot. In non-delayed reverse mode the data is shifted with different edge of MCLK (on falling edge from TX and on rising edge into RX). TX output is in tristate condition during non selected time slots. The TX output transmits 8 bits of encoded data (A-law or µ-law) or 16 bits (14 effective bits, 2 LSB bits zero) of linear data when compressor is bypassed.

Two time slots (B1 and B2) can be used in two formats: in Format 1, time slot B1 corresponds to eight MCLK cycles starting immediately after the rising edge of FS and time slot B2 starts immediately after the B1 is ended. A two-bit space is left after B2 for insertion of possible D channel data. The position of this two-bit data is changed in Format 2 to the center of time slots B1 and B2. The data format is selected by bit FF in control register CR0 and time slots B1 and B2 are selected by bit TS in control register CR1.

◆ Control Channel Access to PCM Interface

When companded code is selected it is possible to access the selected time slot (B1 or B2) by writing data bytes to internal registers CR2 and CR3. The byte written to CR3 is transmitted from TX with the following frame in place of PCM data if bit MX (3) of CR1 is selected. To implement a continuous data flow from interface to B channel a control byte has to be sent on each PCM frame.

The byte written into CR2 is sent through the receive audio path (RX) if bit MR (4) of CR1 is selected. CR2 can also be used to read the RX input. In order to implement a continuous data flow from B channel to the interface, register CR2 has to be read at each PCM frame.

*) Trade Mark of National Semiconductor

FUNCTIONAL DESCRIPTION

◆ TX Audio Path

Analog front end provides three identical differential inputs (MIC1, MIC2, MIC3) for capacitive connection of microphones or auxiliary audio circuits. Desired input signal is selected with bits VS and TE (6 and 7) of register CR4 and forwarded to a low noise preamplifier.
Preamplifier has 15.7 dB gain and its output is fed to the programmable gain amplifier which provides an additional gain from 0 to 22.5 dB in 1.5 dB steps. Gain is controlled with bits 4-7 of register CR5.

An active RC anti alias filter is used to prevent signal folding during the sampling. Accurate analog to digital conversion is done by using a sigma-delta modulator followed by a decimation filter.
Digital multiplexer (bit DE (0) in CR 7) is used to select the input of a digital bandpass filter (300-3400 Hz). The input can be taken from the output of the decimator or from an internal ring/tone generator. The bandpass filter output contains hard clipping saturation logic for signals exceeding overload level (+3.14 dB). Highpass part of the bandpass filter can be bypassed with bit HPT of register CR10.

Output data can be compressed by using CCITT A-law or μ255-law coding. The compression code is selected with bits CM (5), MA (4) and IA (3) of register CR0.

◆ RX Audio Path

Received signal is transferred into RX register in 8 bit encoded format or in 16 bit linear format. The data is expanded by using A-law or μ-law signal encoding according to CCITT A and μ255 laws. The expansion code is selected with bits CM (5), MA (4) and IA (3) of register CR0. Signal is then passed through a bandpass filter (bandpass 300-3400 Hz). The high pass section of the filter can be bypassed with bit HPR of register CR4.

The input signal of RX gain3 is controlled with bits SI (5), RTE (2) and SE (0) of register CR4. Bit SI activates the transmit side tone signal, bit RTE activates the ring/tone generator and bit SE activates the received signal to be summed to the gain input. RX gain3 can be programmed with bits 4-7 of register CR6 from 0 dB to -30 dB with -2dB steps. It contains also hard-clipping saturation logic.

After gain adjustment the signal is fed to a digital sigma-delta modulator followed by a switched capacitor (SC) reconstruction filter and a continuous time smoothing filter. Filtered analog signal can be directed to a speaker amplifier (SP1) or to an extra analog output amplifier (SP2) with bits OE1 (4) and OE2 (3) of register CR4. Gains can be set with register CR6 in the range of 0 to -30 dB in -2 dB steps.

Differential analog outputs (SP1, SP2) are capable of directly driving output load of 30 Ω with power level up to 66mW. Also ceramic receivers up to 50nF can be used. Power up transient noise suppression is used in both outputs.

◆ Ring and tone generator

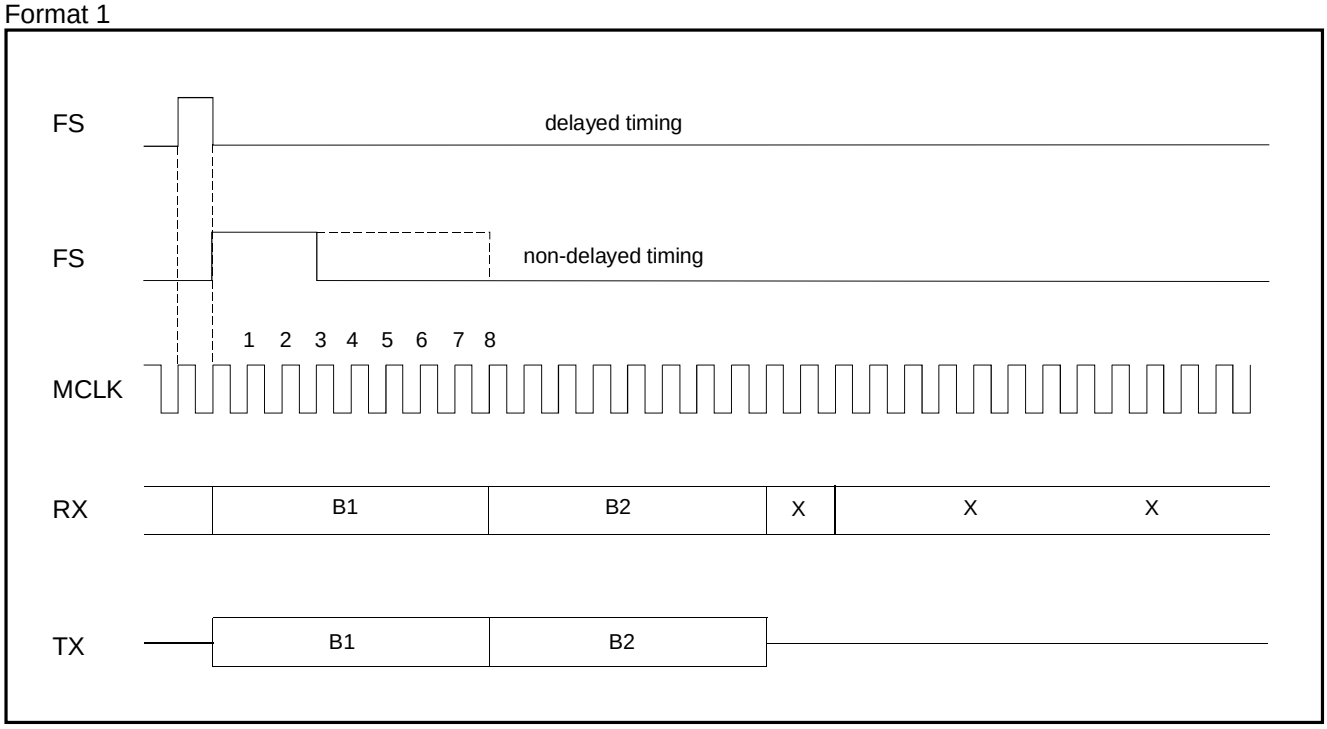
Ring/tone generator is able to generate one or two sinewave or squarewave frequencies (including DTMF tones) to the transmit (TX) receive (RX) or buzzer paths. Generated frequencies can be programmed with registers CR8 and CR9. One of the three frequency ranges can be selected with bits DFT and HFT of register CR10. Output signal level of the tone generator can be selected from 0 to -27 dB with -3dB steps with bits 4-7 of register CR7.

Single ended BZ output is used to drive a buzzer by using an external bipolar transistor with pulse width modulated (PWM) squarewave signal f1 (CR8). This PWM signal can also be amplitude modulated with signal f2 (CR9). Maximum load for BZ is 5 kΩ and 50pF. Implementation of tone generator is fully digital. Therefore no amplitude or frequency response variations (at TX output) over temperature, power supply or from unit to unit exist.

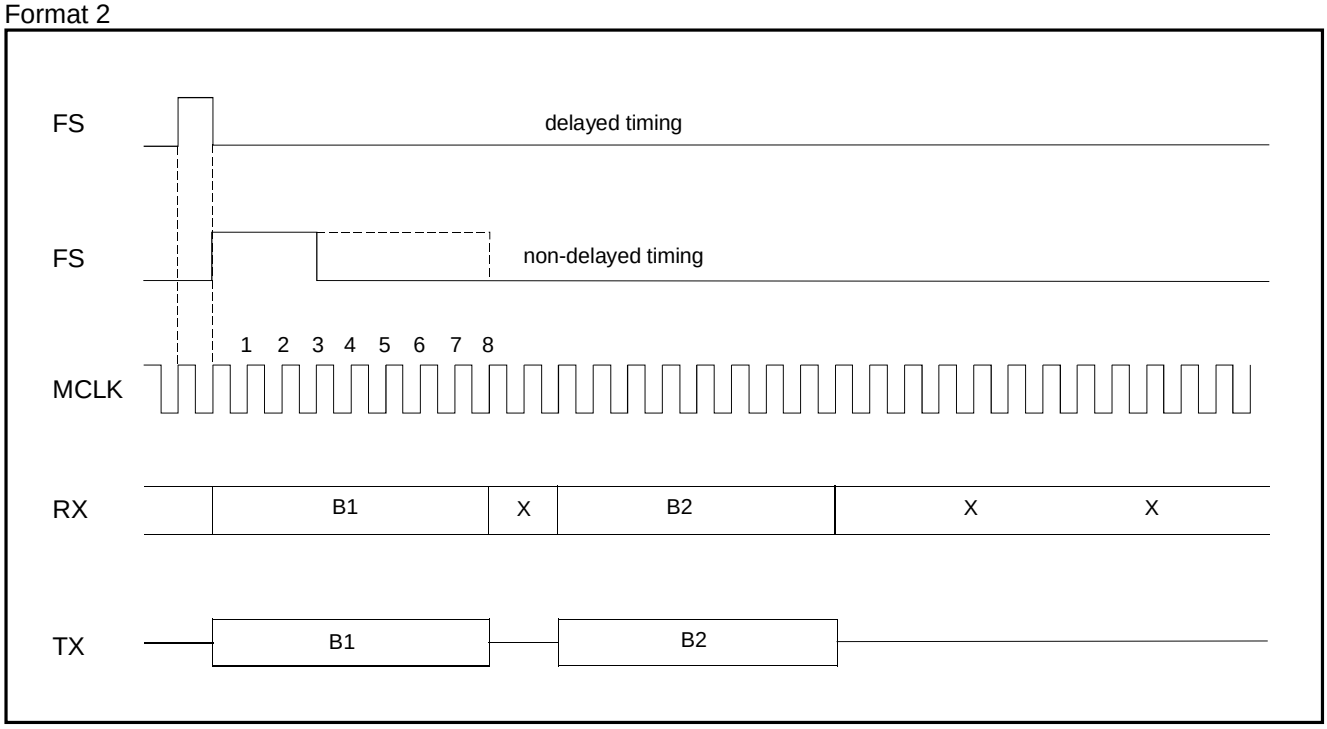
FUNCTIONAL DESCRIPTION

◆ Digital Interface Format

Format 1



Format 2



FUNCTIONAL DESCRIPTION

◆ Registers

Register Map

Register	Address Byte								I/O	Data Byte							
	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
Power	P	X	X	X	X	X	0	X									
CR0	P	0	0	0	0	0	1	X	Write	F1	F0	CM	MA	IA	FF	B7	DL
	P	0	0	0	0	1	1	X	Read								
CR1	P	0	0	0	1	0	1	X	Write	DM1	DM0	DO	MR	MX	EN	TS	SV
	P	0	0	0	1	1	1	X	Read								
CR2	P	0	0	1	0	0	1	X	Write	Input data [0:7]							
	P	0	0	1	0	1	1	X	Read								
CR3	P	0	0	1	1	0	1	X	Write	Output data [0:7]							
	P	0	0	1	1	1	1	X	Read								
CR4	P	0	1	0	0	0	1	X	Write	VS	TE	SI	OE1	OE2	RTE	HPR	SE
	P	0	1	0	0	1	1	X	Read								
CR5	P	0	1	0	1	0	1	X	Write	TX gain [4:7]				Side tone gain [0:3]			
	P	0	1	0	1	1	1	X	Read								
CR6	P	0	1	1	0	0	1	X	Write	SP1 gain [4:7]				SP2 gain [0:3]			
	P	0	1	1	0	1	1	X	Read								
CR7	P	0	1	1	1	0	1	X	Write	Tone gain [4:7]				F1	F2	SN	DE
	P	0	1	1	1	1	1	X	Read								
CR8	P	1	0	0	0	0	1	X	Write	Binary word used for calculating f1							
	P	1	0	0	0	1	1	X	Read								
CR9	P	1	0	0	1	0	1	X	Write	Binary word used for calculating f2							
	P	1	0	0	1	1	1	X	Read								
CR10	P	1	0	1	0	0	1	X	Write	POR	SCA	HPT	EXT	LI	LO	DFT	HFT
	P	1	0	1	0	1	1	X	Read								
CR11	P	1	0	1	1	0	1	X	Write	BE	BI	Duty cycle for BZ (0:5)					
	P	1	0	1	1	1	1	X	Read								
CR14	X	X	X	X	X	X	X	X		For testing purposes only							

Address byte bits:

- Bit 0 reserved for future extensions
- Bit 1 indicates the presence of a second byte. If cleared indicates single byte power up/down command
- Bit 2 is write/read select bit
- Bits 6 to 3 contain the address of register
- Registers CR12, CR13, CR15 are not accessible
- MSB bit (bit 7) of the address and data byte is always clocked first into or out from CI and CO pins
- Bit 7 ‘P’ controls the power up/down state of the chip. P = 1 means power down

Data bits:

- All registers are cleared during power on reset or by writing to bit POR of CR10
- Default value for all bits is zero.

Notice the difference between power down and POR. Registers can be written in both power down/up states and they retain their values in power down. Both data and control registers are cleared when POR bit (in CR10) is written high or during power on reset (i.e. Vcc transition from 0 volts to 3-5 volts).

FUNCTIONAL DESCRIPTION

Control register CR0

7	6	5	4	3	2	1	0	Function
F1	F0	CM	MA	IA	FF	B7	DL	
0	0							MCLK = 512 kHz *
0	1							MCLK = 1536 kHz
1	0							MCLK = 2048 kHz
1	1							Not implemented
		0						Linear code *
			0	0				2's complement *
			0	1				sign and magnitude
			1	0				2's complement
			1	1				1's complement
		1						Companded code
			0	0				μ-Law: CCITT D3-D4
			0	1				μ-Law: bare coding
			1	0				A-Law: including even bit inversions
			1	1				A-Law: bare coding
					0			B1 and B2 consecutive (1)*
					1			B1 and B2 separated (1)
						0		8-bit time slot (1)*
						1		7-bit time slot (1)
							0	Normal operation (default) *
							1	Digital loop back (TX and RX muted)

Control register CR1

7	6	5	4	3	2	1	0	Function
TM1	TM0	DO	MR	MX	EN	TS	SV	
0	X							Delayed data timing *
1	0							Non-delayed normal data timing
1	1							Non-delayed reverse data timing
		0						LO latch set to 1 *
		1						LO latch set to 0
			0					RX connected to RX path *
			1					CR2 connected to RX path (1)
				0				TX path connected to TX *
				1				CR3 connected to TX (1)
					0			Voice data transfer disable *
					1			Voice data transfer enable
						0		B1 channel selected (1)*
						1		B2 channel selected (1)
							0	2.7-3.6V power supply *
							1	5.0V power supply

(1) significant in companded mode only
* state at power on initialization

FUNCTIONAL DESCRIPTION

Control register CR2

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb								Data sent to RX path or data received from RX input

Control register CR3

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb								TX data transmitted

Control register CR4

7	6	5	4	3	2	1	0	Function	
VS	TE	SI	OE1	OE2	RTE	HPR	SE		
0	0							TX input muted	*
0	1							MIC1 selected	
1	0							MIC2 selected	
1	1							MIC3 selected	
		0						Internal side tone disabled	*
		1						Internal side tone enabled	
			0	0				RX output muted	*
			0	1				SP1 output selected	
			1	0				SP2 output selected	
			1	1				NOT ALLOWED	
					0			Ring/Tone to SP1 or SP2 disabled	*
					1			Ring/Tone to SP1 or SP2 enabled	
						0		Receive HP filter enabled	*
						1		Receive HP filter disabled	
							0	RX signal to SP1 or SP2 disabled	*
							1	RX signal to SP1 or SP2 enabled	

Control register CR5

7	6	5	4	3	2	1	0	Function	
TX Gain				Sidetone Gain					
0	0	0	0					0 dB gain	*
0	0	0	1					1.5 dB gain	
-	-	-	-					in 1.5 dB steps	
1	1	1	1					22.5 dB gain	
				0	0	0	0	-12.5 dB gain	*
				0	0	0	1	-13.5 dB gain	
				-	-	-	-	in 1 dB steps	
				1	1	1	1	-27.5 dB gain	

* state at power on initialization

FUNCTIONAL DESCRIPTION

Control register CR6

7	6	5	4	3	2	1	0	Function
Earpiece Gain (SP1)				Extra Gain (SP2)				
0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1					0 dB gain * -2 dB gain in -2 dB steps -30 dB gain
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	0 dB gain * -2 dB gain in -2 dB steps -30 dB gain

Control register CR7

7	6	5	4	3	2	1	0	Function			
Tone gain				f1	f2	SN	DE	Attenuation	f1 dBm0	f2 dBm0	f1+f2 dBm0
0 0 0 0 0 0 0 0 1 1	0 0 0 0 1 1 1 1 X X	0 0 1 1 0 0 1 1 X X	0 1 0 1 0 1 0 1 0 1					0 dB gain * -3 dB -6 dB -9 dB -12 dB -15 dB -18 dB -21 dB -24 dB -27 dB	1.20 (2) -25.80	-0.87 (2) -27.87	-1.81 (2) -28.81
				0 0 1 1	0 1 0 1			f1 and f2 muted * f2 selected f1 selected f1 and f2 in summed mode			
						0 1		Squarewave signal selected * Sinewave signal selected			
							0 1	Normal operation * Tone/Ring generator connected to TX path			

Control register CR8

7	6	5	4	3	2	1	0	Function
d7	d6	D5	d4	d3	d2	d1	d0	
msb								f1 control word

Control register CR9

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb								f2 control word

(2) values are calculated from TX output, levels on RX are 6 dB smaller
X don't care
* state at power on initialization

FUNCTIONAL DESCRIPTION

Control register CR10

7	6	5	4	3	2	1	0	Function
POR	SCA	HPT	EXT	L1	L0	DFT	HFT	
0 1								Normal operation * Set power-on-reset initialization
	0 1							Normal operation * Scan. CI is input, DX is output. For device testing.
		0 1						Normal operation * Bypass TX highpass filter
			0 1					Normal operation * Read 2-bit input to the decimator. For device testing (CI and DR)
				0 1				Normal operation * Loop from expander to compressor
					0 1			Normal operation * Loop from TX to Rx
						0 0 1 1	0 1 0 1	Standard frequency tone range * Halved frequency tone range Double frequency tone range Forbidden

Control register CR11

7	6	5	4	3	2	1	0	Function
BE	BI	BZ5	BZ4	BZ3	BZ2	BZ1	BZ0	
0 1								Buzzer Output disabled (set to 0) * Buzzer output enabled
	0 1							Duty cycle is relative to width of logic 1 * Duty cycle is relative to width of logic 0
		msb						Duty cycle control word

Control register CR14 (for testing purposes only)

7	6	5	4	3	2	1	0	Function	
AM2	AM1	AM0	DM2	DM1	DM0	MUX	EDX		
								rxtest pin	Txtest pin
0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1						VSA Anti-image filter DAC output RX pos. reference RX neg. reference RX agnd NC NC	VSA Gain amplifier VSA Anti-image filter VSA VSA VSA NC
			0 0 0 0 1 1	0 0 1 1 X X	0 1 0 1 0 1			TX (configured for test by MUX) Power-on reset Input of TX bandpass filter Sign bit of DIGSDM 512 kHz clock (phi1) internal frame sync Output of RX gain3	
						0 1		Normal operation Connect selected test outputs to TX output	
							0 1	Normal operation Enable TX output continuously	

* state at power on initialization

REGISTER DESCRIPTION

Control register CR0

Master Clock Frequency Selection:

External MCLK frequency can be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz. During initialization Bits F1 (7) and F0 (6) must be set to select correct value for internal clock divider. Default value for external MCLK is 512 kHz. Any other value must be selected before Power up command.

Coding Selection

Bit CM (5) permits selection of 14-bit linear coding or companded coding. Default is linear mode.

In case of companded mode (CM=1) bits MA (4) and IA (3) select either μ-255 or A law coding mode and the format for both.

In case of linear mode (CM=0) bits MA (4) and IA (3) select the linear data to be in 2's complement, 1's complement or sign and magnitude format.

Digital Interface Format (1)

Bit FF (2) selects the format for TX and Rx data transfer. If FF=0 Format 1 is selected and channels B1 and B2 are consecutive. FF = 1 selects Format 2 where channels B1 and B2 are separated by two bits.

56+8 Selection (1)

If bit B7 (1) is selected MAS9090 takes only seven most significant bits of the companded PCM data byte. LSB bit on RX is ignored and LSB bit on TX is in high impedance state. This allows direct connection of an external "in band" data generator to the digital interface.

Digital Loopback

Bit DL (0) selects the digital loopback mode, where data written into RX data register (CR2) from received time slot is read-back from that register in the selected time-slot on TX.

No PCM decoding or encoding takes place in this mode.

Control Register CR1

Digital Interface Timing

Bit TM1 (7) selects the timing mode for digital interface. As a default (TM1=0) delayed timing mode is selected. In delayed mode (TM1=1) bit TM0 (6) selects the normal (TM0=0) or reversed timing mode (TM0=1).

Latch output control

Bit DO (5) controls directly the LO output pin. Bit written to DO is seen inverted from the output LO.

Microwire access on RX path (1)

When bit MR (4) is set high the data written into register CR2 is decoded each frame and sent to receive path. Data input RX is ignored when MR is high.

In other direction, current PCM data input received at RX can be read from register CR2 each frame.

Microwire access on TX path (1)

Bit MX (3) enables the access of write only register CR3 to TX output. When MX is set active data written to CR3 is send to TX output every frame. PCM encoder is ignored.

Transmit/Receive enable/disable

Bit EN (2) enables or disables voice data transfer on TX and RX pins. When disabled PCM data from RX input is not decoded and TX output is on high impedance state. Default value is disabled.

B-channel selection (1)

Bit TS (1) selects the active channel B1 or B2. Default (TS=0) is B1 channel. (See Fig on page 14)

Power supply selection

Bit SV (0) selects the main supply voltage used. When SV is low a 2.7-3.6 V supply is assumed. When SV is high 4.5-5.5 V is expected.

Control Register CR2 (1)

Data sent to receive path or data received from RX input is seen in register CR2. See register CR1 bit MR (4).

Control Register CR3 (1)

TX data transmitted. Refer to bit MX (3) in CR1.

(1) Significant in companded mode only

REGISTER DESCRIPTION

Control Register CR4

Transmit Input Selection

Bits VS (7) and TE (6) select active input (MIC1, MIC2 or MIC3). Default is that all inputs are muted. Transmit (TX) gain can be adjusted from 0 to 22.5 dB in 1.5 dB steps with register CR5 bits (7:4).

Sidetone Selection

Transmit signal after bandpass filter can be fed back to the receive amplifiers when bit SI (5) is set high.

Output Driver Selection

Bits OE1 (4) and OE2 (3) select the active output of the RX gain to be SP1 or SP2. Both outputs can be muted.

Ring/Tone Signal Selection

Bit RTE (2) connects the on-chip Ring/Tone generator to the RX gain input.

Receive High Pass Filter Selection

Bit HPR (1) provides possibility to bypass high pass section of the receive bandpass filter.

PCM receive data selection

Bit SE (0) enables the connection of the received signal to the RX gain input.

Control Register CR5

Transmit Gain Selection

TX gain can be programmed from 0 to 22.5 dB in 1.5 dB steps with bits (7:4).

Sidetone Attenuation Selection

Transmit signal picked after digital bandpass filters can be fed back to RX gain. Attenuation of the sidetone signal can be programmed from –12.5 dB to –27.5 dB in 1 dB steps with bits (7:4). Attenuation is relative to the input signal level of bandpass filter.

Control Register CR6

Speaker 1 and 2 Gain Selection

The attenuation of both speaker gains can be programmed separately from 0 to –30 dB in 2 dB steps with bits (7:4) and (3:0).

0 dBm0 voltage at the output of the RX gain on pins SP1/2+ and SP1/2- is 1.965 Vrms when 0 dB gain is selected. When –30 dB gain is selected the 0 dBm0 level is 61.85 mVrms.

Control Register CR7

Tone/Ring Gain Selection

Output of Tone/Ring generator can be attenuated from 0 to –27 dB in 3 dB steps with bits (7:4).

Frequency Mode Selection

Bits f1 (3) and f2 (2) permit selection of f1 and/or f2 frequency generators. When f1 (f2) is selected the output of the tone generator is signal at the frequency programmed by the register CR8 (CR9). If both f1 and f2 are selected the output is a sum of both signals. In case of squarewave the f1 is amplitude modulated by f2. In order to meet DTMF specifications the level of f2 is attenuated by 2 dB relative to f1.

Waveform Selection

Bit SN (1) selects the output waveform of the tone generator to be square (SN=0) or sinewave (SN=1).

DTMF Selection

Bit DE (0) permits the connection of the tone generator to the transmit path. Speaker output can also be provided by using sidetone circuit (bit SI of CR4) or directly connecting the tone generator to RX gain with bit RTE of CR4.

REGISTER DESCRIPTION

Control Registers CR8 and CR9

The frequency of both frequency generators is programmed by CR8 and CR9.

When standard frequency range is selected (CR10: DFT=0, HFT=0) the frequency is defined by formulas: f1 = CR8 / 0.128 Hz and f2 = CR9 / 0.128 Hz, where CR8 and CR9 are decimal equivalents of the register content. Thus any frequency between 7.8 Hz and 1992 Hz in 7.8 Hz step can be selected.

When halved frequency range is selected (CR10:DFT=0, HFT=1) the frequency is defined by formulas: f1 = CR8 / 0.256 Hz and f2 = CR9 / 0.256 Hz. Thus any frequency between 3.9 Hz and 996 Hz in 3.9 Hz step can be selected.

When doubled frequency range is selected (CR10:DFT=1, HFT=0) the frequency is defined by formulas: f1 = CR8 / 0.064 Hz and f2 = CR9 / 0.064 Hz. Thus any frequency between 15.6 Hz and 3984 Hz in 15.6 Hz step can be selected.

Control Register CR10

Writing bit POR (7) high puts the MAS9090 in power-on-reset state and all data and control registers are cleared (including the POR bit).

Logic low written to bit SCA (6) sets the chip to scan mode. During scan CI is the input and TX is the output. Used only for device testing.

High written to bit HPT (5) bypasses the highpass part of the TX bandpass filter.

When Bit EXT (4) is set active the two bit output of the ADC is disabled and data is fed from pins CR and DR. Used only for device testing.

With bit L0 (3) it is possible to loop internally from TX to RX. Bit L1 (2) permits looping from the expander output to the compressor input.

Frequency Range Selection

Bits DFT (1) and HFT (0) define the frequency range of the tone generator output. Three modes are possible: halved, standard and doubled with output frequencies from 3.9…996 Hz and 7.8…1992 Hz, 15.6…3984 Hz respectively.

Control Register CR11

When bit BE (7) is high it permits the connection of f1 squarewave pulse width modulated (PWM) ring signal to buzzer driver output pin BZ. Signal can be amplitude modulated (AM) with squarewave signal f2.
When bit BE is low (buzzer disabled) the state of the output pin BZ is logical inversion of bit BI (6). This works also in power-down state.

When buzzer output is enabled (BE = 1) bit BI (6) controls the polarity of the duty cycle selection. BI = 1 means the duty cycle is calculated from the relative width of the logic one. When BI = 0 the duty cycle is calculated from the relative width of the logic zero.

Bits BZ5:BZ0 (5:0) define the duty cycle of the PWM squarewave, according to the following formula: duty cycle = CR11(5:0) x 0.78125 %, where CR11 (5:0) is the decimal equivalent of binary value BZ5:BZ0.

Control Register CR14 (for testing)

Bits AM2:AM0 (7:5) control the analog multiplexer. Different analog test signals can be fed to test pads. Test pads are not wire bonded in production packages.

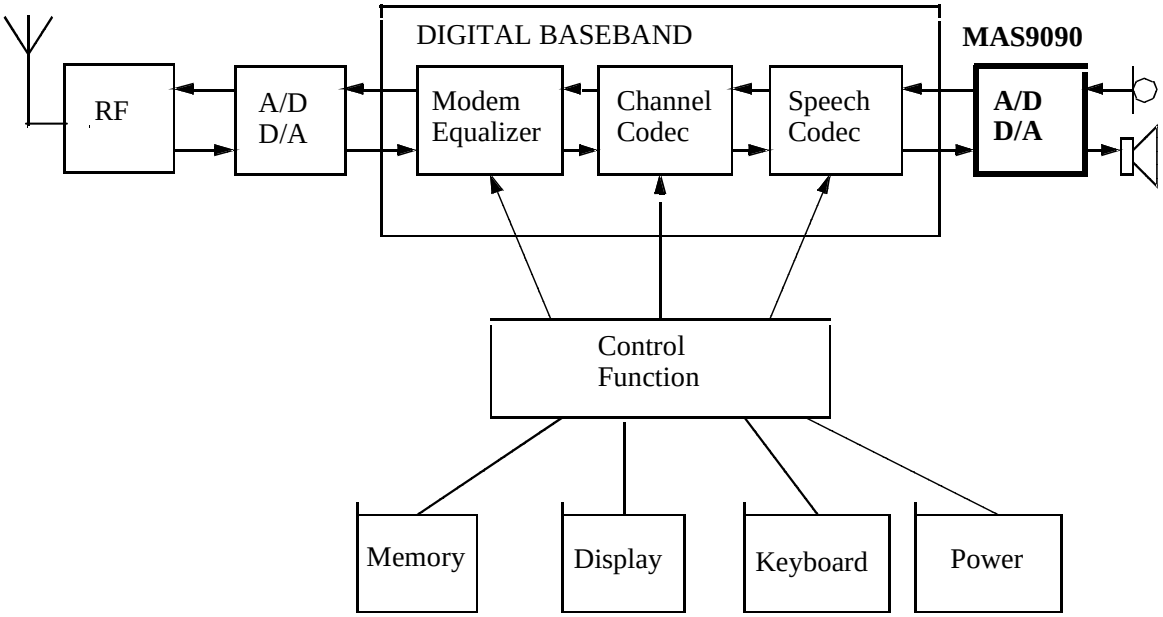
Bits DM2:DM0 (4:2) control the digital multiplexer. Different test signals can be fed to the TX output pin.

Bit MUX (1) connects the test outputs to the TX output pin. It is for device testing.

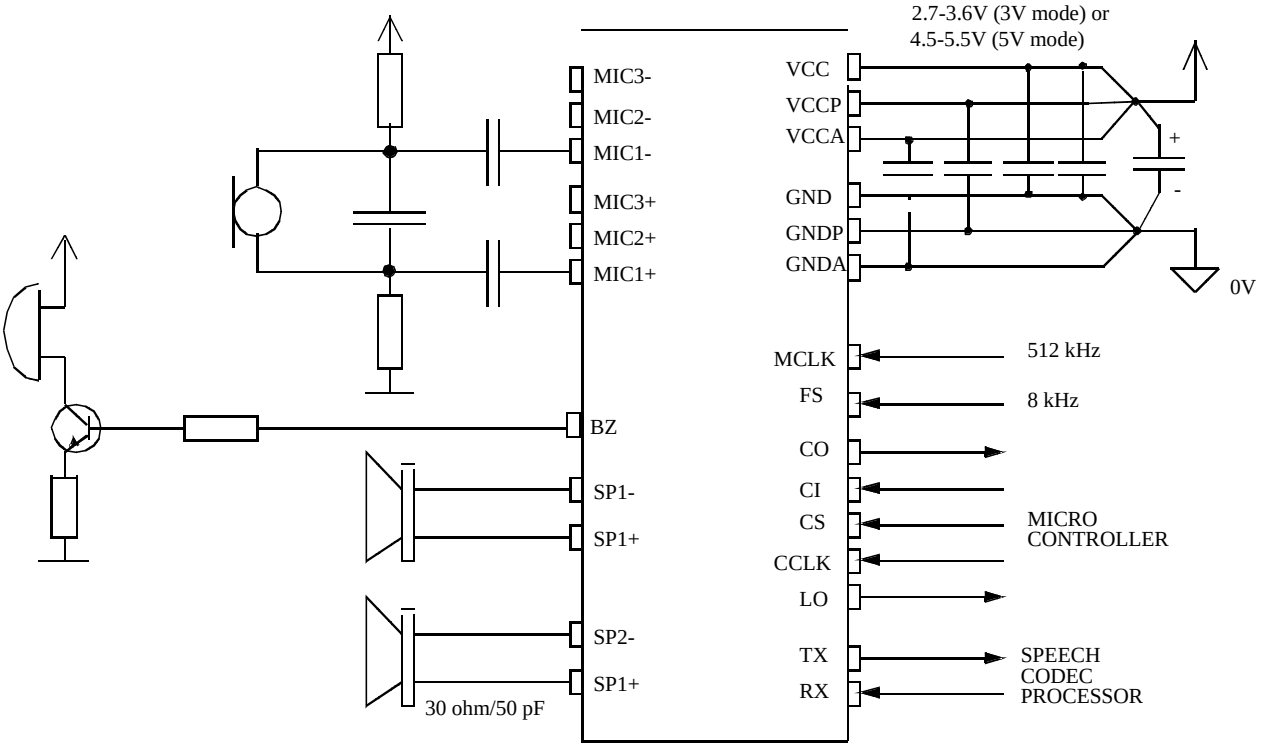
Bit EDX (0) enables the TX output continuously. No pull-up resistor is needed when TX pin is the only output for the reading device and EDX is written High.

APPLICATION INFORMATION

Typical application of MAS9090 for digital cellular systems

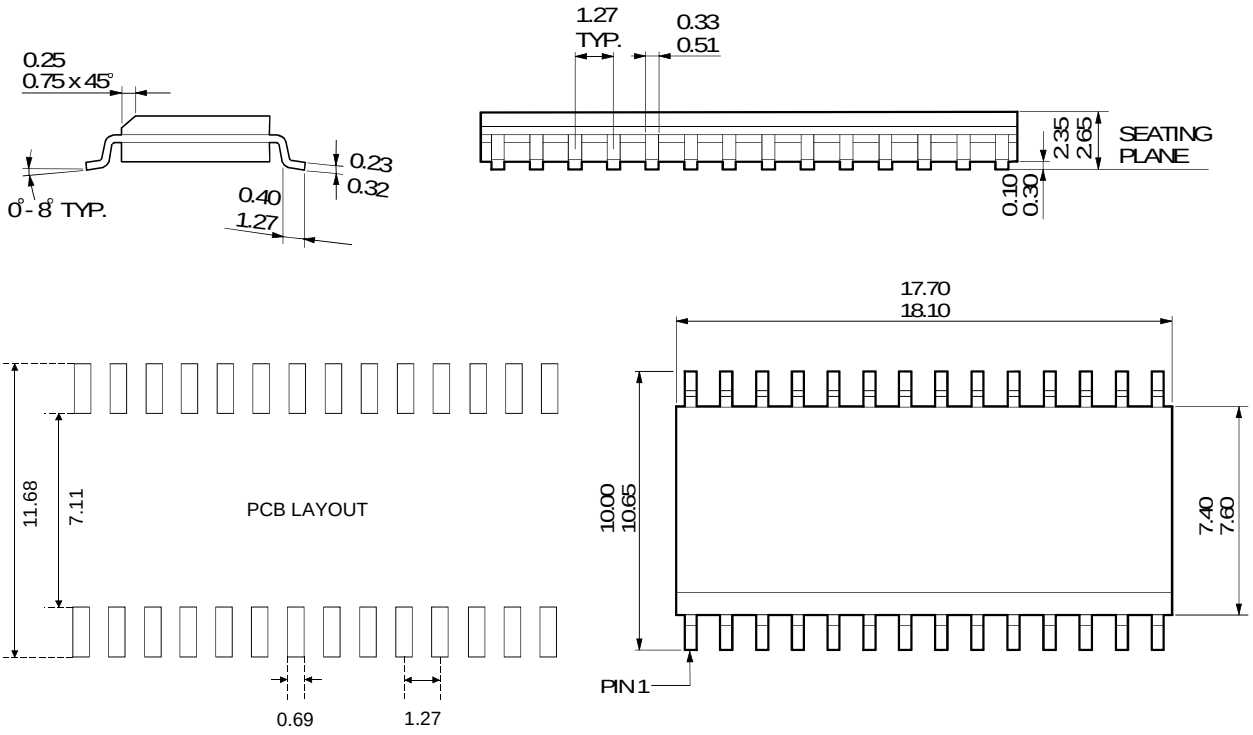


Typical application circuit of MAS9090



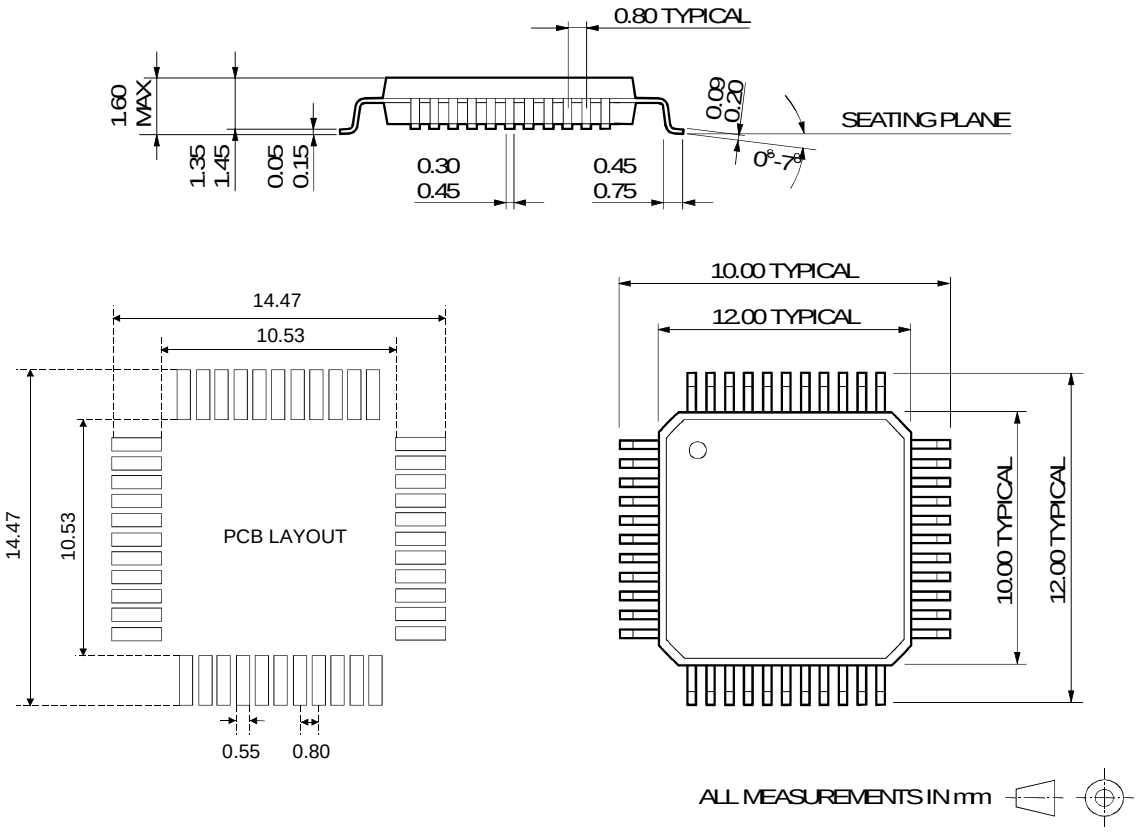
PACKAGE OUTLINES AND RECOMMENDED LAND PATTERNS

28 LEAD SO OUTLINE (300 MIL BODY)



ALL MEASUREMENTS IN mm

44 LEAD TQFP OUTLINE



ALL MEASUREMENTS IN mm

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9090BS	Low Voltage 14-bit Linear Codec	SO28	
MAS9090BS-T	Low Voltage 14-bit Linear Codec	SO28	Tape and Reel
MAS9090BJ	Low Voltage 14-bit Linear Codec	TQFP44	
MAS9090BJ-T	Low Voltage 14-bit Linear Codec	TQFP44	Tape and Reel

LOCAL DISTRIBUTOR

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End of Data Sheet