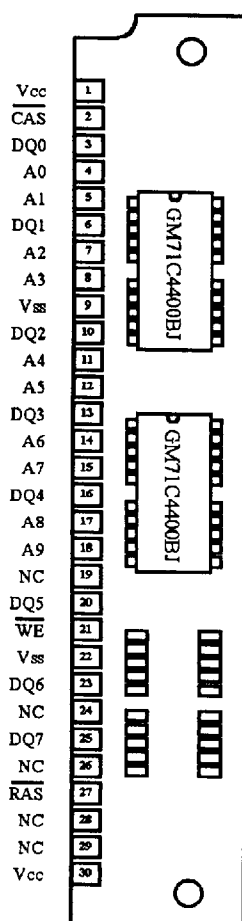


Description

The GMM781100BNS is an 1M x 8 bits Dynamic RAM Module which is assembled 2 pieces of 4M bit DRAM (GM71C4400BJ, 1M x 4) sealed in 20 pin SOJ package. The GMM781100BNS is a socket type memory module, suitable for easy change or addition of module. The GMM781100BNS provides common data inputs and outputs. It's module board has decoupling capacitors mounted for each DRAM.

• GMM781100BNS (Single Side)



Features

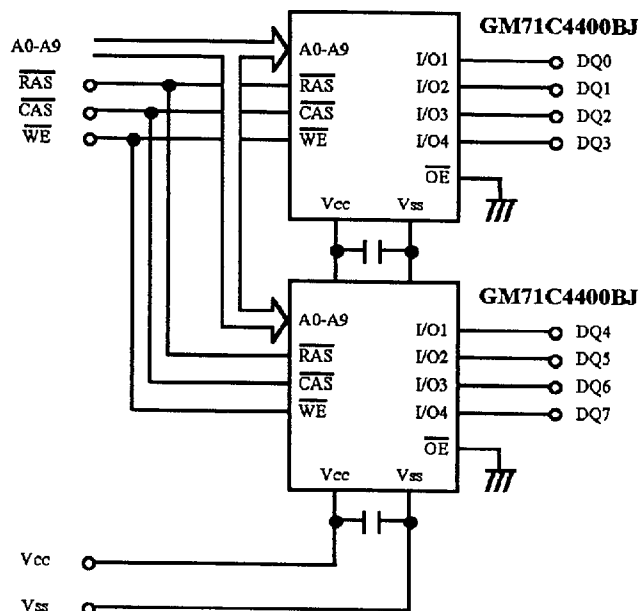
- High Density Standard 30 pin mounting 2 pcs of 4M DRAM GM71C4400BJ (SOJ)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}
GMM781100BNS-60	60	15	110	40
GMM781100BNS-70	70	20	130	45
GMM781100BNS-80	80	20	150	50

- Low Power
Active : 1,210/1,190/990mW (MAX)
Standby : 11mW (CMOS level : MAX)
- RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

Block Diagram



Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	$\overline{WE}$	Read/Write Enable
DQ0-DQ7	Data Input/Output	V _{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V _{SS}	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

*Note: 1. Common $\overline{CAS}$ controls for eight common data-in and data-out lines.
 2. The common controls for one separate pair of data-in and data-out lines.
 3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	°C
T _{STG}	Storage Temperature (Plastic)	-55 ~ 125	°C
V _{IN/VOUT}	Voltage on any Pin Relative to V _{SS}	-1.0 ~ 7.0	V
V _{CC}	Power Supply Voltage	-1.0 ~ 7.0	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	2.0	W

*Note: 1. Stress greater than above "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V _{IH}	Input High Voltage	2.4	-	6.5	V	1
V _{IL}	Input Low Voltage	-1.0	-	0.8	V	1

*Note: 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC \min}$)	60 ns	-	220	mA 1, 2
		70 ns	-	200	
		80 ns	-	180	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} = V_{IH}$)	-	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC \min}$)	60 ns	-	220	mA 2
		70 ns	-	200	
		80 ns	-	180	
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling : $t_{RC} = t_{RC \min}$)	60 ns	-	220	mA 1, 3
		70 ns	-	200	
		80 ns	-	180	
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} \geq V_{CC-0.2V}$)	-	2	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current ($t_{RC} = t_{RC \min}$)	60 ns	-	220	mA
		70 ns	-	200	
		80 ns	-	180	
I_{CC7}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	-	10	mA	1
I_{IL}	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V	-20	20	μA	
I_{OL}	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)	-10	10	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC}(\max)$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$, $f = 1MHz$)

Symbol	Parameter	Min	Max	Unit	Note
C_{in}	Input Capacitance (Address)	-	20	pF	1
C_{in}	Input Capacitance (Clocks)	-	20	pF	1, 2
C_{IO}	Input Capacitance (DQ0~DQ7)	-	17	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable DOUT.

AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ C$, Notes 1, 14)

The GMM781100BNS writes data only in early write cycle ($twcs \geq twcs(min)$).
 Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	GMM781100 BNS-60		GMM781100 BNS-70		GMM781100 BNS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{rCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{rAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
t_{rSH}	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period (1024 Cycles)	-	16	-	16	-	16	ms	

Read Cycle

Symbol	Parameter	GMM781100 BNS-60		GMM781100 BNS-70		GMM781100 BNS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	60	-	70	-	80	ns	2, 3
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	15	-	20	-	20	ns	3, 4
t _{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	3, 5
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	30	-	35	-	40	-	ns	
t _{OFF}	Output Buffer Turn-off Time	0	15	0	20	0	20	ns	6

Write Cycle

Symbol	Parameter	GMM781100 BNS-60		GMM781100 BNS-70		GMM781100 BNS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	10
t _{WCH}	Write Command Hold Time	15	-	15	-	15	-	ns	
t _{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	15	-	20	-	20	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	15	-	20	-	20	-	ns	
t _{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	11
t _{DH}	Data-in Hold Time	15	-	15	-	15	-	ns	11

Refresh Cycle

Symbol	Parameter	GMM781100 BNS-60		GMM781100 BNS-70		GMM781100 BNS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	10	-	10	-	10	-	ns	
t _{CPN}	$\overline{\text{CAS}}$ Precharge Time in Normal Mode	10	-	10	-	10	-	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMM781100 BNS-60		GMM781100 BNS-70		GMM781100 BNS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{PC}	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
t _{CP}	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	10	-	10	-	10	-	ns	
t _{RASC}	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	12
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	35	-	40	-	45	ns	13
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	35	-	40	-	45	-	ns	

Notes:

1. AC measurements assume $t_r = 5\text{ ns}$.
2. Assumes that $t_{\text{rCD}} \leq t_{\text{rCD}}(\text{max})$ and $t_{\text{rAD}} \leq t_{\text{rAD}}(\text{max})$. If t_{rCD} or t_{rAD} is greater than the maximum recommended value shown in this table, t_{rAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{\text{rCD}} \geq t_{\text{rCD}}(\text{max})$ and $t_{\text{rAD}} \leq t_{\text{rAD}}(\text{max})$.
5. Assumes that $t_{\text{rCD}} \leq t_{\text{rCD}}(\text{max})$ and $t_{\text{rAD}} \geq t_{\text{rAD}}(\text{max})$.
6. $t_{\text{OFF}}(\text{max})$ defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
8. Operation with the $t_{\text{rCD}}(\text{max})$ limit insures that $t_{\text{rAC}}(\text{max})$ can be met, $t_{\text{rCD}}(\text{max})$ is specified as a reference point only, if t_{rCD} is greater than the specified $t_{\text{rCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
9. Operation with the $t_{\text{rAD}}(\text{max})$ limit insures that $t_{\text{rAC}}(\text{max})$ can be met, $t_{\text{rAD}}(\text{max})$ is specified as a reference point only, if t_{rAD} is greater than the specified $t_{\text{rAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
12. t_{RASC} is defines $\overline{\text{RAS}}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles are required.

Timing Waveforms

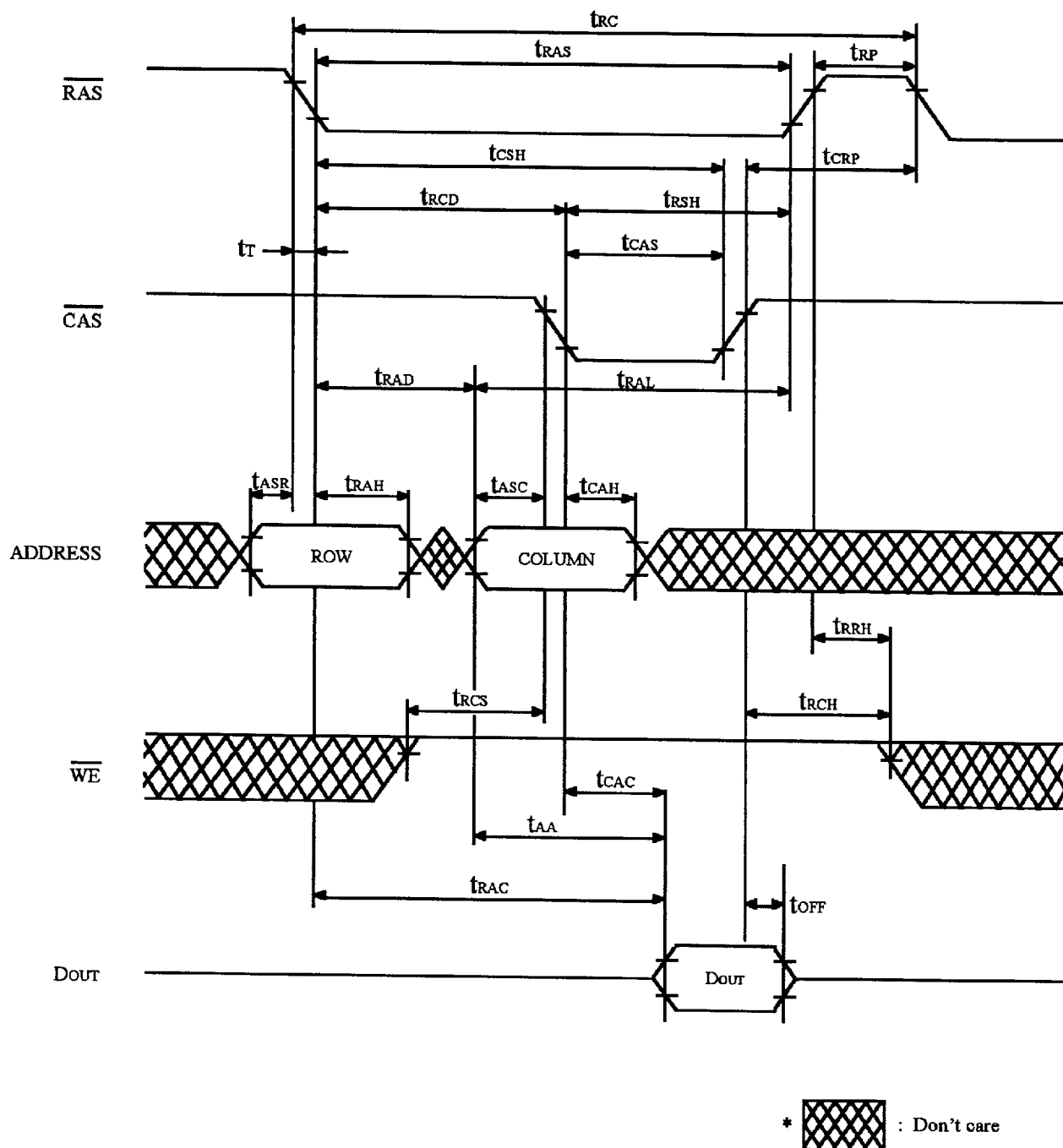
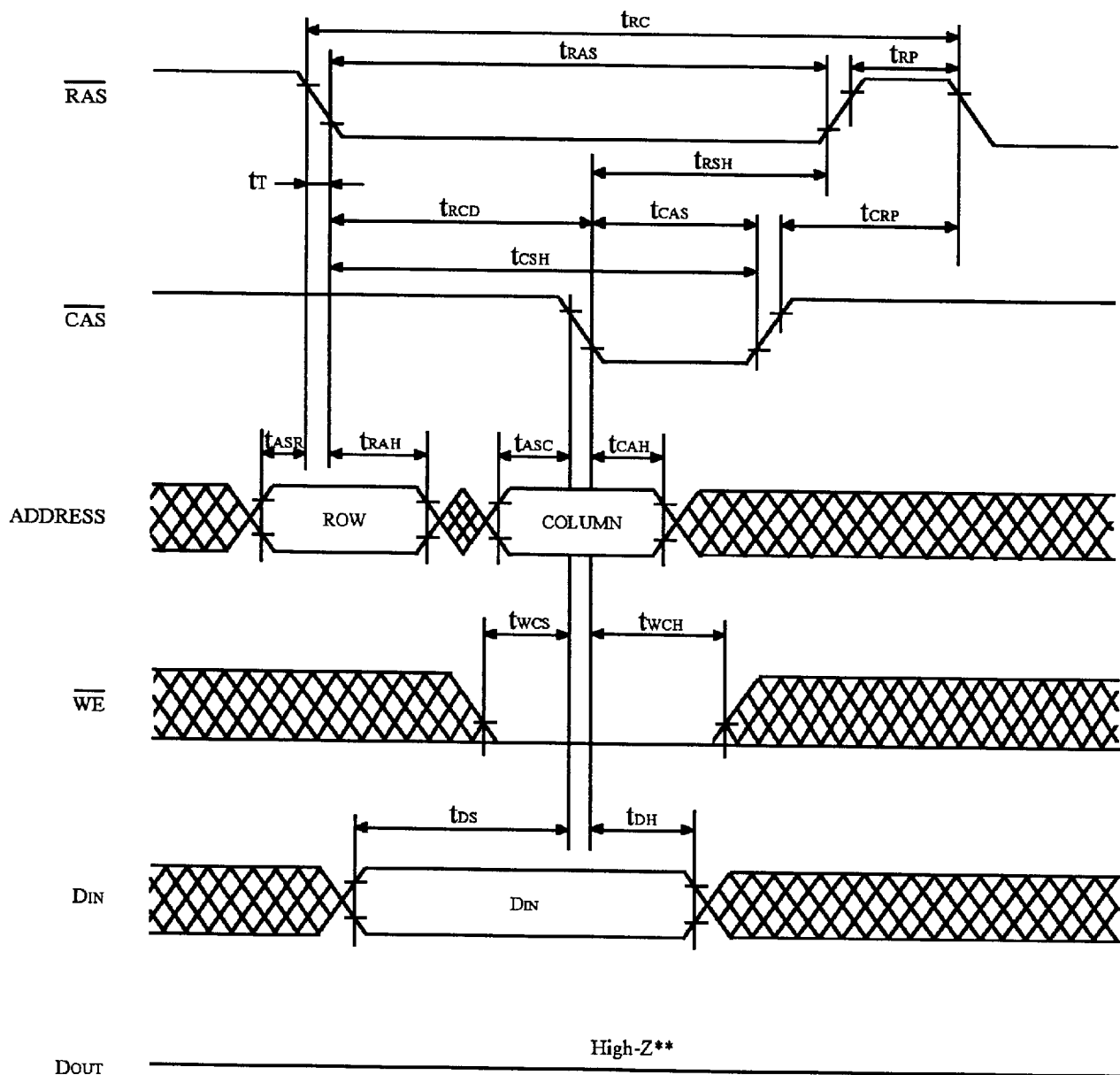


FIGURE 1. READ CYCLE



*  : Don't care

** $t_{WCS} \geq t_{WCS}(\text{min})$

FIGURE 2. EARLY WRITE CYCLE

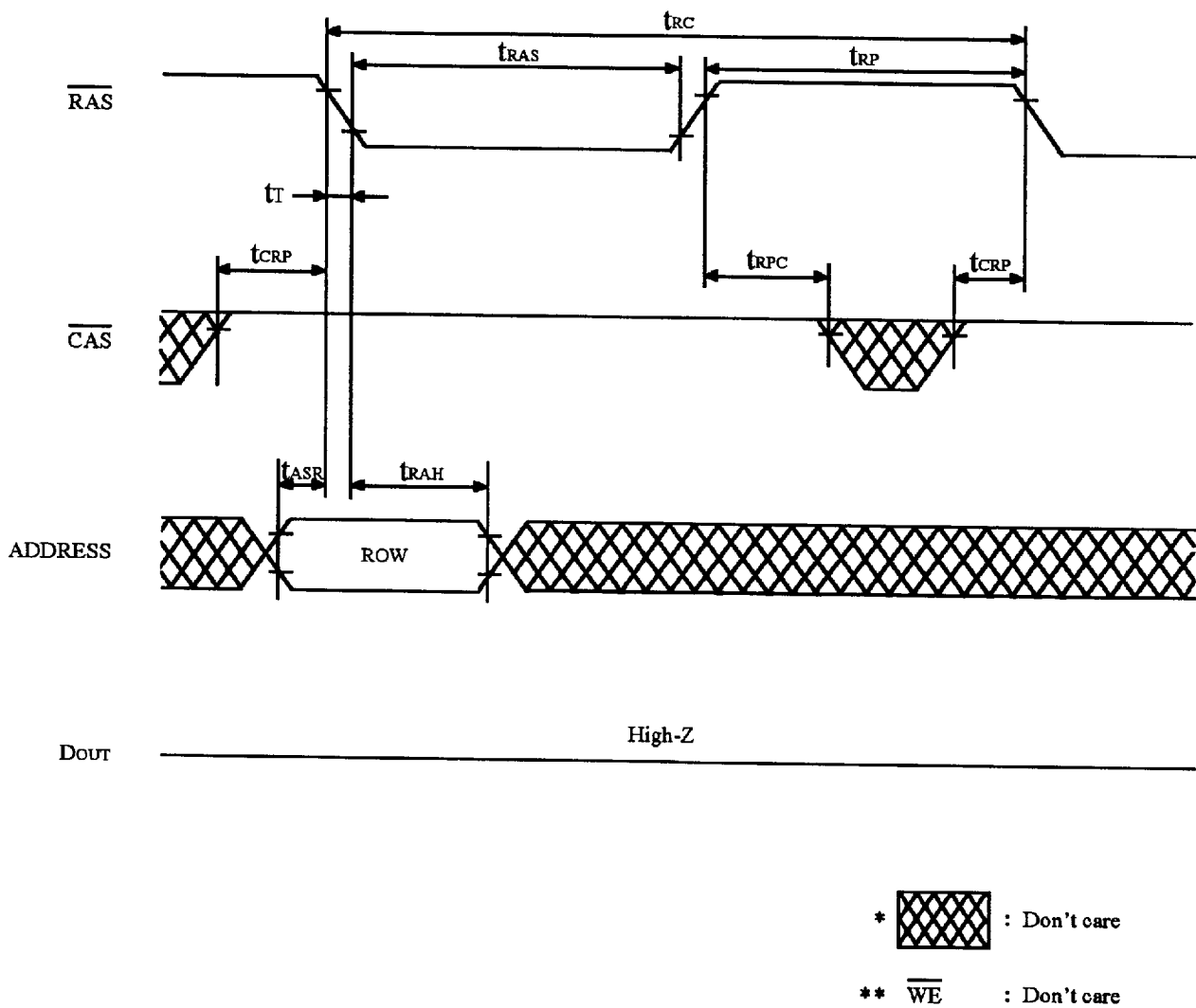
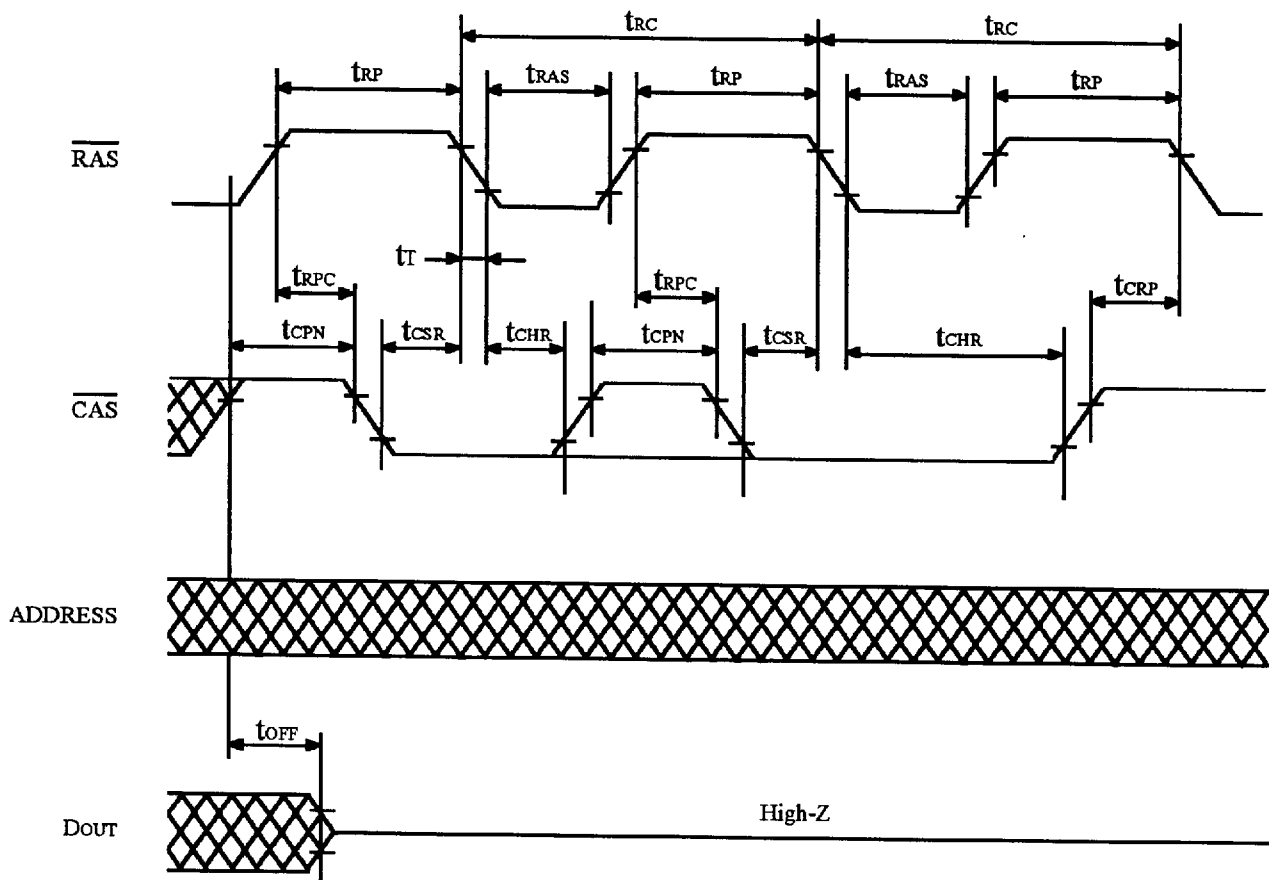


FIGURE 3. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



*  : Don't care

* * $\overline{\text{WE}}$: V_{IH}

FIGURE 4. $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

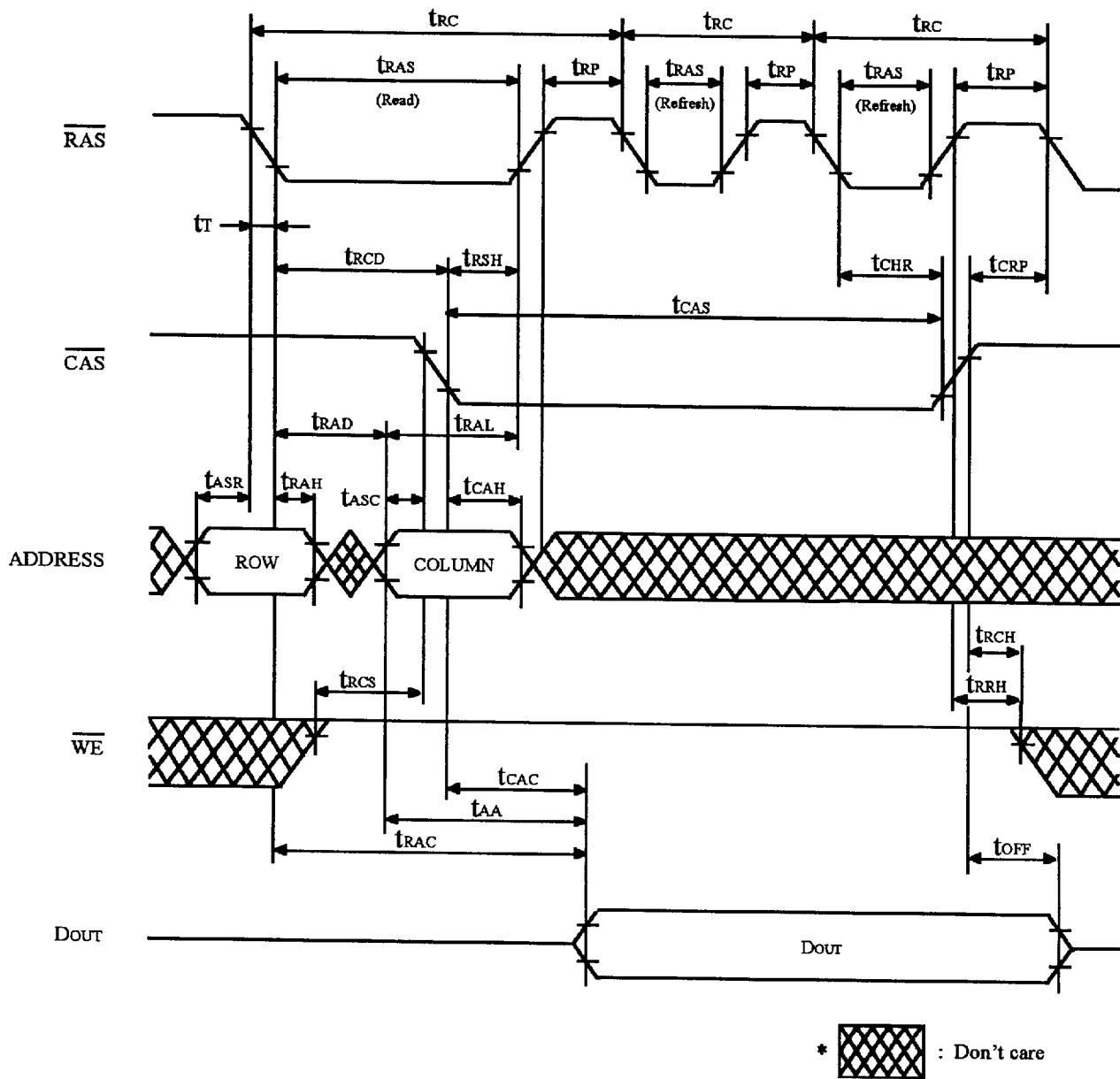


FIGURE 5. HIDDEN REFRESH CYCLE



4028757 0007475 T72

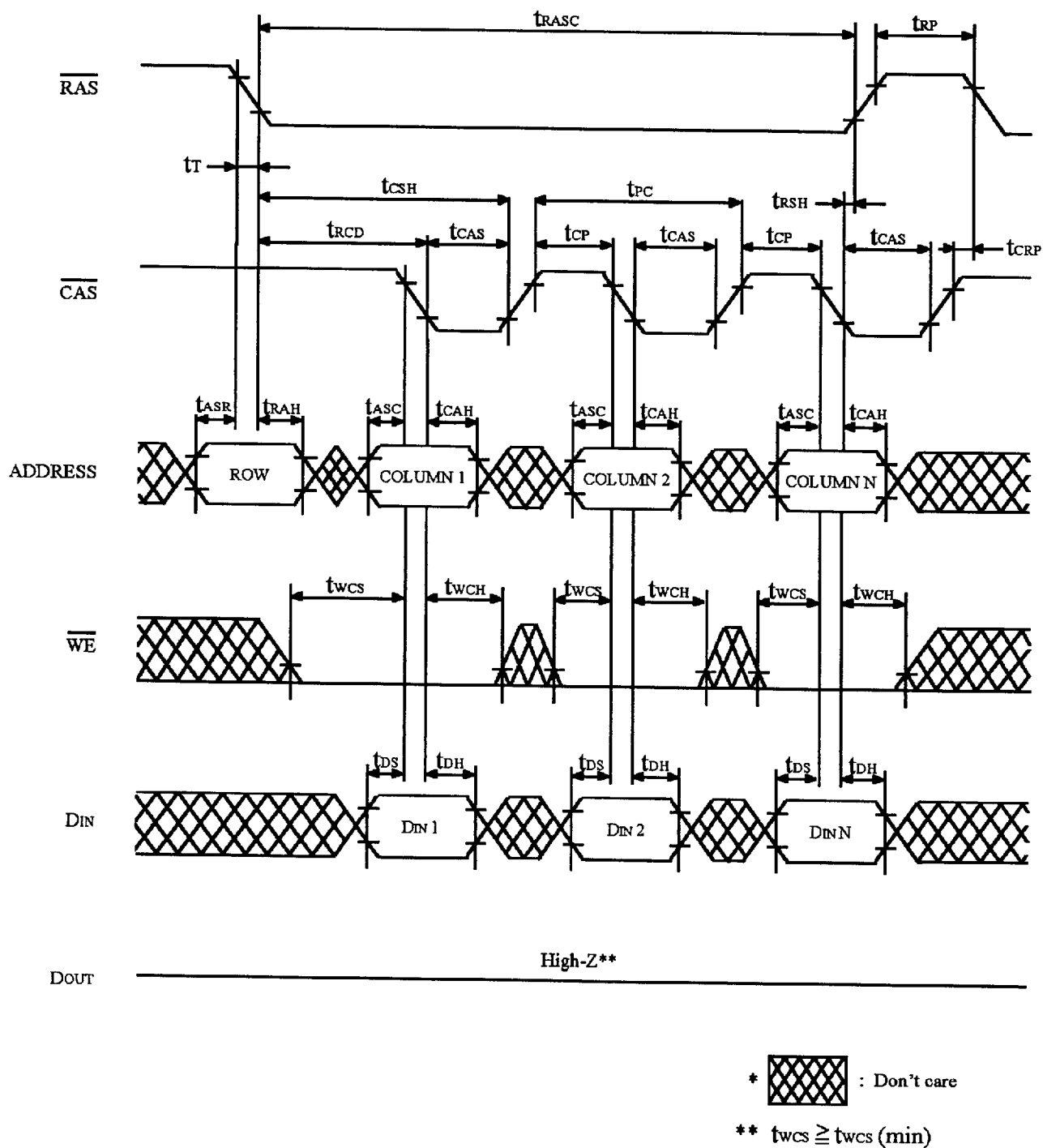


FIGURE 7. FAST PAGE MODE EARLY WRITE CYCLE

