National Semiconductor

DM74AS181B Arithmetic Logic Unit/Function Generator

General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM74AS182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown in Table III illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading AS182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM74AS182.

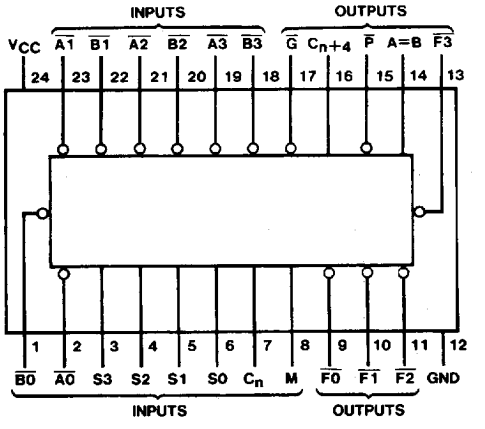
(Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words
- Switching specifications guaranteed over full temperature and V_{CC} range
- Switching specifications at 500Ω/50 pF
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6295–1

Order Number DM74AS181BN, NT
See NS Package Number N24A or N24C

Pin Designations

Designation	Pin Nos.	Function
$\overline{A3}$, $\overline{A2}$, $\overline{A1}$, $\overline{A0}$	19, 21, 23, 2	Word A Inputs
$\overline{B3}$, $\overline{B2}$, $\overline{B1}$, $\overline{B0}$	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F3}$, $\overline{F2}$, $\overline{F1}$, $\overline{F0}$	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
$\overline{P}$	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off-State Output Voltage (A = B only)	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	48.5°C/W
M Package	80.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current	All Outputs Except A = B and $\overline{G}$			−2	mA
		$\overline{G}$			−3	
I_{OL}	Low Level Output Current	All Outputs Except $\overline{G}$			20	mA
		$\overline{G}$			48	
V_{OH}	High Level Output Voltage, (A = B Only)				5.5	V
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA	Any Output Except A = B	V_{CC} − 2			V
		I_{OH} = −3 mA	$\overline{G}$	2.4	3.4		
I_{OH}	High Level Output Current (A = B)	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA	Any Output Except $\overline{G}$		0.3	0.5	V
		I_{OL} = 48 mA	$\overline{G}$		0.4	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_{IH} = 7V	Mode			0.1	mA
			Any A or B			0.3	
			S			0.4	
			Carry			0.6	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7V	Mode Input			20	μA
			Any S Input			80	
			Any A or B Input			60	
			Carry Input			120	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Mode Input			−0.5	mA
			Any S Input			−2	
			Any A or B Input			−1.5	
			Carry Input			−2.5	
I_O (Note 1)	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			70	104	mA

Note 1: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 2)	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_{n+4}	2	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	2	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	2	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	16	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	C_n	Any $\overline{F}$	3	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	2	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	2	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	2	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	2	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (logic mode)	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	2	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any $\overline{A}$ or $\overline{B}$	A = B	4	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				4	21	

Note 1: See Section 5 for test waveforms and output load.

Note 2: V_{CC} = 4.5V to 5.5V, C_L = 50 pF (15 pF for A = B), R_L = 500Ω (280Ω for A = B).

Dynamic Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_n+4	In-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_n+4	Out-of-Phase

Dynamic Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}_i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining A	Remaining B, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_n+4 or any F	In-Phase
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	In-Phase

General Description (Continued)

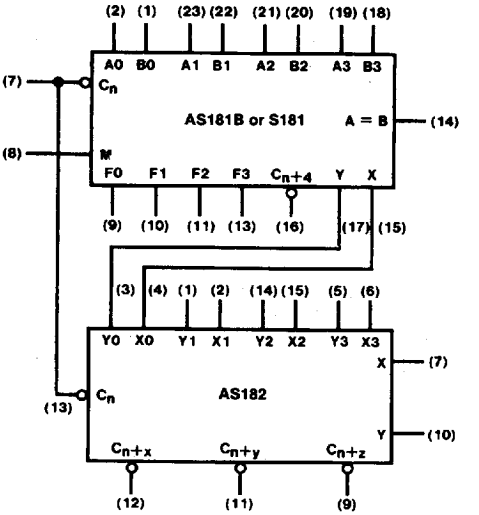


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FIGURE 1

TABLE I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

Input C_n	Output C_n+4	Active-High Data *(Figure 1)*
H	H	A ≤ B
H	L	A > B
L	H	A < B
L	L	A ≥ B

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y

General Description (Continued)

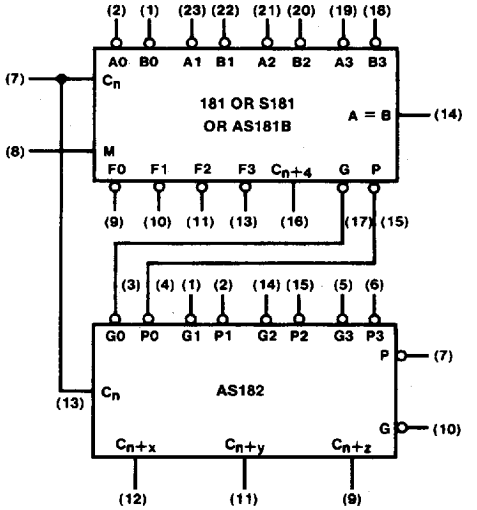

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FIGURE 2

TABLE II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A ⊕ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Input C_n	Output C_n + 4	Active-Low Data *(Figure 2)*
H	H	A ≥ B
H	L	A < B
L	H	A > B
L	L	A ≤ B

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table II)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_n+4	$\overline{P}$	$\overline{G}$

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The AS181B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables I and II and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

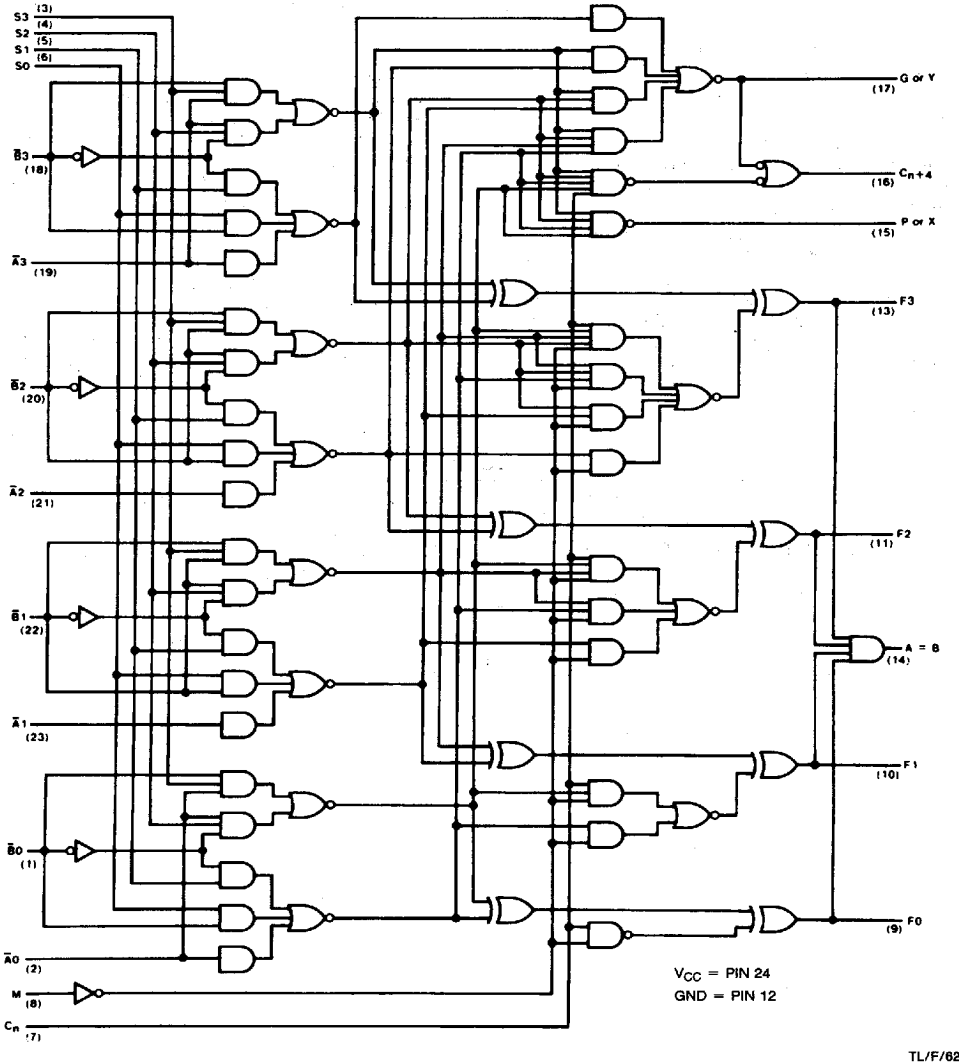
The TTL S181 and AS181B can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

TABLE III

Number of Bits	Typical Addition Times Using AS181B & AS882	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	5 ns	1	0	None
5 to 8	10 ns	2	0	Ripple
9 to 16	14 ns	3 or 4	1	Full Look-Ahead
17 to 64	101 ns	5 to 16	2 to 5	Full Look-Ahead

Logic Diagram



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