SONY CXD1256R

CCD Camera Timing Generator

Description

The CXD1256R is for use with the ICX038, ICX039 CCD image sensors and other signal processing circuits to generate the necessary timing pulses.

Features

- NTSC and PAL compatible
- On-chip electronic shutter
- Built-in defect compensation circuit
- Built-in H-driver
- Compatible with digital and analog camera systems
- Built-in standby function

Applications

CCD cameras

Structure

Silicon-gate CMOS IC

64pin VQFP (Plastic)

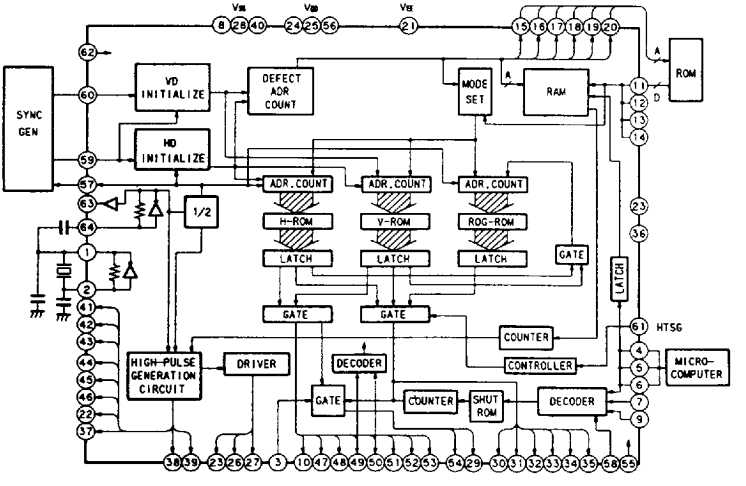
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	$V_{SS}-0.5$ to $+7.0$	V
• Input voltage	V_I	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Supply voltage	V_{EE}	−5 to V_{SS}	V

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	T_{opr}	−20 to +75	°C

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation
2	OSCI	I	Inverter input for oscillation
3	EF	I	Input mode select for defect compensation data (With pull-up resistance.) High: External ROM use Low: Serial input from microcomputer
4	ED0	I	Shutter speed select pin. When set for serial mode, strobe input activated. (With pull-up resistance.)
5	ED1	I	Shutter speed select pin. When set for serial mode, clock input activated. (With pull-up resistance)
6	ED2	I	Shutter speed select pin. When set for serial mode, data input. (With pull-up resistance)
7	SMD1	I	Shutter mode select. (With pull-up resistance)
8	V_{SS}	—	GND
9	SMD2	I	Shutter mode select. (With pull-up resistance)
10	XVCT	O	External ROM power supply control pin.
11	D1	I	When using external ROM, data input pin. (With pull-down resistance). When not using external ROM, Low: No defect compensation; High: Defect compensation enabled.
12	D2	I	When using external ROM, data input (With pull-down resistance). When not using external ROM, this pin is fixed at Low.
13	D3	I	When using external ROM, data input (With pull-down resistance). When not using external ROM , this pin is fixed at Low.
14	D4	I	When using external ROM, data input (With pull-down resistance). When not using external ROM, Low: NTSC; High: PAL.
15	A5	O	External ROM address output.
16	A4	O	External ROM address output.
17	A3	O	External ROM address output.
18	A0	O	External ROM address output.
19	A1	O	External ROM address output.
20	A2	O	External ROM address output.
21	V_{EE}	—	Power supply (−4V) for LH1.
22	RG	O	Reset gate pulse output.
23	LH1	—	CCD horizontal register final-step clock output (9V amplitude output).
24	V_{DD}	—	Power supply.
25	V_{DD}	—	Power supply for H1 and H2.
26	H1	O	Clock output for CCD horizontal register.
27	H2	O	Clock output for CCD horizontal register.
28	V_{SS}	—	GND for H1 and H2.
29	XSUB	O	CCD discharge pulse output.

Pin No.	Symbol	I/O	Description
30	XV2	O	Clock output for CCD vertical register.
31	XV1	O	Clock output for CCD vertical register.
32	XSG1	O	CCD sensor charge Read Out pulse output.
33	XV3	O	Clock output for CCD vertical register.
34	XSG2	O	CCD sensor charge Read Out pulse output.
35	XV4	O	Clock output for CCD vertical register
36	TEST2	I	Input for test use. Set Low in normal operation.
37	CLD	O	4fsc clock output.
38	XSHP	O	Pulse for pre-charge level and sample-and-hold.
39	XSHD	O	Pulse for data sample-and-hold.
40	V_{SS}	—	GND
41	XSP1	O	Color separation sample-and-hold pulse.
42	XSP2	O	Color separation sample-and-hold pulse.
43	XSH1	O	Pulse for sample-and-hold select.
44	XSH2	O	Pulse for sample-and-hold select.
45	XDL1	O	Delay line clock output.
46	XDL2	O	Delay line clock output.
47	BFG	O	Encoder/Chroma Modulator pulse output. When GM is set at High, acts as defect indicator pulse output.
48	CLP1	O	Clamp pulse output.
49	CLP2	IO	Clamp pulse output. When GM is set at High, acts as standby mode switch input.
50	CLP3	IO	Clamp pulse output. When GM is set at High, acts as standby mode switch input.
51	CLP4	O	Clamp pulse output.
52	PBLK	O	Blanking cleaning pulse output.
53	ID	O	Line indicator output.
54	WEN	O	During low-speed shutter operation only, serves as write enable output.
55	GM	I	Low: Analog signal processing; High: Digital signal processing (With pull-down resistance).
56	V_{DD}	—	Power supply.
57	CL	O	4fsc clock output.
58	PS	I	Changeover switch for electronic shutter speed input method. (With pull-up resistance). Low: Serial input; High: Parallel input.
59	HD	I	Horizontal synchronization signal input.
60	VD	I	Vertical synchronization signal input.
61	HTSG	I	Control input for XSG1, XSG2. (With pull-up resistance). Low: XSG1, XSG2 are halted; High: XSG1, XSG2 are generated.
62	TEST	I	Test input. Set at Low during normal operation. (With pull-down resistance.)
63	XCK	O	8fsc clock output.
64	CK	I	8fsc clock input.

Description of Operation

1 Mode Control

Pin	Pin No.	Low	High
GM	55	Analog signal processing	Digital signal processing
PS	58	Serial shutter speed select	Parallel shutter speed select
EF	3	Set at High in normal operation	
HTSG	61	XSG1, 2 OFF	ON
D1	11	Set at Low in normal operation	
D2	12	Set at Low in normal operation	
D3	13	Set at Low in normal operation	
D4	14	NTSC	PAL

2. Digital Signal Processor Compatibility

During digital signal processing operation, when GM is set at High, outputs from XSP1, XSP2, XSH1, XSH2, XDL1, XDL2, CLP2, CLP3 are not essential; thus they are halted. However, depending on the particular system, XSP1, XSP2, XSH1, and XSH2 may be required. By setting Test 2at High, these pins will be output at a fixed timing. Also, using the standby function, the IC's operation can be halted and to stop power consumption without turning off the power.

The CCD clock drivers and signal processing timing pulses are the same as during analog mode operation.

Depending on whether GM is set at High or Low, the functions of certain pins can be changed as shown in the chart below.

Pin	Pin No.	GM=Low (Analog)	GM=High (Digital)
TEST2	36	(Input) Set at Low in normal operation.	(Input) Low: XSP1, XSP2, XSH1, XSH2, XDL1, XDL2 are halted. High: XDL1, XDL2 are halted.
CLP2	49	(Output) Clamping pulse	(Input) Standby control Low: Standby condition High: Normal operation.
CLP3	50	(Output) Clamping pulse	(Input) Standby condition select Low: When in standby, all circuits are halted. High: When in standby, only CL signal is output.
BFG	48	(Output) Burst flag gate pulse.	(Output) Not used in normal operation.

3. Electronic Shutter

The operation of the electronic shutter is controlled by the output of XSUB during particular intervals.

Shutter Mode

SMD1	SMD2	
Low	Low	Flicker-less mode: Removal of fluorescent frequency induced inter-line flickers.
Low	High	High-speed shutter mode: Shutter speed faster than 1/60 (NTSC), 1/50 (PAL).
High	Low	Low-speed shutter mode: Shutter speed slower than 1/60 (NTSC), 1/50 (PAL).
High	High	Shutter operation disabled.

Shutter Mode and Speed Select Method

PS=H: Parallel input: ED0, ED1, ED2, SMD1, SMD2 selected.

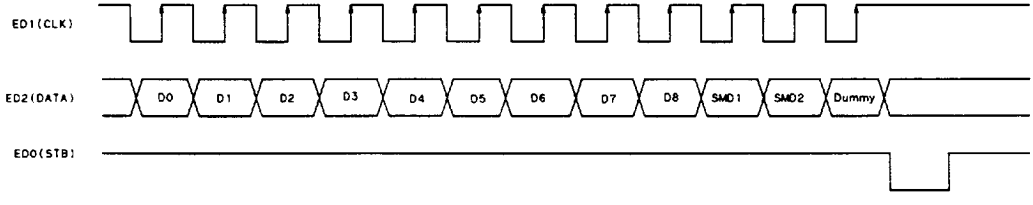
PS=L: Serial input: ED0 (strobe), ED1 (clock), ED2 (data) pins are used for serial input.

3-1. Parallel Input

Shutter Speed Compatibility Chart

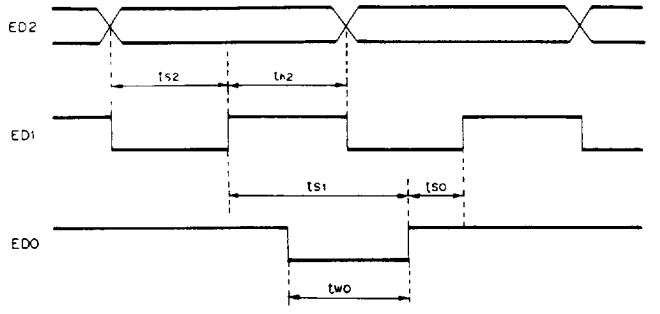
Mode	NTSC/PAL	PS	SMD1	SMD2	ED0	ED1	ED2	Shutter Speed
OFF	X	X	H	H	X	X	X	Shutter Off
Flicker-less	NTSC	X	L	L	X	X	X	1/100 (S)
	PAL	X	L	L	X	X	X	1/120 (S)
High-speed shutter	NTSC	H	L	H	H	H	H	1/60 (S)
	PAL	H	L	H	H	H	H	1/50 (S)
	X	H	L	H	L	H	H	1/125 (S)
	X	H	L	H	H	L	H	1/250 (S)
	X	H	L	H	L	L	H	1/500 (S)
	X	H	L	H	H	H	L	1/1000 (S)
	X	H	L	H	L	H	L	1/2000 (S)
	X	H	L	H	H	L	L	1/4000 (S)
	X	H	L	H	L	L	L	1/10000 (S)
Low-speed shutter	X	H	H	L	H	H	H	2FLD
	X	H	H	L	L	H	H	4FLD
	X	H	H	L	H	L	H	6FLD
	X	H	H	L	L	L	H	8FLD
	X	H	H	L	H	H	L	10FLD
	X	H	H	L	L	H	L	12FLD
	X	H	H	L	H	L	L	14FLD
	X	H	H	L	L	L	L	16FLD

3-2. Serial Input



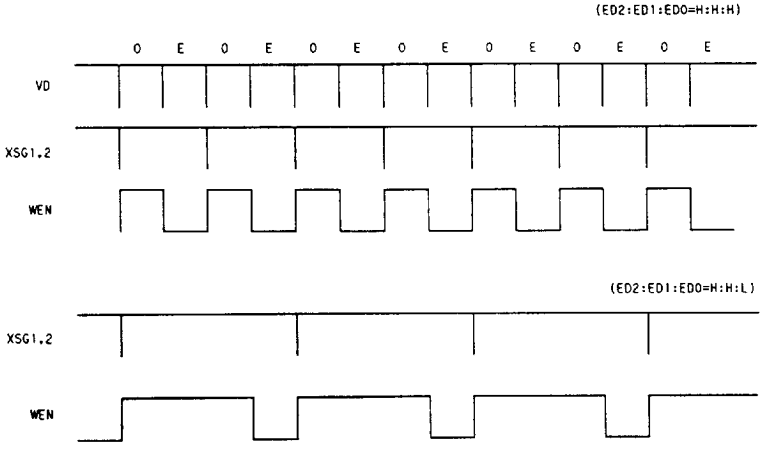
ED2 data is latched to the register at the build up of ED1, and transferred within during the Low peiod of ED0.

AC Characteristics



Symbol		Min.	Max.
t_{S2}	ED2 setup time, activated by the rising edge of ED1.	20ns	—
t_{h2}	ED2 hold time, activated by the rising edge of ED1.	20ns	—
t_{S1}	ED1 rising edge setup time, activated by rising edge of ED0.	20ns	—
t_{WO}	ED0 pulse width.	20ns	50μs
t_{SO}	ED0 raising edge setup time, activated by rising edge of ED1.	20ns	—

3-3. Low-Speed Shutter Timing Chart



3-4. Shutter Speed Calculation Formula

High-speed shutter

• NTSC operation

$T = [262_{10} - (1FF_{16} - L_{16})] \times 63.56 + 34.78\mu s$ ($*L_{16}$ = load value)

• PAL operation

$T = [312_{10} - (1FF_{16} - L_{16})] \times 64 + 35.6\mu s$

NTSC			PAL		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
$0FA_{16}$	1/10000	1/10169	$0C8_{16}$	1/1000	1/10040
$0FC_{16}$	1/4000	1/4435	$0CA_{16}$	1/4000	1/4394
100_{16}	1/2000	1/2085	$0CE_{16}$	1/2000	1/2068
108_{16}	1/1000	1/1012	$0D6_{16}$	1/1000	1/1004
118_{16}	1/500	1/499	$0E6_{16}$	1/500	1/495
137_{16}	1/250	1/252	105_{16}	1/250	1/250
176_{16}	1/125	1/125	143_{16}	1/125	1/125
196_{16}	1/100	1/100	149_{16}	1/120	1/120

Low-speed shutter

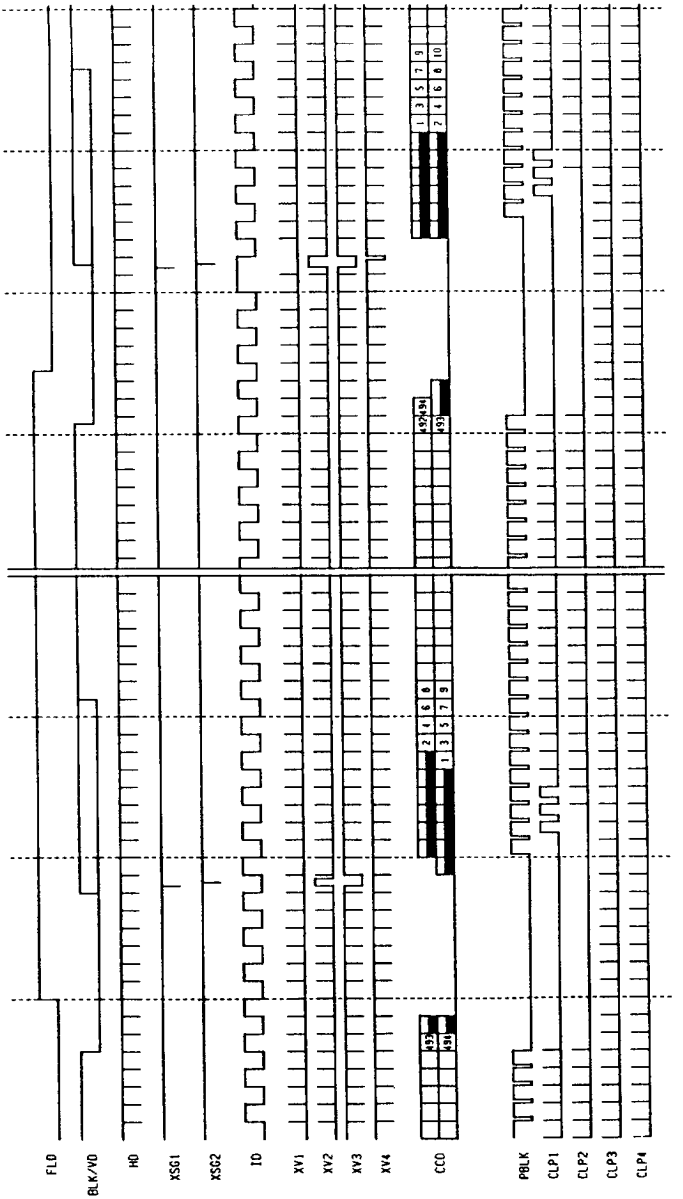
Shutter Speed Calculation Formula

$N = 2 \times (1FF_{16} - L_{16})$ FLD

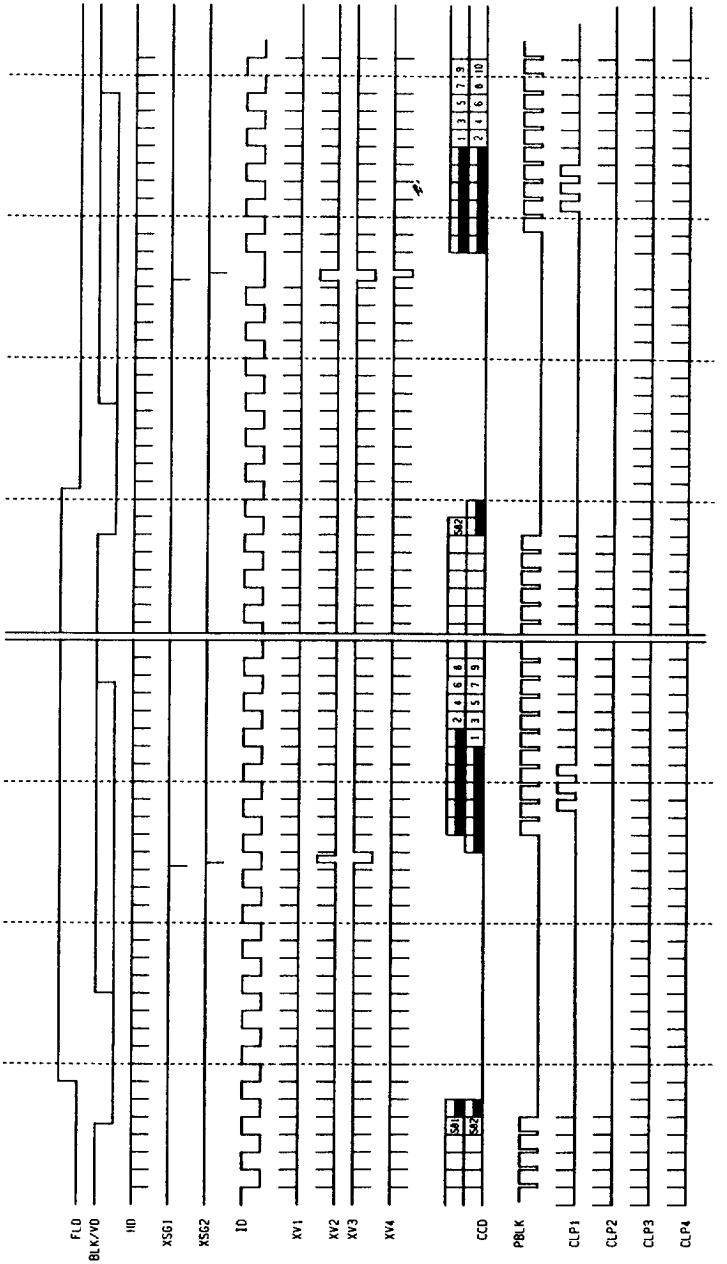
Note that FF cannot be used as load value.

Load value	Shutter speed (FLD)
$1FE_{16}$	2
$1FD_{16}$	4
⋮	⋮
101_{16}	508
100_{16}	510

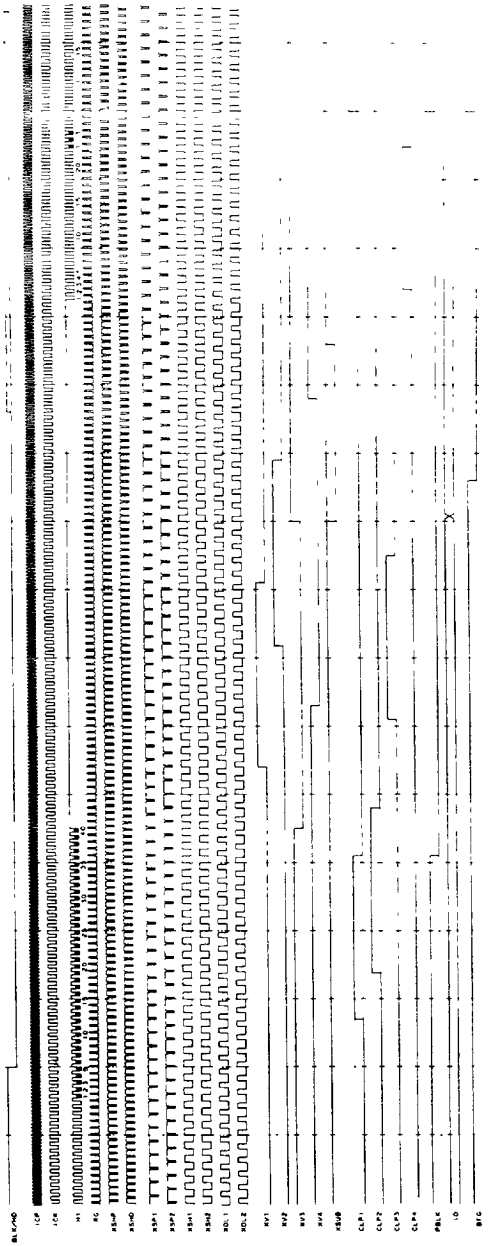
Time Chart (1) 〈NTSC vertical direction〉



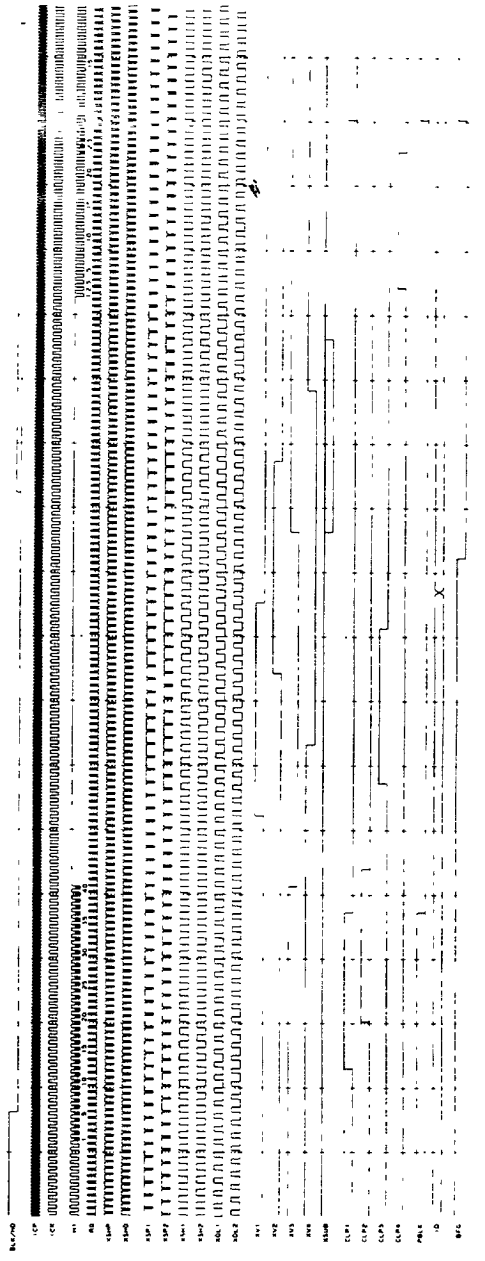
Time Chart (2) 〈PAL vertical direction〉



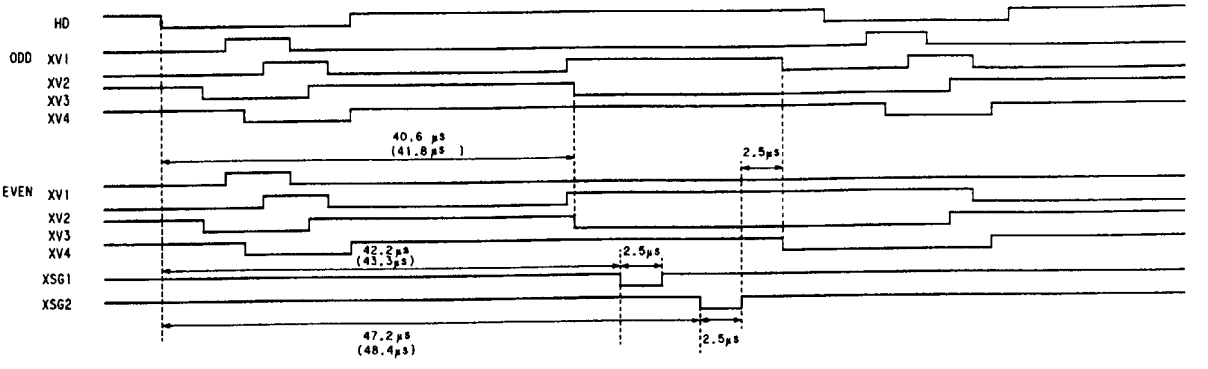
Time Chart (3) 〈NTSC horizontal direction〉



Time Chart (4) 〈PAL horizontal direction〉

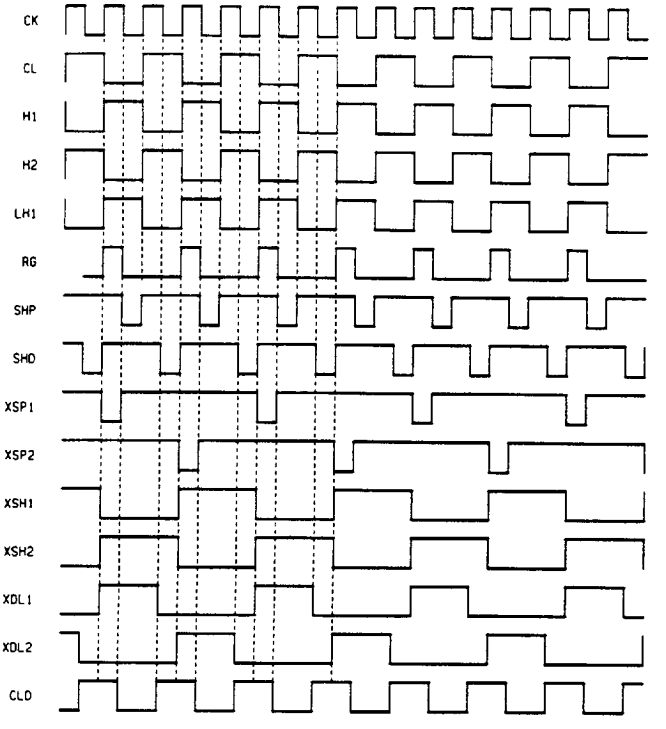


Time Chart (5) 〈XV1 to XV4 modulation〉



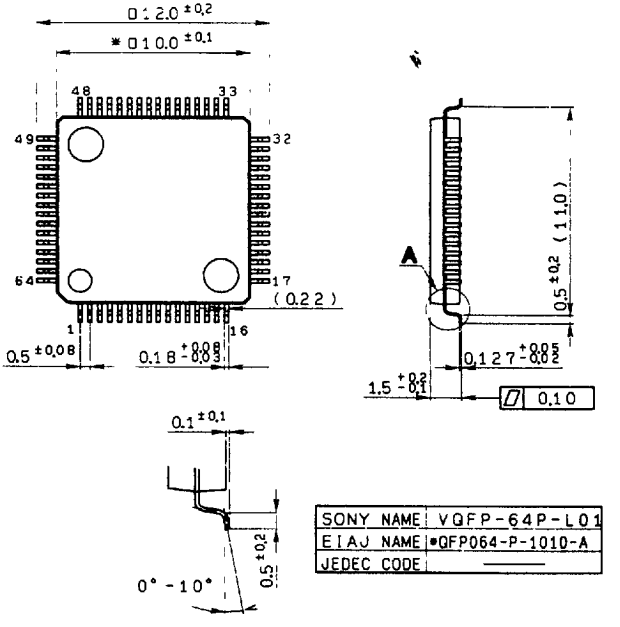
Note) Time at PAL mode is given in parentheses.

Time Chart (6) 〈High speed phase〉



Package Outline **Unit : mm**

64pin VQFP (Plastic) 0.3g



SONY NAME	VQFP-64P-L01
EIAJ NAME	*QFP064-P-1010-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.