

CCD Camera Timing Generator

Description

The CXD1256R is for use with the ICX038, ICX039 CCD image sensors and other signal processing circuits to generate the necessary timing pulses.

Features

- NTSC and PAL compatible
- On-chip electronic shutter
- Built-in defect compensation circuit
- Built-in H-driver
- Compatible with digital and analog camera systems
- Built-in standby function

Applications

CCD cameras

Structure

Silicon-gate CMOS IC

64pin VQFP (Plastic)



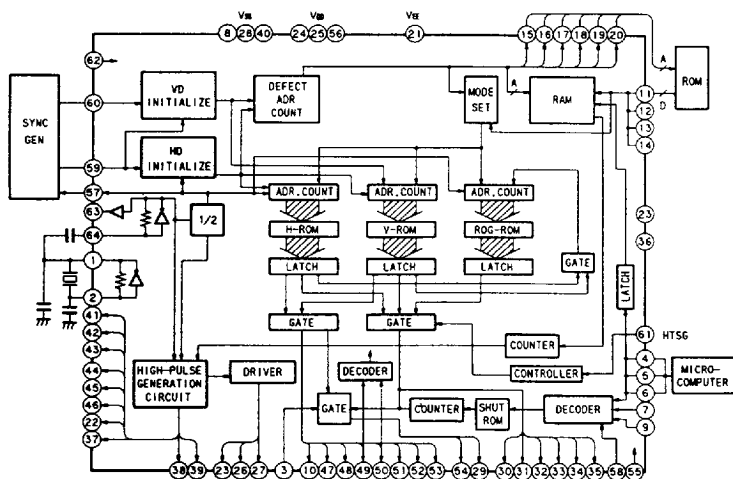
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	$V_{SS} - 0.5$ to $+7.0$	V
• Input voltage	V_i	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
• Output voltage	V_o	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
• Operating temperature	T_{opr}	-20 to $+75$	°C
• Storage temperature	T_{stg}	-55 to $+150$	°C
• Supply voltage	V_{EE}	-5 to V_{SS}	V

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	T_{opr}	-20 to $+75$	°C

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation
2	OSCI	I	Inverter input for oscillation
3	EF	I	Input mode select for defect compensation data (With pull-up resistance.) High: External ROM use Low: Serial input from microcomputer
4	ED0	I	Shutter speed select pin. When set for serial mode, strobe input activated. (With pull-up resistance.)
5	ED1	I	Shutter speed select pin. When set for serial mode, clock input activated. (With pull-up resistance.)
6	ED2	I	Shutter speed select pin. When set for serial mode, data input. (With pull-up resistance.)
7	SMD1	I	Shutter mode select. (With pull-up resistance)
8	V _{SS}	—	GND
9	SMD2	I	Shutter mode select. (With pull-up resistance)
10	XVCT	O	External ROM power supply control pin.
11	D1	I	When using external ROM, data input pin. (With pull-down resistance). When not using external ROM, Low: No defect compensation; High: Defect compensation enabled.
12	D2	I	When using external ROM, data input (With pull-down resistance). When not using external ROM, this pin is fixed at Low.
13	D3	I	When using external ROM, data input (With pull-down resistance). When not using external ROM, this pin is fixed at Low.
14	D4	I	When using external ROM, data input (With pull-down resistance). When not using external ROM, Low: NTSC; High: PAL.
15	A5	O	External ROM address output.
16	A4	O	External ROM address output.
17	A3	O	External ROM address output.
18	A0	O	External ROM address output.
19	A1	O	External ROM address output.
20	A2	O	External ROM address output.
21	V _{EE}	—	Power supply (−4V) for LH1.
22	RG	O	Reset gate pulse output
23	LH1	—	CCD horizontal register final-step clock output (9V amplitude output).
24	V _{DD}	—	Power supply.
25	V _{DD}	—	Power supply for H1 and H2.
26	H1	O	Clock output for CCD horizontal register.
27	H2	O	Clock output for CCD horizontal register.
28	V _{SS}	—	GND for H1 and H2.
29	XSUB	O	CCD discharge pulse output.

Pin No.	Symbol	I/O	Description
30	XV2	O	Clock output for CCD vertical register.
31	XV1	O	Clock output for CCD vertical register.
32	XSG1	O	CCD sensor charge Read Out pulse output.
33	XV3	O	Clock output for CCD vertical register.
34	XSG2	O	CCD sensor charge Read Out pulse output.
35	XV4	O	Clock output for CCD vertical register.
36	TEST2	I	Input for test use. Set Low in normal operation.
37	CLD	O	4fsc clock output.
38	XSHP	O	Pulse for pre-charge level and sample-and-hold.
39	XSHD	O	Pulse for data sample-and-hold.
40	V _{SS}	—	GND
41	XSP1	O	Color separation sample-and-hold pulse.
42	XSP2	O	Color separation sample-and-hold pulse.
43	XSH1	O	Pulse for sample-and-hold select.
44	XSH2	O	Pulse for sample-and-hold select.
45	XDL1	O	Delay line clock output.
46	XDL2	O	Delay line clock output.
47	BFG	O	Encoder/Chroma Modulator pulse output. When GM is set at High, acts as defect indicator pulse output.
48	CLP1	O	Clamp pulse output.
49	CLP2	IO	Clamp pulse output. When GM is set at High, acts as standby mode switch input.
50	CLP3	IO	Clamp pulse output. When GM is set at High, acts as standby mode switch input.
51	CLP4	O	Clamp pulse output.
52	PBLK	O	Blanking cleaning pulse output.
53	ID	O	Line indicator output.
54	WEN	O	During low-speed shutter operation only, serves as write enable output.
55	GM	I	Low: Analog signal processing; High: Digital signal processing (With pull-down resistance).
56	V _{DD}	—	Power supply.
57	CL	O	4fsc clock output.
58	PS	I	Changeover switch for electronic shutter speed input method. (With pull-up resistance). Low: Serial input; High: Parallel input.
59	HD	I	Horizontal synchronization signal input.
60	VD	I	Vertical synchronization signal input.
61	HTSG	I	Control input for XSG1, XSG2. (With pull-up resistance). Low: XSG1, XSG2 are halted; High: XSG1, XSG2 are generated.
62	TEST	I	Test input. Set at Low during normal operation. (With pull-down resistance.)
63	XCK	O	8fsc clock output.
64	CK	I	8fsc clock input.

Description of Operation

1 Mode Control

Pin	Pin No.	Low	High
GM	55	Analog signal processing	Digital signal processing
PS	58	Serial shutter speed select	Parallel shutter speed select
EF	3	Set at High in normal operation	
HTSG	61	XSG1, 2 OFF	ON
D1	11	Set at Low in normal operation	
D2	12	Set at Low in normal operation	
D3	13	Set at Low in normal operation	
D4	14	NTSC	PAL

2. Digital Signal Processor Compatibility

During digital signal processing operation, when GM is set at High, outputs from XSP1, XSP2, XSH1, XSH2, XDL1, XDL2, CLP2, CLP3 are not essential; thus they are halted. However, depending on the particular system, XSP1, XSP2, XSH1, and XSH2 may be required. By setting Test 2 at High, these pins will be output at a fixed timing. Also, using the standby function, the IC's operation can be halted and to stop power consumption without turning off the power.

The CCD clock drivers and signal processing timing pulses are the same as during analog mode operation.

Depending on whether GM is set at High or Low, the functions of certain pins can be changed as shown in the chart below.

Pin	Pin No.	GM=Low (Analog)	GM=High (Digital)
TEST2	36	(Input) Set at Low in normal operation.	(Input) Low: XSP1, XSP2, XSH1, XSH2, XDL1, XDL2 are halted. High: XDL1, XDL2 are halted.
CLP2	49	(Output) Clamping pulse	(Input) Standby control Low: Standby condition High: Normal operation.
CLP3	50	(Output) Clamping pulse	(Input) Standby condition select Low: When in standby, all circuits are halted. High: When in standby, only CL signal is output.
BFG	48	(Output) Burst flag gate pulse.	(Output) Not used in normal operation.

3. Electronic Shutter

The operation of the electronic shutter is controlled by the output of XSUB during particular intervals.

Shutter Mode

SMD1 SMD2

Low	Low	Flicker-less mode: Removal of fluorescent frequency induced inter-line flickers.
Low	High	High-speed shutter mode: Shutter speed faster than 1/60 (NTSC), 1/50 (PAL).
High	Low	Low-speed shutter mode: Shutter speed slower than 1/60 (NTSC), 1/50 (PAL).
High	High	Shutter operation disabled.

Shutter Mode and Speed Select Method

PS=H: Parallel input: ED0, ED1, ED2, SMD1, SMD2 selected.

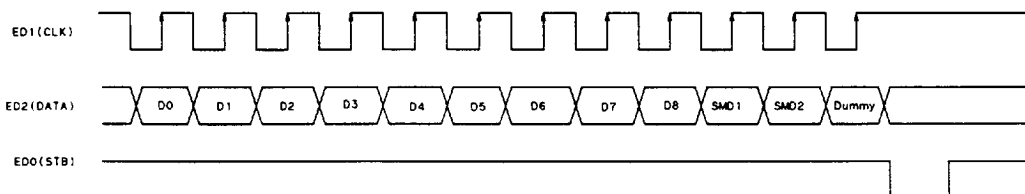
PS=L: Serial input: ED0 (strobe), ED1 (clock), ED2 (data) pins are used for serial input.

3-1. Parallel Input

Shutter Speed Compatibility Chart

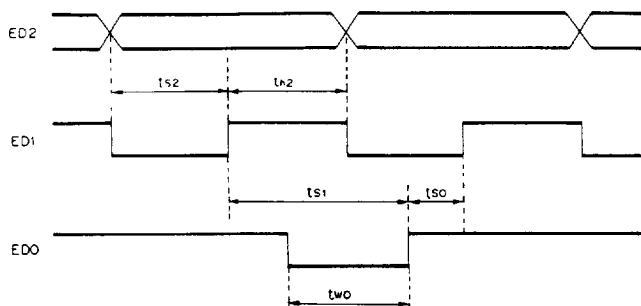
Mode	NTSC/PAL	PS	SMD1	SMD2	ED0	ED1	ED2	Shutter Speed
OFF	X	X	H	H	X	X	X	Shutter Off
Flicker-less	NTSC	X	L	L	X	X	X	1/100 (S)
	PAL	X	L	L	X	X	X	1/120 (S)
High-speed shutter	NTSC	H	L	H	H	H	H	1/60 (S)
	PAL	H	L	H	H	H	H	1/50 (S)
	X	H	L	H	L	H	H	1/125 (S)
	X	H	L	H	H	L	H	1/250 (S)
	X	H	L	H	L	L	H	1/500 (S)
	X	H	L	H	H	H	L	1/1000 (S)
	X	H	L	H	L	H	L	1/2000 (S)
	X	H	L	H	H	L	L	1/4000 (S)
	X	H	L	H	L	L	L	1/10000 (S)
	X	H	H	L	H	H	H	2FLD
Low-speed shutter	X	H	H	L	L	H	H	4FLD
	X	H	H	L	H	L	H	6FLD
	X	H	H	L	L	L	H	8FLD
	X	H	H	L	H	H	L	10FLD
	X	H	H	L	L	H	L	12FLD
	X	H	H	L	H	L	L	14FLD
	X	H	H	L	L	L	L	16FLD

3-2. Serial Input



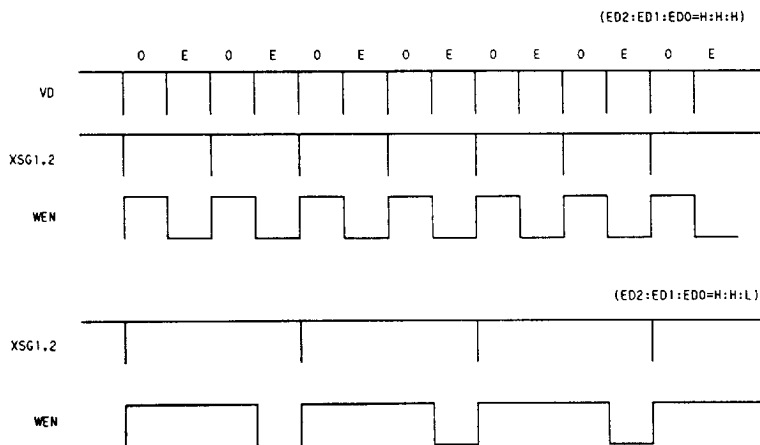
ED2 data is latched to the register at the build up of ED1, and transferred within during the Low period of EDO.

AC Characteristics



Symbol		Min.	Max.
t_{s2}	ED2 setup time, activated by the rising edge of ED1.	20ns	—
t_{h2}	ED2 hold time, activated by the rising edge of ED1.	20ns	—
t_{s1}	ED1 rising edge setup time, activated by rising edge of ED0.	20ns	—
t_{w0}	ED0 pulse width.	20ns	50 μ s
t_{s0}	ED0 raising edge setup time, activated by rising edge of ED1.	20ns	—

3-3. Low-Speed Shutter Timing Chart



3-4. Shutter Speed Calculation Formula

High-speed shutter

• NTSC operation

$$T = [262_{10} - (1FF_{16} - L_{16})] \times 63.56 + 34.78 \mu s \quad (* L_{16} = \text{load value})$$

• PAL operation

$$T = [312_{10} - (1FF_{16} - L_{16})] \times 64 + 35.6 \mu s$$

NTSC			PAL		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
0FA ₁₆	1/10000	1/10169	0C8 ₁₆	1/1000	1/10040
0FC ₁₆	1/4000	1/4435	0CA ₁₆	1/4000	1/4394
100 ₁₆	1/2000	1/2085	0CE ₁₆	1/2000	1/2068
108 ₁₆	1/1000	1/1012	0D6 ₁₆	1/1000	1/1004
118 ₁₆	1/500	1/499	0E6 ₁₆	1/500	1/495
137 ₁₆	1/250	1/252	105 ₁₆	1/250	1/250
176 ₁₆	1/125	1/125	143 ₁₆	1/125	1/125
196 ₁₆	1/100	1/100	149 ₁₆	1/120	1/120

Low-speed shutter

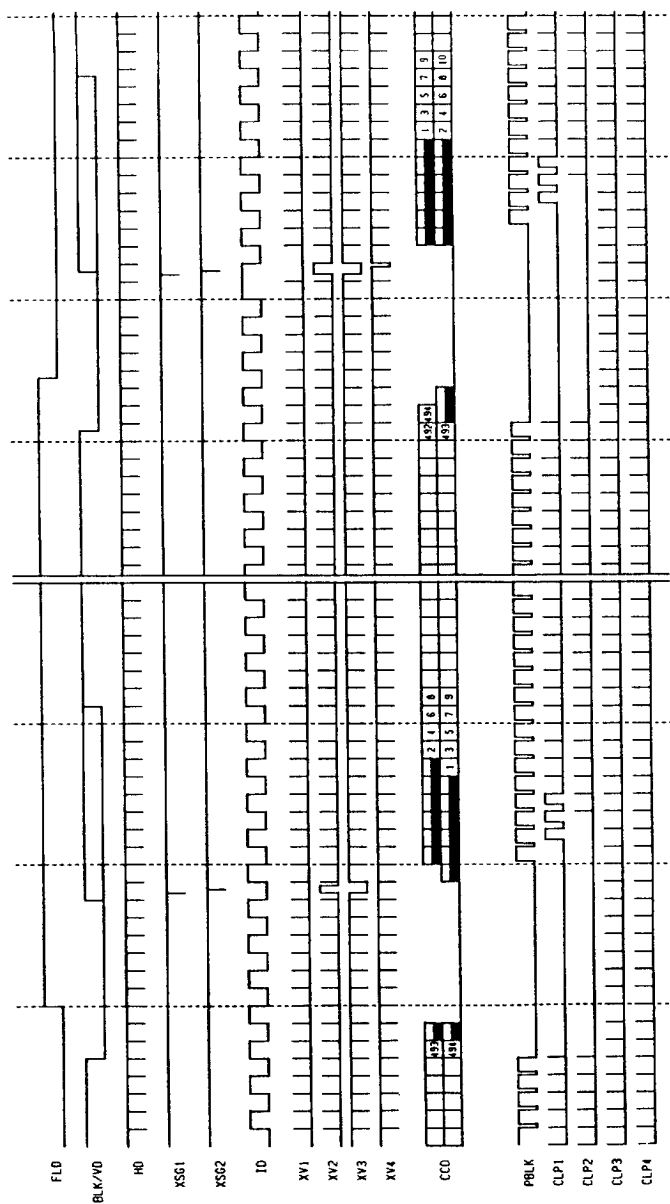
Shutter Speed Calculation Formula

$$N = 2 \times (1FF_{16} - L_{16}) \quad \text{FLD}$$

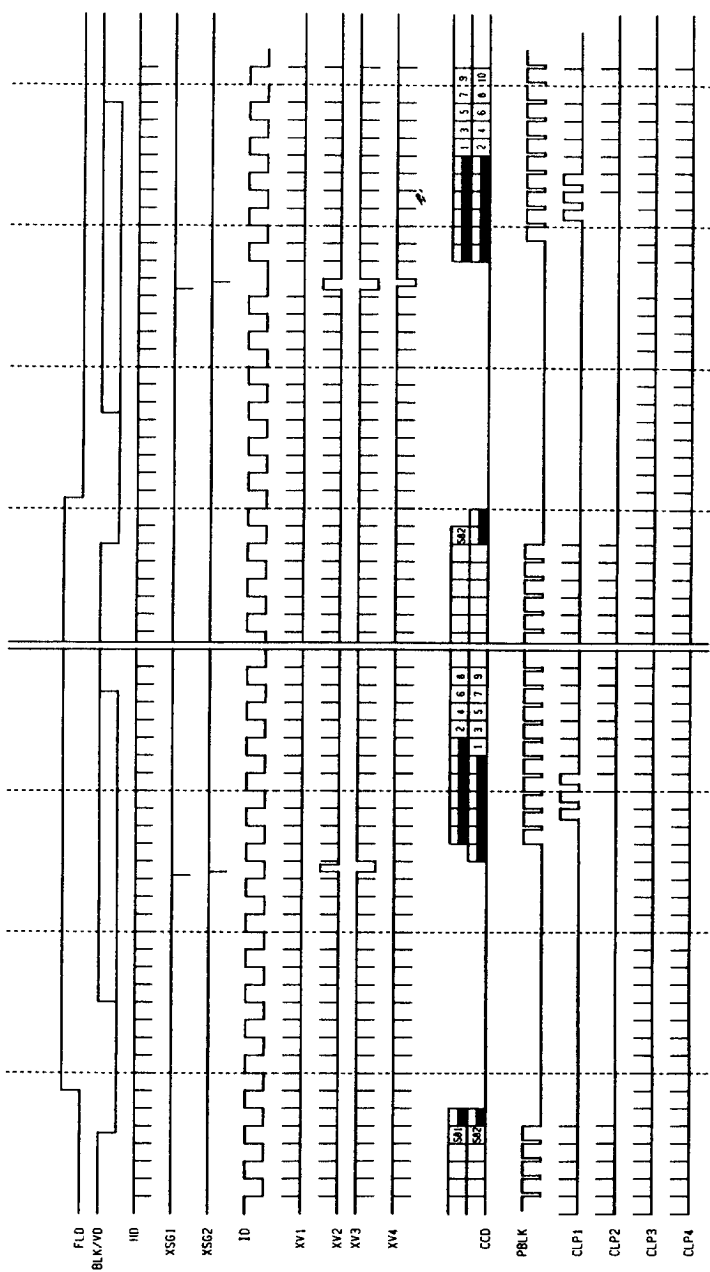
Note that FF cannot be used as load value.

Load value	Shutter speed (FLD)
1FE ₁₆	2
1FD ₁₆	4
⋮	⋮
101 ₁₆	508
100 ₁₆	510

Time Chart (1) <NTSC vertical direction>

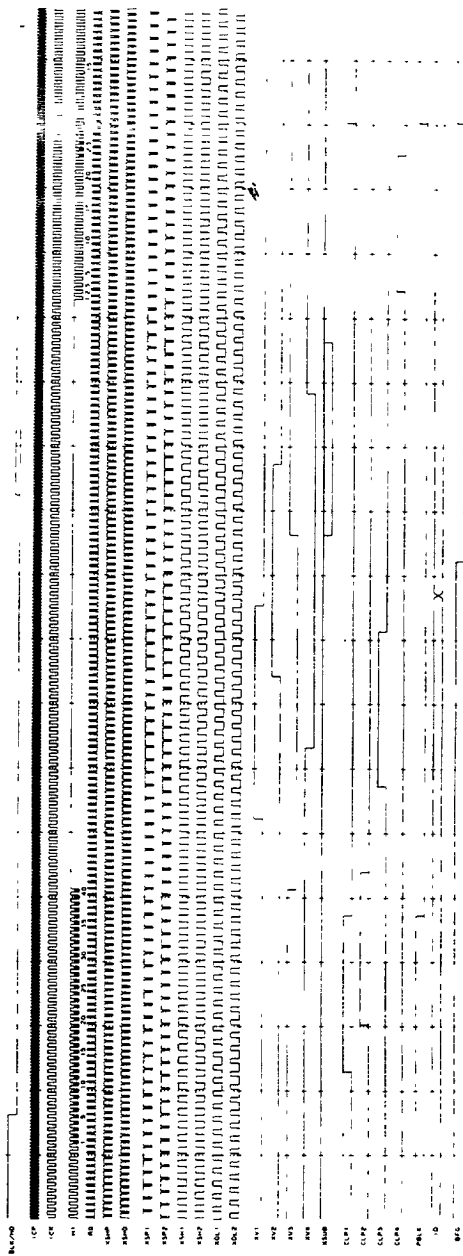


Time Chart (2) <PAL vertical direction>

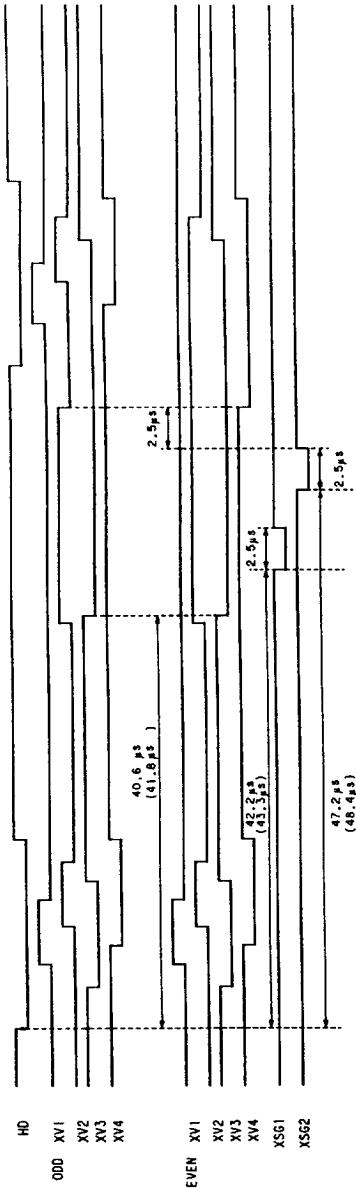


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
84

Time Chart (4) <PAL horizontal direction>

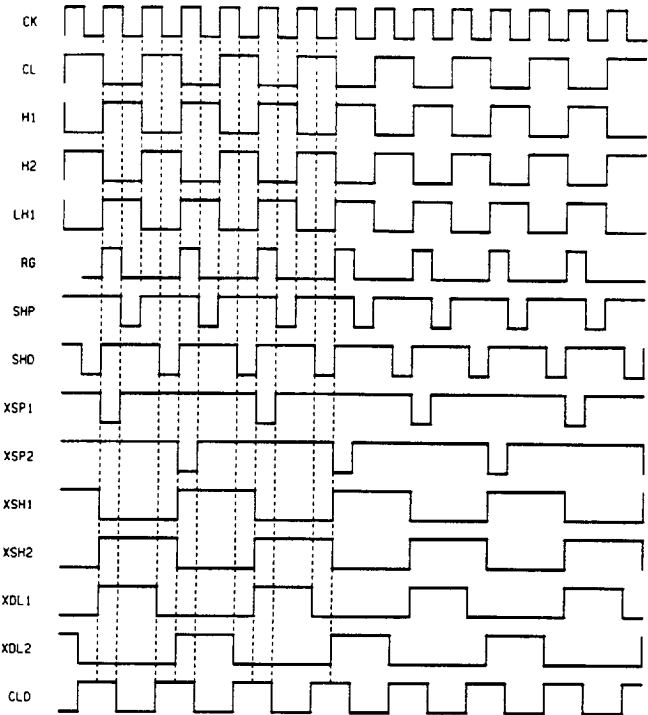


Time Chart (5) <XV1 to XV4 modulation>



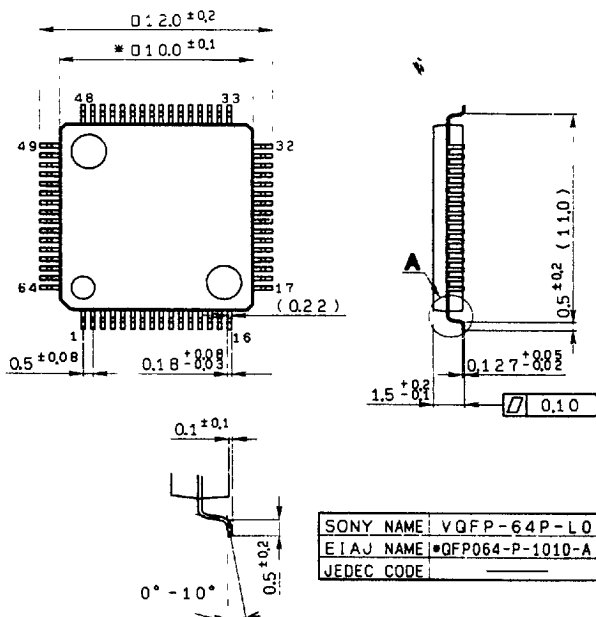
Note) Time at PAL mode is given in parentheses.

Time Chart (6) <High speed phase>



Package Outline Unit: mm

64pin VQFP (Plastic) 0.3g



Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.