SONY

CXB1106Q/Q-Y

T-45-19-05

4-bit Ripple Down Counter with Enable and Reset

Description

The CXB1106Q is an ECL ultra high speed monolithic Binary Ripple Down Counter with divide-by-2/4/8/16 outputs.

Clock input has differential input pins C and $\overline{C}$. Built-in reference voltage V_{BB} is provided to facilitate the use of single clock input. Enable input ($\overline{E}$) enables clock input. Common direct reset input (R) resets the counter and separate Set inputs (Sn) set each stage of the counter.

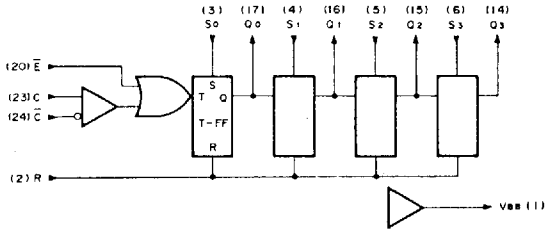
Features

- Typical clock rate up to 3.0GHz
- Differential Clock input (positive edge trigger)
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

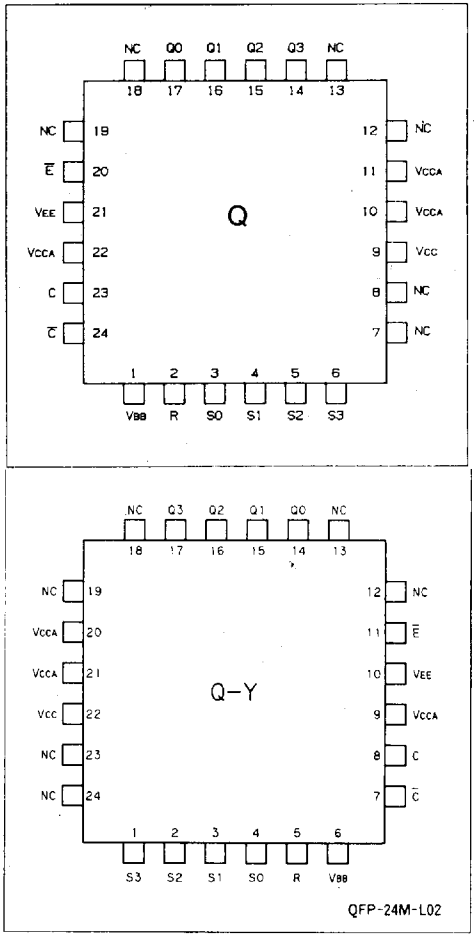
Pin Names

C, $\overline{C}$	Clock inputs
Qn	Data outputs
Sn	Direct set inputs
R	Common direct Reset input
$\overline{E}$	Clock enable (active LOW)
V_{BB}	Reference voltage output
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment



T-45-19-05

Sequencial Truth Table

Inputs							Outputs			
R	$\overline{E}$	S0	S1	S2	S3	C	Q0	Q1	Q2	Q3
H	×	L	L	L	L	×	L	L	L	L
H	H	L	L	L	L	×	L	L	L	L
L	H	L	L	L	L	×	L	L	L	L
L	L	L	L	L	L	∫	H	H	H	H
L	L	L	L	L	L	∫	L	H	H	H
L	L	L	L	L	L	∫	H	L	H	H
L	L	L	L	L	L	∫	L	L	H	H
L	L	L	L	L	L	∫	H	H	L	H
L	L	L	L	L	L	∫	L	H	L	H
L	L	L	L	L	L	∫	H	L	L	H
L	L	L	L	L	L	∫	L	L	L	H
L	L	L	L	L	L	∫	H	H	H	L
L	L	L	L	L	L	∫	L	H	H	L
L	L	L	L	L	L	∫	H	L	H	L
L	L	L	L	L	L	∫	L	L	H	L
L	L	L	L	L	L	∫	H	H	L	L
L	L	L	L	L	L	∫	L	H	L	L
L	L	L	L	L	L	∫	H	L	L	L
L	L	L	L	L	L	∫	L	L	L	L
L	×	L	L	H	H	×	L	L	H	H
L	×	L	H	L	H	×	L	H	H	H
L	∫	L	L	L	L	L	H	L	H	H
L	∫	L	L	L	L	L	L	L	H	H
H	×	H	H	H	H	×	×	×	×	×

Note: H; HIGH voltage level
L; LOW voltage level
X; Don't care

T-45-19-05

DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−202	−148	−103	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	C, $\overline{E}$	Q0		540	870	1100	ps
	T_{PHL}				550	880	1110	
	T_{PLH}		Q1		710	1040	1270	
	T_{PHL}				720	1050	1280	
	T_{PLH}		Q2		830	1160	1390	
	T_{PHL}				840	1170	1400	
	T_{PLH}		Q3		1140	1470	1700	
	T_{PHL}				1150	1480	1710	
	T_{PLH}	Sn	Qn		560	810	1130	
	T_{PHL}	R			640	890	1180	
Release time	T_R	S0, C	Q0		160			
		S1, C	Q1		−20			
		S2, C	Q2		−230			
		S3, C	Q3		−450			
		R, C	Q0		430			
		$\overline{E}$, C			170			
Min. Pulse width	T_{PW}	Sn	Qn		330			
		R			390			
Max. Clock frequency	f_{MAX}	C	Qn		2.4	3.0		GHz
Rise time	T_{TLH}			20% to 80%		270	320	ps
Fall time	T_{THL}					220	270	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

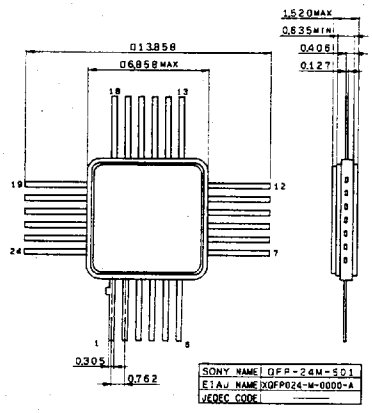
Package Data

T-90-20

Package Outline Uuit: mm

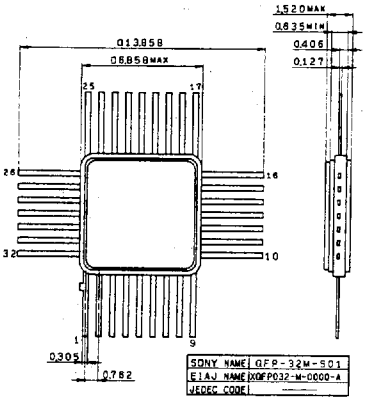
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



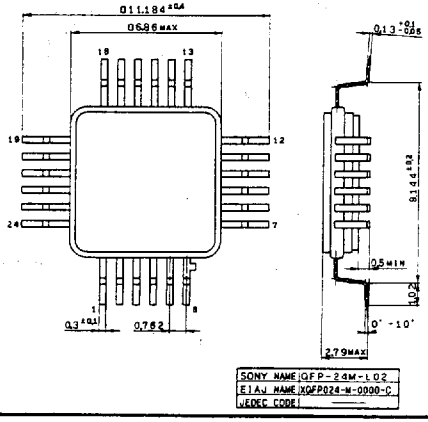
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



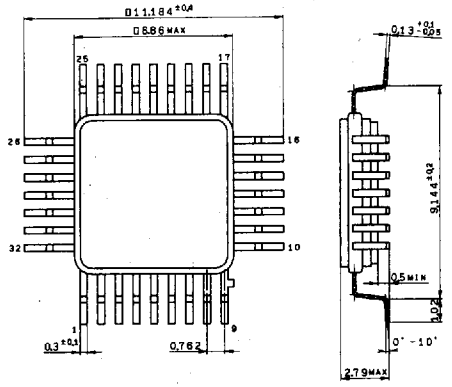
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

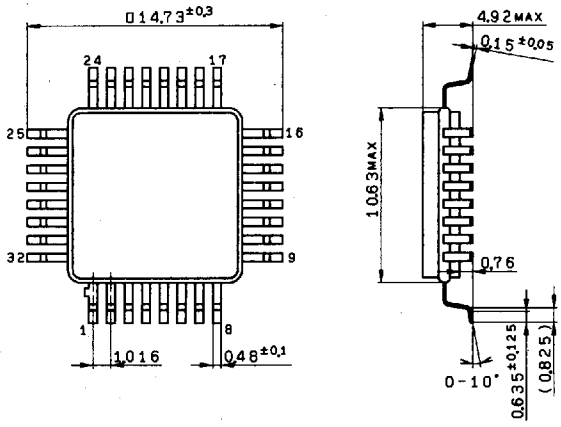
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

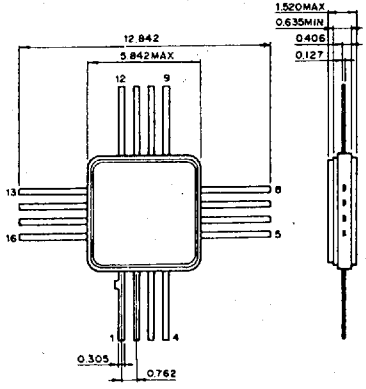
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

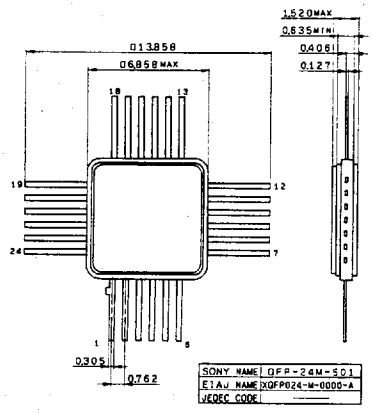
Package Data

T-90-20

Package Outline Uuit: mm

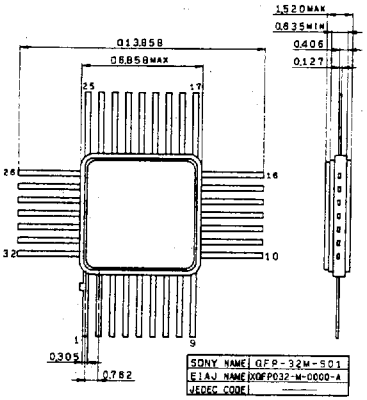
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



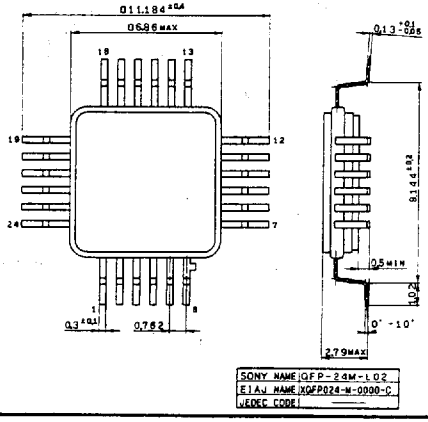
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



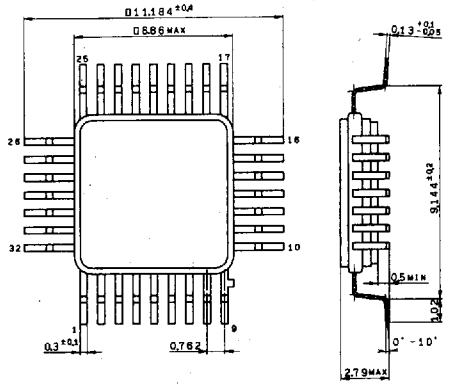
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

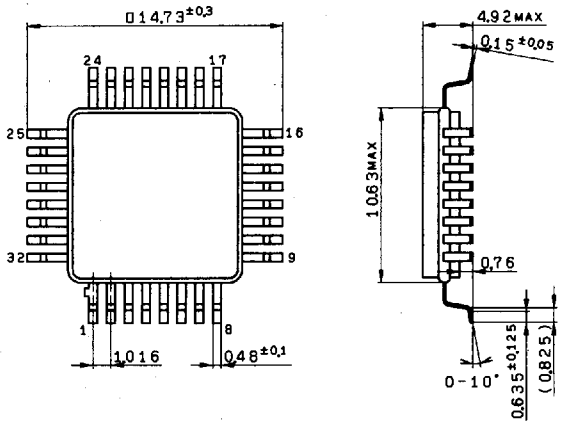
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP