MOTOROLA

1:9 Differential Clock Driver

Product Preview

ELECTRICALLY TESTED PER:
100E511

Military 100E511

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: F

The 100E511 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

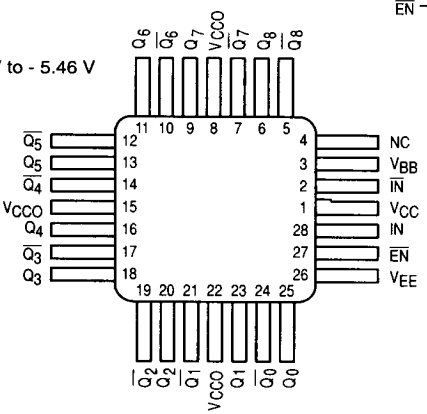
To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i. e. sharing the same V_{CCO}) as the pairs(s) being used on the same side, in order to maintain minimum skew. Failure to do this will result in small degradation of propagation delay (on the order of 10-20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

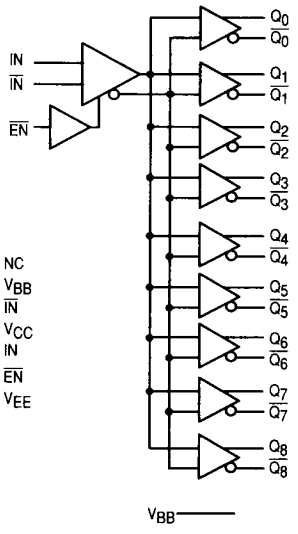
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- V_{BB} output
- Enable
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
En	Enable
Q_0, $\overline{Q_0}$ - Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Outputs



LOGIC DIAGRAM



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	V	V_{IL} = Open, V_{IH} = Open, R_L = 50Ω to − 2.0 V.
I_{IH}	Input Current High		150		150		150	μA	V_{IL} = − 1.810 V, V_{IH} = − 0.880 V, R_L = 50Ω to − 2.0 V.
I_{EE}	Power Supply Current		60		69		60	mA	V_{EE} (MAX), V_{IL} = − 1.810 V, V_{IH} = − 0.880 V, R_L = 50Ω to − 2.0 V.

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay to Output								
t_{PHL}	IN (Differential)	430	630	430	630	430	630	ps	(Note 1)
	IN (Single-ended)	330	730	330	730	330	730	ps	(Note 2)
	Enable	450	850	450	850	450	850	ps	(Note 3)
	Disable	450	850	450	850	450	850	ps	(Note 3)
t_{Skew}	Within-Device Skew		50		50		50	ps	(Note 4)
t_S	Setup Time $\overline{En}$ to IN	200		200		200		ps	(Note 5)
t_H	Hold Time IN to $\overline{En}$	0		0		0		ps	(Note 6)
t_R	Release Time $\overline{En}$ to IN	300		300		300		ps	(Note 7)
V_{PP}	Minimum Input Swing	250		250		250		mV	(Note 8)
V_{CMR}	Common Mode Range	-1.6	-0.4	-1.6	-0.4	-1.6	-0.4	V	(Note 9)
t_r t_f	Rise/Fall Times 20 - 80%	275	600	275	600	275	600	ps	

See Notes on the following page.

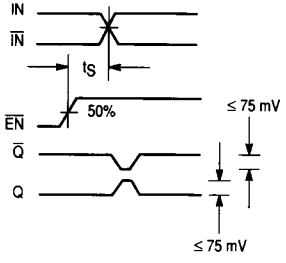

Figure 1. Setup Time

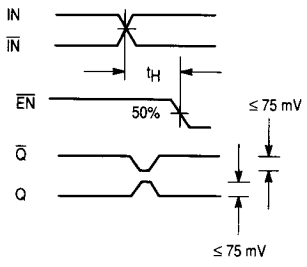

Figure 2. Hold Time

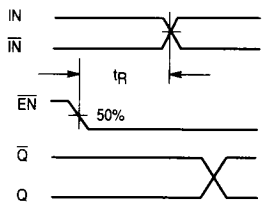

Figure 3. Release Time

Notes

1. The differential propagation is defined as the delay from the crossing points of the differential input signals to the crossing point of differential output signals. (See *Definitions and testing ECLinPS AC Parameters* in Section 1.)
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. (See *Definitions and testing ECLinPS AC Parameters* in Section 1.)
3. Enable is defined as the propagation delay from 50% point of the **negative** transition $\overline{EN}$ to the 50% point of the **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from 50% point of the **positive** transition on $\overline{EN}$ to the 50% point of the **negative** transition on Q (or a negative transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ± 75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ± 75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP} (min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min) is AC limited for the E511, a differential input as low as 50 mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP} (min). Measured output voltages must fall within the specified limits of V_{OH} and V_{OL} (V_{OH} = - 0.880 V max, - 1.090 V min, V_{OL} = - 1.580 V max, - 1.810 V min).

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