SIEMENS

ICs for Communications

High Voltage Subscriber Line IC
HV-SLIC

PEB/F 4065 Version 3.0

Data Sheet 03.98
DS 1

PEB/F 4065		
Revision History:		**Current Version: 03.98**
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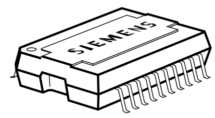
PEB/F 4065

Version 1.1 **SPT**

1 Overview



P-DSO-20-5

The High Voltage Subscriber Line IC PEB 4065 is a rugged and reliable interface between the telephone line and the SLICOFI, a low voltage Subscriber Line Interface and Codec Filter IC. It is fabricated in a Smart Power Technology offering a breakthrough voltage of at least 170 V.

The PEB 4065 provides battery feeding between – 24 V and – 80 V and internal ringing injection with a differential ring voltage up to 85 Vrms. In order to achieve these high amplitudes an auxiliary positive battery voltage is used during ringing. This voltage can also be applied in order to drive very long telephone lines.

The SLIC is designed for a voltage feeding – current sensing line interface concept and provides sensing of transversal and longitudinal current on both wires.

A power-down mode offers reduced power consumption at full functionality; in the power denial mode the device is switched off turning the line outputs to a high impedance state.

1.1 Features

- High voltage line feeding
- Internal ring and metering signal injection
- Sensing of transversal and longitudinal line current
- Reliable 170 V Smart Power Technology
- Battery voltage – 24 V … – 80 V
- Boosted battery mode for long telephone lines and up to 85 Vrms balanced ringing
- Polarity reversal
- Small P-DSO-20-5 power package

Type	Ordering Code	Package
PEB/F 4065	on request	P-DSO-20-5

1.2 Functional Description

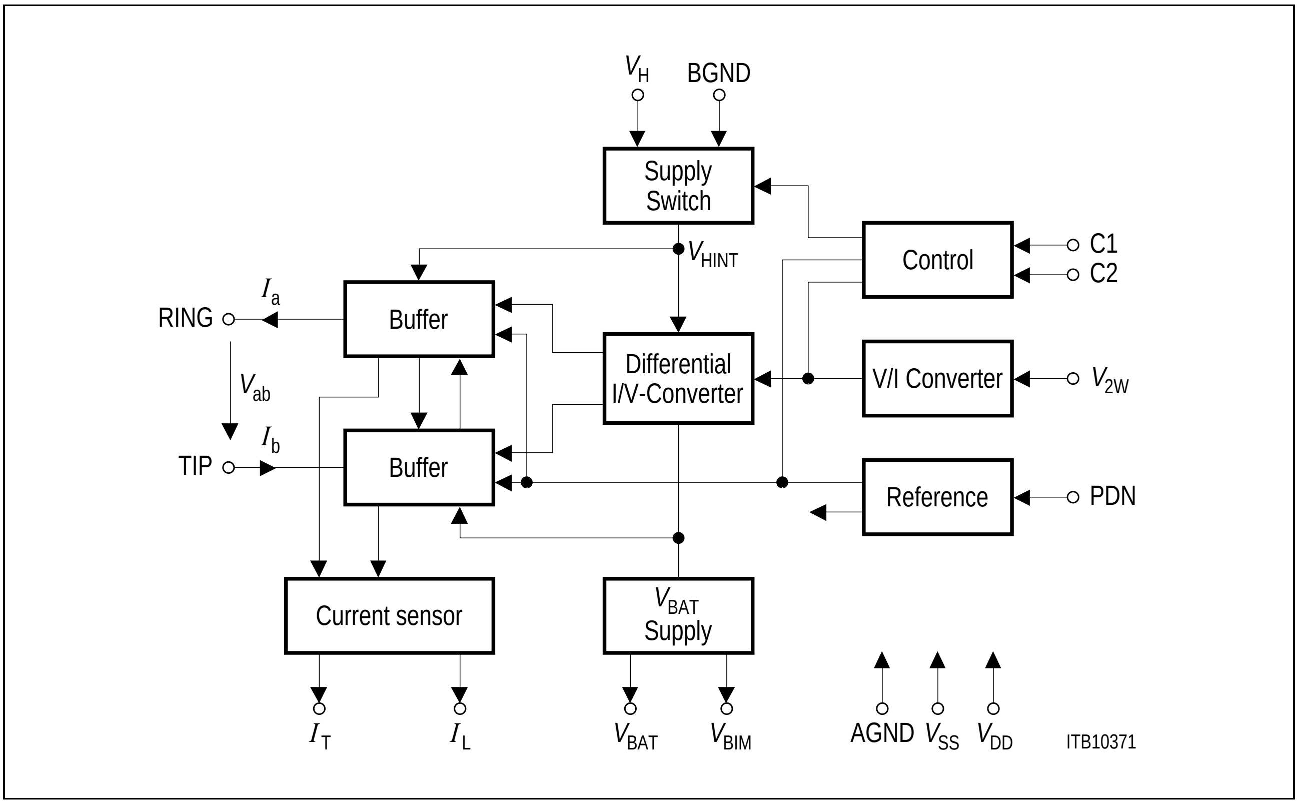


Figure 1 Block Diagram

The PEB 4065 supports AC and DC control loops based on feeding a voltage V_{ab} to the line and sensing the transversal line current I_{ab} (**Figure 2**).

It converts a unipolar input voltage V_{2W} into a differential output voltage V_{ab} with an AC receiving gain of

$$|\mathrm{Gr}| = V_{abAC}/V_{2WAC} = 40.$$

This is accomplished by converting the input voltage to a current which is used to transpose the low voltage signals of the interface to the high voltage line feeding section. This current is reconverted to two voltages of opposite phase which are referenced to the positive and negative supply voltage, respectively. Thus the differential DC line-voltage in all normal polarity modes except ringing is related to the input voltage by

$$V_{abDC} = V_{BAT} - V_{HINT} + V_{fix} - 40 \times V_{2WDC}$$

V_{BAT} negative battery voltage

V_{HINT} internal positive supply voltage

V_{fix} internal voltage drop of supply filter (appr. 2 V).

Depending on the operation mode, V_{HINT} is switched either to V_H ($V_{HINT} = V_H - 1$ V) or to BGND ($V_{HINT} = -0.5$ V) via the supply switch.

Controlled by C2, the polarity of V_{ab} can be reversed and the DC-line-voltage then is

$$V_{abDC} = -\,(V_{BAT} - V_{HINT} + V_{fix} - 40 \times V_{2WDC}).$$

The transversal and longitudinal currents are measured in the buffers and scaled images are provided at the I_T and I_L pin, respectively:

$$I_T = (I_a + I_b)/100 = I_{ab}/50 \qquad I_L = -\,(I_a - I_b)/100 = -\,I_{Long}/50.$$

The PEB 4065 operates in four modes controlled by ternary logic signals at the C1 and C2 input. Additionally, in the active modes a polarity reversal of the output voltage can be programmed (see **Table 1**).

Power down (PD): Power consumption is reduced by decreasing bias current levels. All functions operate at some small performance reductions. In this mode each of the line outputs can be programmed to show high impedance. HI b switches off the TIP buffer, while the current through the RING output still can be measured by I_T or I_L. Programming HI a reverses the polarity and switches off the RING buffer.

Conversation (CONV): This is the regular transmit and receive mode for voiceband and teletax. The line driving section is operated between V_{BAT} and BGND.

Boosted battery (BB): In order to drive longer telephone lines an auxiliary positive battery voltage V_H is used, enabling a higher DC-voltage across the line.

Ringing (RING): This mode also uses the auxiliary voltage V_H in order to provide a balanced ring signal of up to 85 Vrms. The ring tone without any DC-component has to be switched to the V_{2W} input. Internally a DC-voltage is superimposed. This voltage is proportional to the total supply voltage $V_H - V_{BAT}$ and amounts to typically 23 V at $V_H - V_{BAT}$ = 120 V. The current sensing functions are available for ring trip detection.

The Power Denial (PDN) state is intended to reduce power consumption of the linecard to a minimum: the PEB 4065 is switched off completely by connecting the PDN pin to V_{DD}, no operation is available.

With respect to the output impedance of TIP and RING two PDN-modes have to be distinguished. A resistive one (PDNR) provides a connection of 15 kΩ each from TIP to BGND and RING to V_{BAT}, respectively, while the outputs of the buffers show high impedance (**Figure 3**).

The other mode (PDNH) offers high impedance at TIP and RING. It is entered when, in addition to connecting PDN to V_{DD}, the programming inputs C1, C2 are tied to V_{IL}.

All other combinations of C1, C2 yield the resistive power denial state PDNR.

Table 1 Programming of Operation Modes

		C2 (Pin 13)		
		V_{IL}	V_{IZ}	V_{IH}
C1 (Pin 12)	V_{IL}	RING RP	RING NP	HI a RP
	V_{IZ}	BB RP	BB NP	HI b NP
	V_{IH}	CONV RP	CONV NP	PD NP

NP Normal Polarity RP...Reverse Polarity

HI a RP Ring wire set to high impedance

HI b NP Tip wire set to high impedance

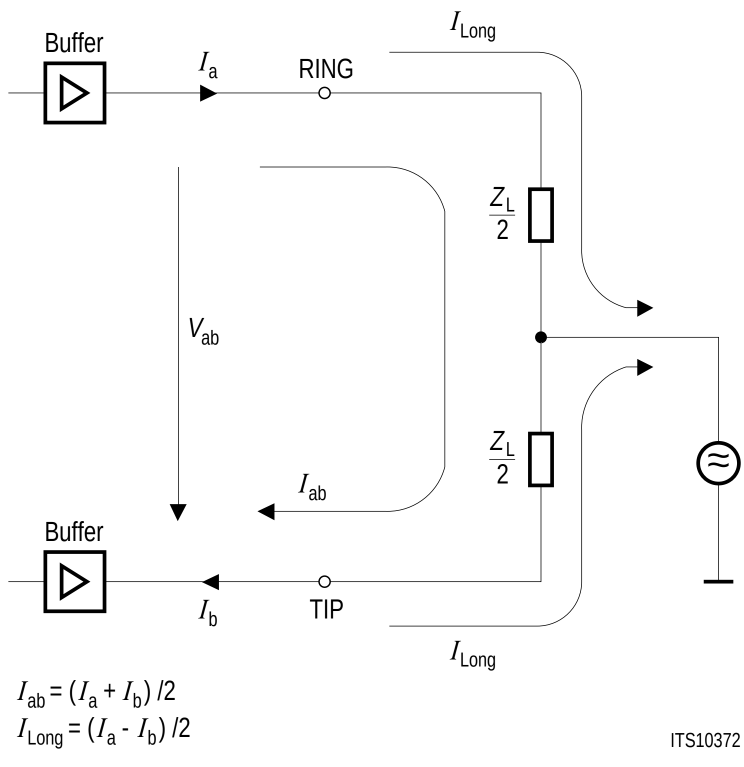


Figure 2 Definition of Output Current Directions

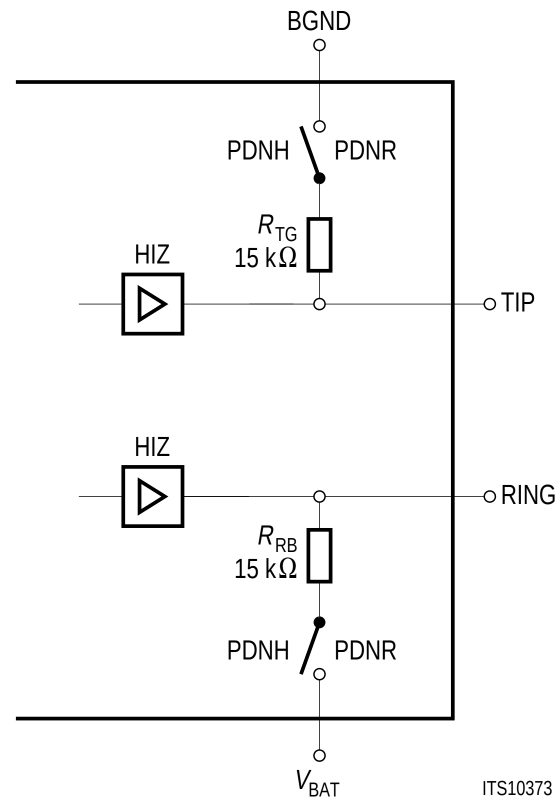
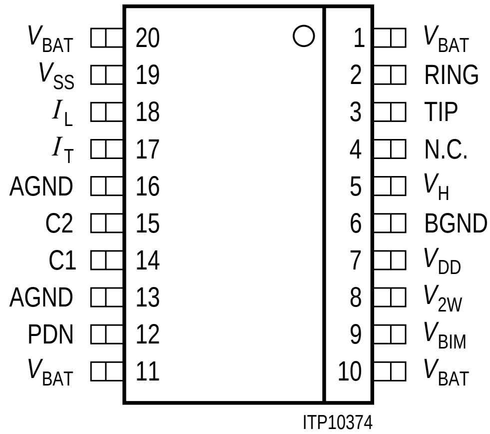


Figure 3 TIP and RING Impedance in Power Denial

1.3 Pin Description

P-DSO-20-5 (11 mm)



Due to reverse bending of the leads,
the numbering of the pins is also reversed.

Figure 4 Pin Configuration (top view)

Table 2 Pin Definition and Functions

Pin No.	Symbol	Type Input (I) Output (O)	Function
1, 10, 11, 20	V_{BAT}	Supply	Negative battery supply voltage (– 24 … – 80 V), referred to BGND
2	RING	O	Subscriber loop connection, negative wire in normal polarity; direction of positive I_a current out of this pin
3	TIP	O	Subscriber loop connection, more positive wire in normal polarity; direction of positive I_b current into this pin
4	–	N.C.	Not connected
5	V_H	Supply	Auxiliary positive battery supply voltage (0 … + 90 V) used in ringing and boosted battery mode
6	BGND	Supply	Battery ground: TIP, RING, V_{BAT} and V_H refer to this pin
7	V_{DD}	Supply	Positive supply voltage (+ 5 V), referred to AGND

Table 2 Pin Definition and Functions (cont'd)

Pin No.	Symbol	Type Input (I) Output (O)	Function
8	V_{2W}	I	Two wire input voltage; multiplied by + 20 and – 20, respectively, it appears at the TIP and RING outputs
9	V_{BIM}	O	Down scaled image of the total supply voltage (V_{HINT} – V_{BAT}); scaling factor 40
12	PDN	I/O	Power denial, reference output when connected to ground via a resistor, switches the device off when connected to V_{DD}
13, 16	AGND	Supply	Analog ground: V_{DD}, V_{SS} and all signal and control pins with exception of TIP and RING refer to AGND
14	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload this pin sinks a current of typ. 550 µA
15	C2	I	Ternary logic input, controlling the operation mode
17	I_T	O	Current output representing the transversal current scaled down by 50; In normal polarity this pin sinks the I_T current.
18	I_L	O	Current output representing the longitudinal current scaled down by 50; For I_{long} flowing out of TIP and RING this pin sinks the I_L current.
19	V_{SS}	Supply	Negative supply voltage (– 5 V), referred to AGND

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 3

Parameter	Symbol	Limit Values		Unit	Condition
		min.	**max.**		
Battery voltage	V_{BAT}	– 90	0.5	V	referred to BGND
Auxiliary supply voltage	V_{H}	– 0.5	90	V	referred to BGND
Total battery supply voltage, continuously	$V_{H} - V_{BAT}$	–	160	V	–
Total battery supply voltage, pulse < 1 ms	$V_{H} - V_{BAT}$	–	170	V	–
V_{DD} supply voltage	V_{DD}	– 0.4	5.5	V	referred to AGND
V_{SS} supply voltage	V_{SS}	– 5.5	0.4	V	referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	– 0.5	0.5	V	–
Junction temperature	T_{j}	–	150	°C	–
Input voltages	V_{2W}, V_{C1}, V_{C2}	V_{SS} – 0.3	V_{DD} + 0.3	V	–
Voltages on current outputs	V_{IT}, V_{IL}	– 3.5	V_{DD} + 0.3	V	–
Voltages on PDN	V_{PDN}	– 0.3	V_{DD} + 0.3	V	–
RING, TIP voltages, continuously	V_{a}, V_{b}	V_{BAT} – 0.3	V_{H} + 0.3	V	–
RING, TIP voltages, pulse < 1 ms[1)]	V_{a}, V_{b}	V_{BAT} – 10	V_{H} + 10	V	–
RING, TIP voltages, pulse < 1 µs[1)]	V_{a}, V_{b}	V_{BAT} – 30	V_{H} + 30	V	–
ESD-voltage, all pins	–	–	1	kV	Human body model

1) See **Test Figure 10**.

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 Operating Range

Table 4

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
Battery voltage	V_{BAT}	– 80	– 24	V	referred to BGND
Auxiliary supply voltage	V_{H}	5	85	V	referred to BGND
Total battery supply voltage	$V_{H} - V_{BAT}$	–	150	V	–
V_{DD} supply voltage	V_{DD}	4.75	5.25	V	referred to AGND
V_{SS} supply voltage	V_{SS}	– 5.25	– 4.75	V	referred to AGND
Ground voltage difference	–	– 0.3	0.3	V	–
Ambient temperature	T_{amb}	0 – 40	70 85	°C °C	PEB 4065 PEF 4065
Voltage compliance I_{T}, I_{L}	V_{IT}, V_{IL}	– 3	3	V	–
Input range V_{2W}	V_{2W}	– 3.2 – 3.2	+ 3.2 0	V V	RING CONV, PD, BB

Note: In the operating range the functions given in the circuit description are fulfilled.

2.3 Thermal Resistances

Table 5

Parameter	Symbol	Limit Values	Unit	Condition
Junction to case	$R_{th,\ jC}$	5	K/W	–
Junction to ambient	$R_{th,\ jA}$	20	K/W	with heatsink, typ.

2.4 Electrical Parameters

Min/max values are valid within the full operating range. If PEB- and PEF-specifications are different, both values can be found in the respective column.

Testing is performed according to the test figures with external circuitry as depicted in **Figure 4**. Unless otherwise stated, load impedance R_L = 600 Ω. Test temperatures are 25 and 70 °C for PEB, – 40, 25 and 85 °C for PEF-type (without heatsink). DC line voltages refer to V_{BAT} = – 70 V and V_H = + 60 V.

Table 6 Supply Currents and Power Dissipation

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Fig.
				min.	typ.	max. PEB/PEF		
Power Denial								
1.	V_{DD} current	I_{DD}	PDNH, PDNR	–	50	120/150	µA	1
2.	V_{SS} current	I_{SS}	PDNH PDNR	–	50 150	120/150 250/300	µA	1
3.	V_{BAT} current	I_{BAT}	PDNH PDNR	–	10 50	30 120	µA	1
4.	V_H current	I_H	PDNH, PDNR	–	1	10	µA	1
Power Down							**V_{2W} = – 0.5 V**[1)]	
5.	V_{DD} current	I_{DD}	PD	–	0.5	1.0	mA	1
6.	V_{SS} current	I_{SS}	PD	–	0.3	0.4	mA	1
7.	V_{BAT} current	I_{BAT}	PD	–	3.3	4.3/4.4	mA	1
8.	V_H current	I_H	PD	–	1	10	µA	1
9.	Quiescent power dissipation	P_Q	PD	–	–	315	mW	1
Conversation, Normal and Reverse Polarity							**V_{2W} = – 0.5 V**[1)]	
10.	V_{DD} current	I_{DD}	CONV	–	0.8	1.0/1.1	mA	1
11.	V_{SS} current	I_{SS}	CONV	–	0.4	0.5/0.6	mA	1
12.	V_{BAT} current	I_{BAT}	CONV	–	4.0	5.8/5.9	mA	1
13.	V_H current	I_H	CONV	–	1	10	µA	1
14.	Quiescent power dissipation	P_Q	CONV	–	–	420	mW	1

Table 6 Supply Currents and Power Dissipation (cont'd)

No.	Parameter	Symbol	Mode	Limit Values min.	Limit Values typ.	Limit Values max. PEB/PEF	Unit	Test Fig.
Boosted Battery Mode Normal and Reverse Polarity							**V_{2W} = – 0.5 V**[1)]	
15.	V_{DD} current	I_{DD}	BB	–	0.8	1.0	mA	1
16.	V_{SS} current	I_{SS}	BB	–	1.7	2.0	mA	1
17.	V_{BAT} current	I_{BAT}	BB	–	4.0	6.1/6.2	mA	1
18.	V_{H} current	I_{H}	BB	–	3.0	4.8	mA	1
19.	Quiescent power dissipation	P_{Q}	BB	–	–	740	mW	1
Ringing Mode Normal and Reverse Polarity							**V_{2W} = 0 V**	
20.	V_{DD} current	I_{DD}	RING	–	2.3	2.6	mA	1
21.	V_{SS} current	I_{SS}	RING	–	2.8	3.2	mA	1
22.	V_{BAT} current	I_{BAT}	RING	–	8.8	12/12.5	mA	1
23.	V_{H} current	I_{H}	RING	–	7.1	10	mA	1
24.	Quiescent power dissipation	P_{Q}	RING	–	1300	1500	mW	1

1) I_{BAT} and I_{H} depend on the value of V_{2W}:
$I_{BAT}(V_{2W}) = I_{BAT(0)} + |V_{2W}|/440\ \Omega$ typ. (PD, CONV, BB)
$I_{H}(V_{2W}) = I_{H(0)} + |V_{2W}|/440\ \Omega$ typ. (BB)

Table 7 DC-Characteristics

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Fig.	Test Condition
				min. PEB/ PEF	typ.	max. PEB/ PEF			
Line Termination TIP, RING									
25.	Power down DC line voltage	$\lvert V_{ab,DC}\rvert$	PD	46	49	52	V	2	V_{2W} = – 0.5 V
26.			PD	– 14	– 11	– 8	V		V_{2W} = – 2 V
27.	Conversation DC line voltage	$\lvert V_{ab,DC}\rvert$	CONV	65	66.5	68.5	V	2	V_{2W} = 0 V
28.			CONV	46.6	47.8	48.8	V		V_{2W} = – 0.5 V
29.			CONV	– 14	– 12.2	– 10.4	V		V_{2W} = – 2 V
30.	Ringing DC line voltage	$\lvert V_{ab,DC}\rvert$	RING	22.1	25	27.7	V	2	V_{2W} = 0 V
31.	Output current limit	$\lvert I_{a,max}\rvert$, $\lvert I_{b,max}\rvert$	PD others	85/80 90/85	– –	130 130/ 135	mA mA	3	V_{2W} = – 0.5 V V_a, V_b acc. to **Test Figure 3**
32.	Loop open resistance TIP to BGND	R_{TG}	PDNR	12/11	15	18/19	kΩ	9	I_b = 2 mA
33.	Loop open resistance RING to V_{BAT}	R_{RB}	PDNR	12/11	15	18/19	kΩ		I_a = 2 mA
34.	Power denial output leakage current	$I_{Leak,a}$	PDNH	– 30	–	30	μA	–	$V_{BAT} < V_a < V_H$
35.		$I_{Leak,b}$		– 30	–	30	μA		$V_{BAT} < V_a < V_H$
36.	High impedance output leakage current	$I_{Leak,a}$	HI a	– 30	–	30	μA	–	$V_{BAT} < V_a < V_{H-3}$
37.		$I_{leak,b}$	HI b	– 30	–	30	μA		$V_{BAT} < V_b < V_{H-3}$

Table 7 DC-Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values min. PEB/PEF	typ.	max. PEB/PEF	Unit	Test Fig.	Test Condition
Reference Voltage Outputs PDN, V_{BIM}									
38.	Output voltage on PDN	V_{ref}	all	1.15	1.25	1.35	V	1	–
39.	Battery image voltage	V_{BIM}	CONV, PD	– 1.75	– 1.7	– 1.65	V	1	–
40.			BB, RING	– 3.25	– 3.18	– 3.1	V		
Two-wire Input V_{2W}									
41.	Input current	I_{2W}	all	– 30	–	30	µA	–	$-3.2\ V < V_{2W} < 3.2\ V$
42.	Input capacitance	–	–	–	–	20	pF	–	–
Current Outputs I_T, I_L									**V_{2W} = – 0.5 V**
43.	I_T output current	$\|I_T\|$	PD, CONV	–	–	15	µA	2	$I_a = I_b = 0$
44.			PD, CONV	380		420	µA		$I_a = I_b$ = 20 mA[1)]
45.			CONV	0.95		1.05	mA		$I_a = I_b$ = 50mA[1)]
46.			RING			20	µA		$I_a = I_b = 0$
47.	I_L output current	$\|I_L\|$	PD, CONV	–	–	30	µA	2	$I_a = I_b = 0$
48.			PD, CONV			30	µA		$I_a = I_b$ = 20 mA[1)]
49.			PD, CONV	65		135	µA		I_a = 15 mA, I_b = 25 mA
50.			CONV	180		320	µA		I_a = 37.5 mA, I_b = 62.5 mA

Table 7 DC-Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Fig.	Test Condition
				min. PEB/ PEF	typ.	max. PEB/ PEF			
Control Inputs C1, C2									
51.	H-input voltage	V_{IH}	all	2	–	–	V	–	–
52.	Z-input voltage	V_{IZ}	all	– 0.8	–	0.8	V	–	–
53.	L-input voltage	V_{IL}	all	–	–	– 2	V	–	–
54.	Input leakage current	I_{Leak}	all	– 5	–	5	µA	–	– 5 V < $V_{C1(2)}$ < + 5 V
55.	Thermal overload current C1	I_{therm}	all	500	550	–	µA	–	V_{C1} = – 3.2 V
56.	Switching Temperature (guaranteed by design)	T_{joff} T_{jon}	all all	– –	165 145	– –	°C °C	– –	– –

[1] Polarity of I_a and I_b is reversed for measurement in reverse polarity mode

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

2.5 AC-Characteristics

(Normal and reverse polarity unless otherwise stated)

Table 8

No.	Parameter	Symbol	Mode	Limit Values min.	Limit Values typ.	Limit Values max. PEB/PEF	Unit	Test Fig.	Test Condition
Line Termination TIP, RING									
	Receive gain	Gr						4	$V_{2W,AC}$ = 50 mVrms f = 1015 Hz
57.			CONV, BB	31.92	32.04	32.16	dB		I_{ab} = 20 mA
58.			CONV	31.88	32.04	32.2	dB		I_{ab} = 50 mA
59.	Gain flatness (guaranteed by design)	dGr	CONV, BB	– 0.05	–	0.05	dB	–	300 Hz < f < 3400 Hz $V_{2W,AC}$ = 50 mVrms
60.	Gain tracking (guaranteed by design)	dGr	CONV	– 0.2	–	0.2	dB	–	3 dBm0 > V_{ab} > – 20 dBm0 f = 1015 Hz
61.	Total harmonic distortion V_{ab}	THD	CONV	–	–	0.3	%	4	$V_{2W,AC}$ = 50 mVrms f = 1015 Hz I_{ab} = 20 mA
	Teletax distortion	THDTTX	CONV					5	f = 16 kHz R_L = 200 Ω I_{ab} = 50 mA
62.				–	–	3	%		$V_{ab,AC}$ = 2 Vrms
63.				–	–	3	%		$V_{ab,AC}$ = 5 Vrms I_{ab} = 0 mA, V_{ab} = 55 V
64.				–	–	5	%		$V_{ab,AC}$ = 2 Vrms
65.	Psophometric noise	N_P, V_{ab}	CONV	–	–	– 75	dBmp	4	I_{ab} = 30 mA
66.	Longitudinal to transversal rejection ratio V_{long}/V_{ab}	LTRR	CONV	61/58	–	–	dB	6	V_{long} = 3 Vrms 300 Hz < f < 3.4 kHz I_{ab} = 30 mA
67.	Transversal to longitudinal rejection ratio V_{ab}/V_{long}	TLRR	CONV	50	–	–	dB	7	$V_{2W,AC}$ = 150 mVrms 300 Hz < f < 3.4 kHz I_{ab} = 30 mA

Table 8 (cont'd)

No.	Parameter	Symbol	Mode	Limit Values min.	typ.	max. PEB/ PEF	Unit	Test Fig.	Test Condition
	Power supply rejection ratio	PSRR						4	300 Hz < f < 3.4 kHz $V_{Supply,AC}$ = 100 mVp I_{ab} = 30 mA
68.	V_{BAT}/V_{ab}		CONV, BB PD	33 30/28	40 –	– –	dB dB		
69.	V_H/V_{ab}		BB	33/30	40	–	dB		
70.	V_{DD}/V_{ab}		CONV, BB	33	50	–	dB		
71.	V_{SS}/V_{ab}		CONV, BB	33	50 25	–	dB dB		
72.	Ringing voltage	V_{RING}	RING	67	–	–	Vrms, diff	8	R_L = 1 kΩ C_L = 1 µF f = 66 Hz V_{2W} = 1.7 Vrms
73.	Ringing voltage with extended V_H			84	–	–	Vrms, diff	8	V_H = 80 V f = 20 Hz V_{2W} = 2.2 Vrms
74.	Ringing distortion	THD	RING	–	–	4	%	8	f = 66 Hz V_{2W} = 1.7 Vrms
Transversal Current Output I_T									
	Transversal current ratio	Git						4	V_{2W} = 50 mVrms f = 1015 Hz
75.			CONV, BB	33.89	33.98	34.07	dB		I_{ab} = 20 mA
76.			CONV	33.89	33.98	34.07	dB		I_{ab} = 50 mA
77.	Gain flatness (guaranteed by design)	dGit	CONV, BB	– 0.05	–	0.05	dB	–	300 Hz < f < 3400 Hz $V_{2W,AC}$ = 50 mVrms I_{ab} = 20 mA
78.	Gain tracking (guaranteed by design)	dGit	CONV	– 0.2	–	0.2	dB	–	3 dBm0 > V_{ab} > – 20 dBm0 f = 1015 Hz
79.	Total harmonic distortion V_{IT}	THD, I_T	CONV	–	0.01	0.3	%	4	$V_{2W,AC}$ = 50 mVrms f = 1015 Hz I_{ab} = 15 mA

Table 8 (cont'd)

No.	Parameter	Symbol	Mode	Limit Values min.	Limit Values typ.	Limit Values max. PEB/ PEF	Unit	Test Fig.	Test Condition
80.	Psophometric noise	N_P, V_{IT}	CONV	–	–	– 100 -97	dBmp	4	I_{ab} = 30 mA, T>0^0C -40^0C<T<0^0C
	Frequency response V_{IT}/V_{2W} (guaranteed by design)	–	CONV					4	f = 200 kHz $V_{2W,AC}$ = 50 mVrms I_{Line} = 20 mA C_S = 0.2 nF
81.	Amplitude			– 0.5	1.7	1.95	dB		
82.	Phase			100	–	–	deg		
	Longitudinal to transversal current output rejection ratio V_{long}/V_{IT}	LITRR	CONV					6	V_{long} = 3 Vrms I_{ab} = 30 mA
83.				75	–	–	dB		300 Hz < f < 3.4 kHz
84.				81	–	–	dB		f = 1015 Hz
	Power supply rejection ratio	PSRR						4	300 Hz < f < 3.4 kHz $V_{supply,AC}$ = 100 mVp I_{ab} = 30 mA
85.	V_{BAT}/V_{IT}		CONV, PD	50	60	–	dB		
86.	V_H/V_{IT}		BB	50	60	–	dB		
87.	V_{DD}/V_{IT}		CONV	50	60	–	dB		
88.	V_{SS}/V_{IT}		CONV	50	60	–	dB		

Table 9 External Elements in the Application Circuit (Figure 5)
Typical values are used in the test circuits, unless otherwise specified.

Ext. Part	Function	Typ. Value	Tolerance	Limit Values		Comment
				min.	max.	
R_1	Biasing, current reference	25 kΩ	–	–	50 kΩ	power dissipation increases with smaller R_1
R_2, R_3	I_T, I_L gain adjustment	1 kΩ	0.1% (rel.)	–	–	clipping for $I_T \times R_2$ > 3 V or $I_L \times R_3$ > 3 V
R_S	Protection, isolation of capacitive load	50 Ω	0.1% (rel.)	30 Ω	–	–
R_5, R_6	Protection	50 Ω	0.1% (rel.)	–	–	–
C_1	C for the internal supply voltage filter	22 µF ($f_{3dB} \approx$ 3 Hz)	20%	10 nF	–	f_{3dB} increases with smaller C_1, causing worse low frequency PSRR from V_{BAT}
C_S	Suppression of voltage spikes, frequency compensation	15 nF	5% (rel.)	200 pF	20 nF	–
C_2, C_3	V_{DD}, V_{SS} supply voltage blocking	1 µF	20%	10 nF	–	C_2, C_3 > 1 µF and $C_4 \approx C_5$ allows arbitrary switching sequence of all supply voltages incl.
C_4	V_H blocking	100 nF	–	–	–	
C_5	V_{BAT} blocking	100 nF	20%	100 nF	–	ground

Note: Exceeding the min./max. limits can cause stability problems!

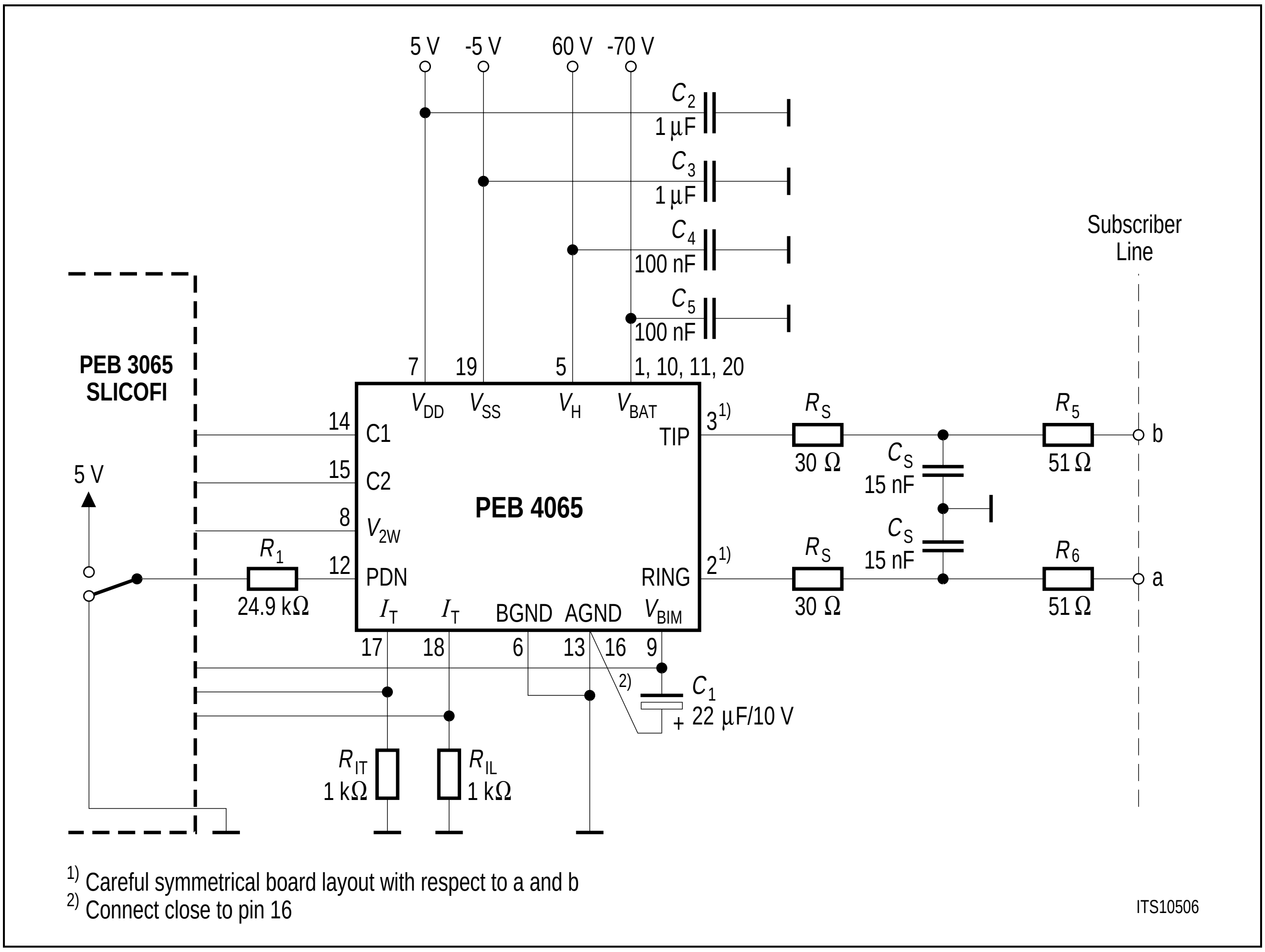
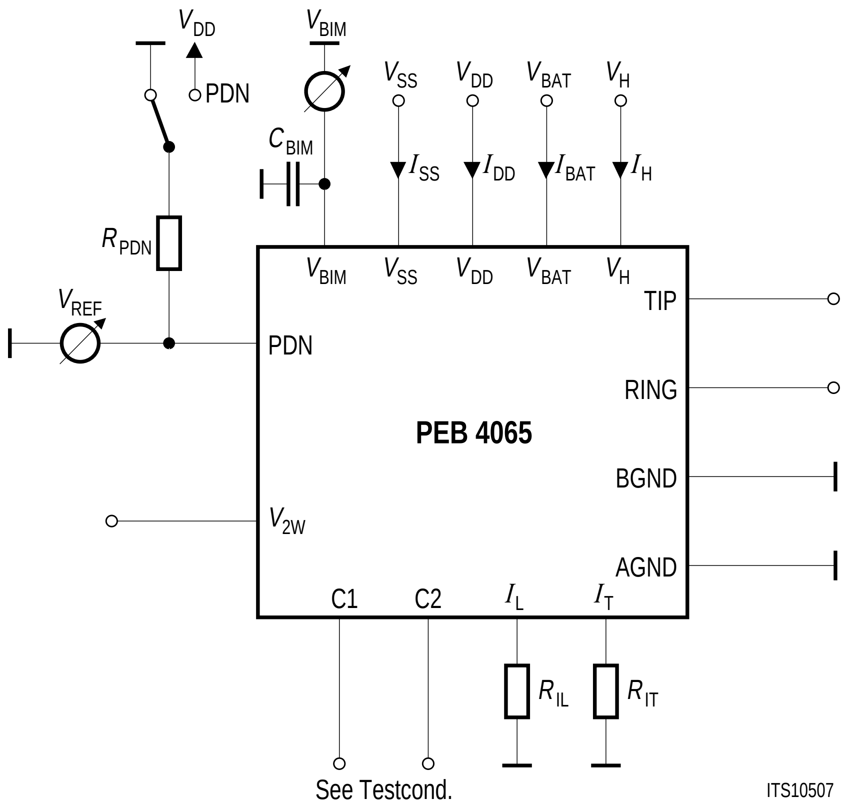
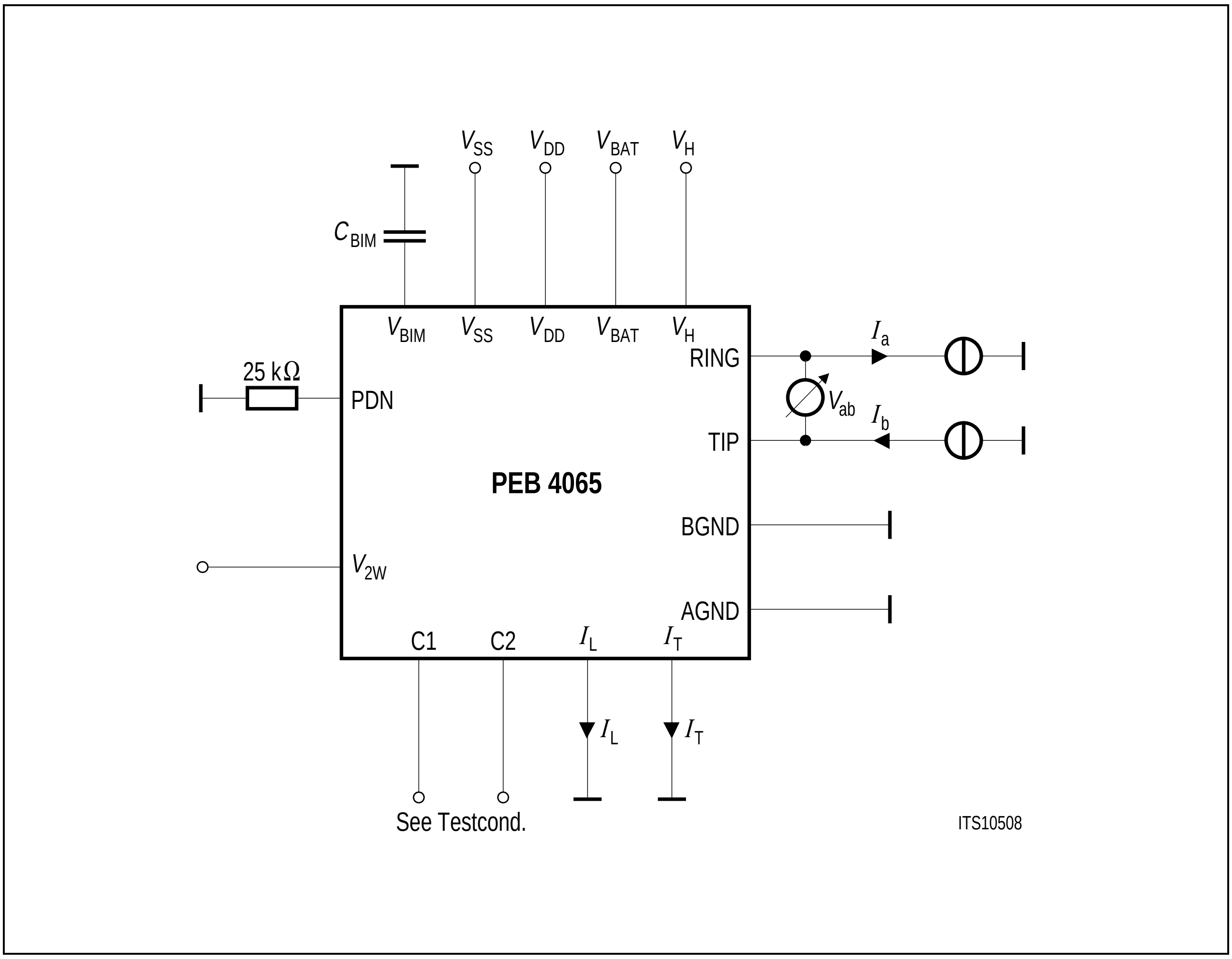


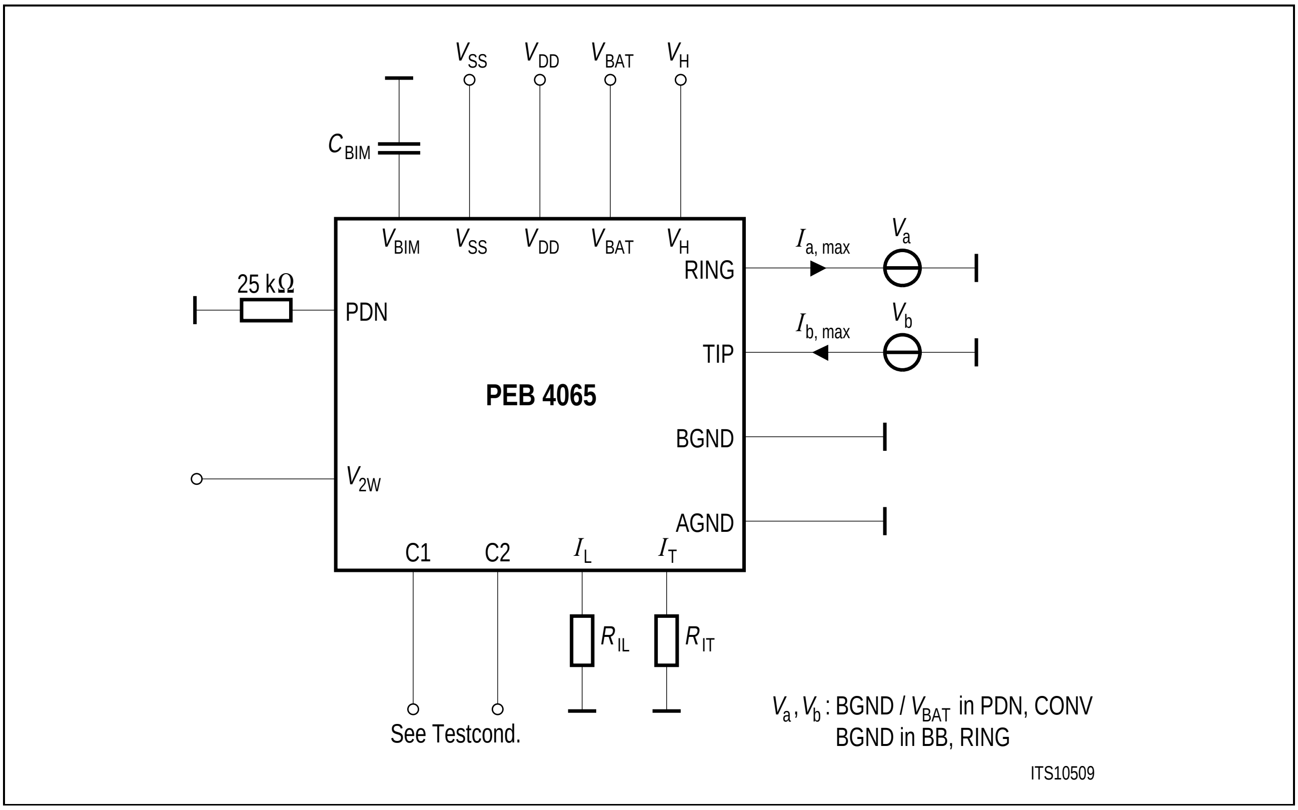
Figure 5 Application Circuit



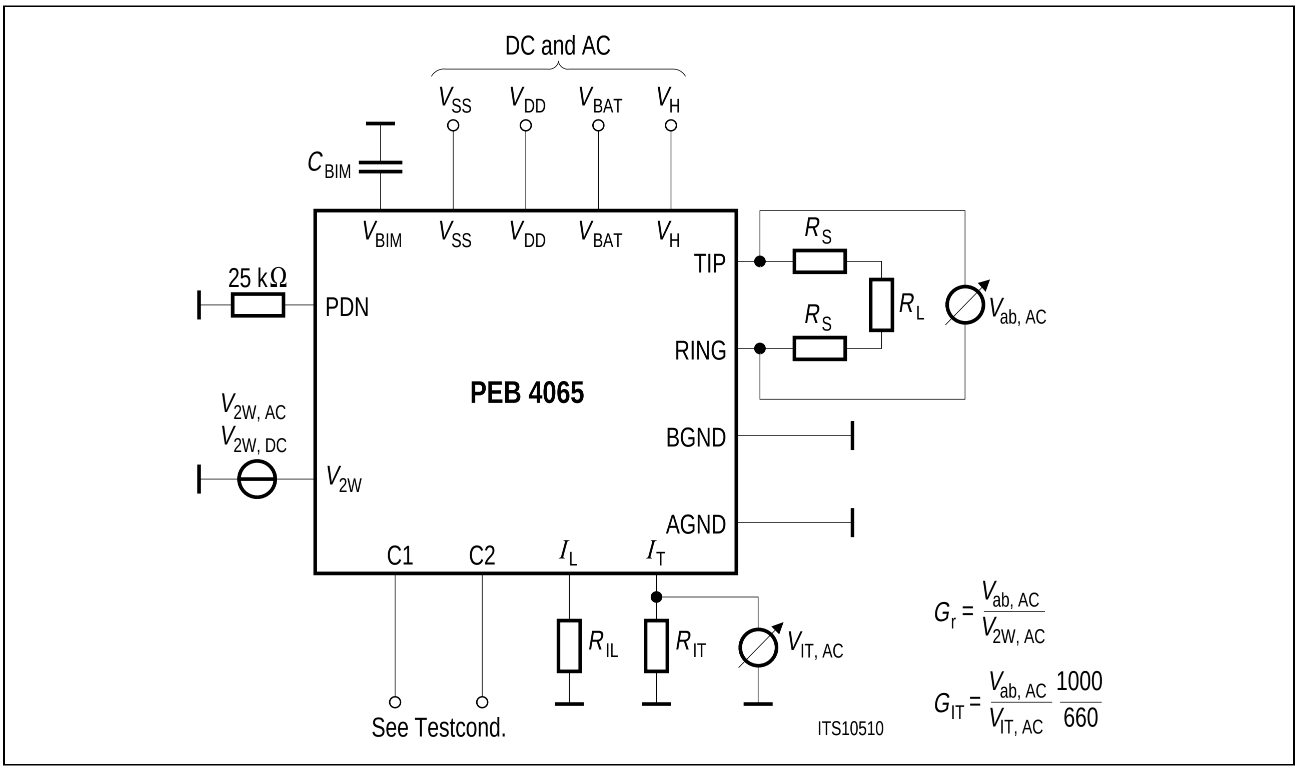
Test Figure 1 DC Characteristics and Power Dissipation



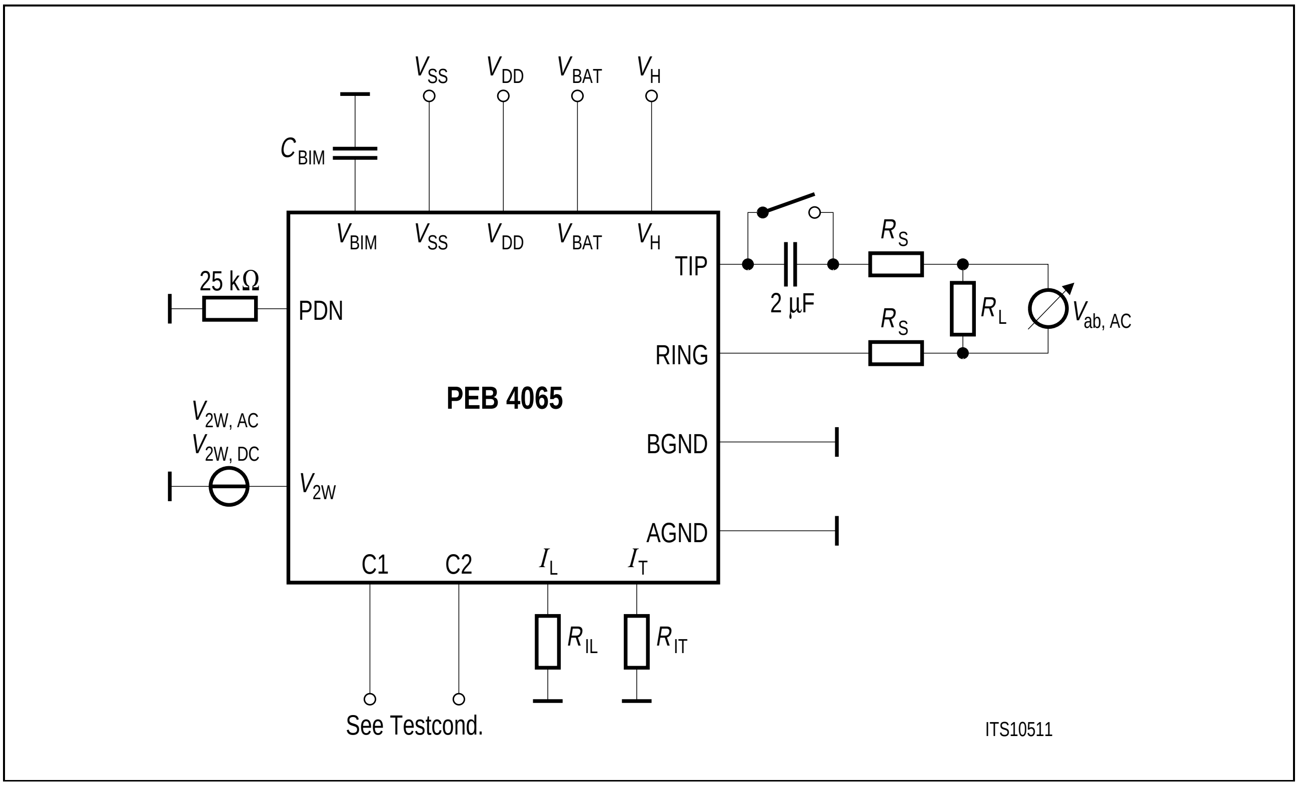
Test Figure 2 DC Line Voltage and Currents



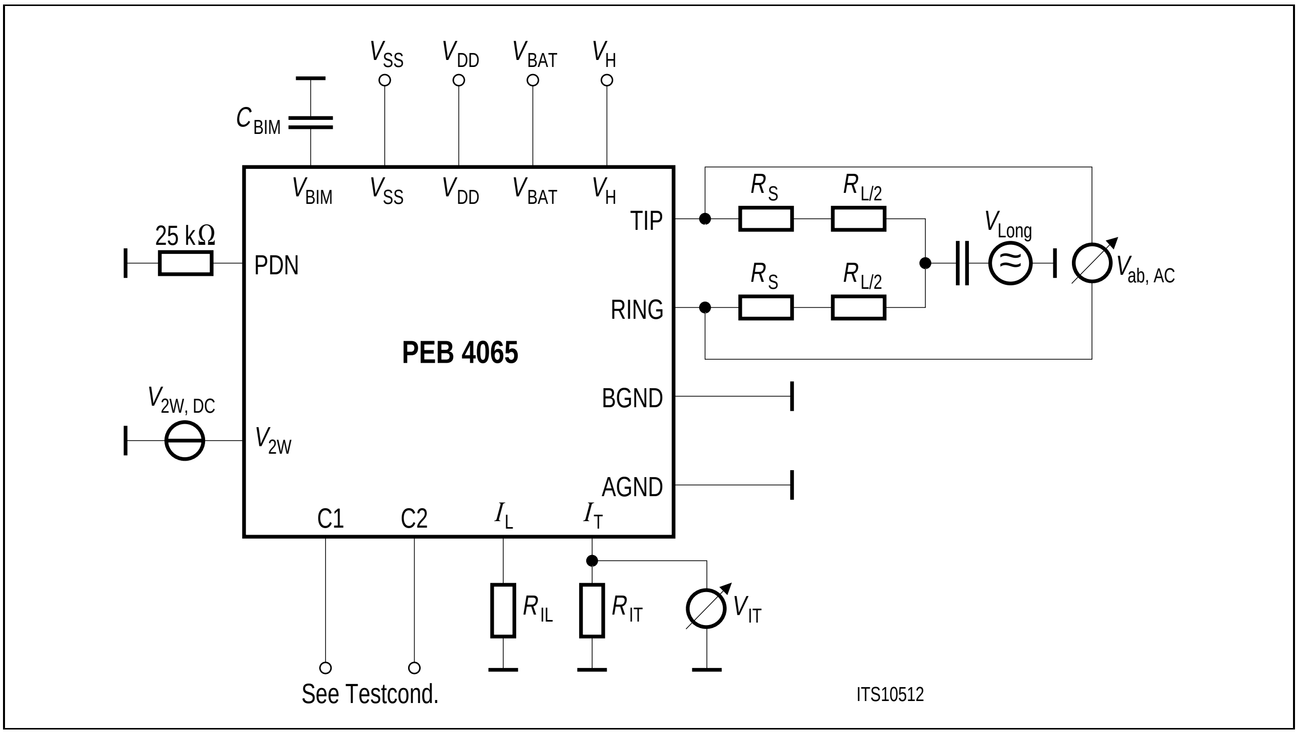
Test Figure 3 Output Current Limit



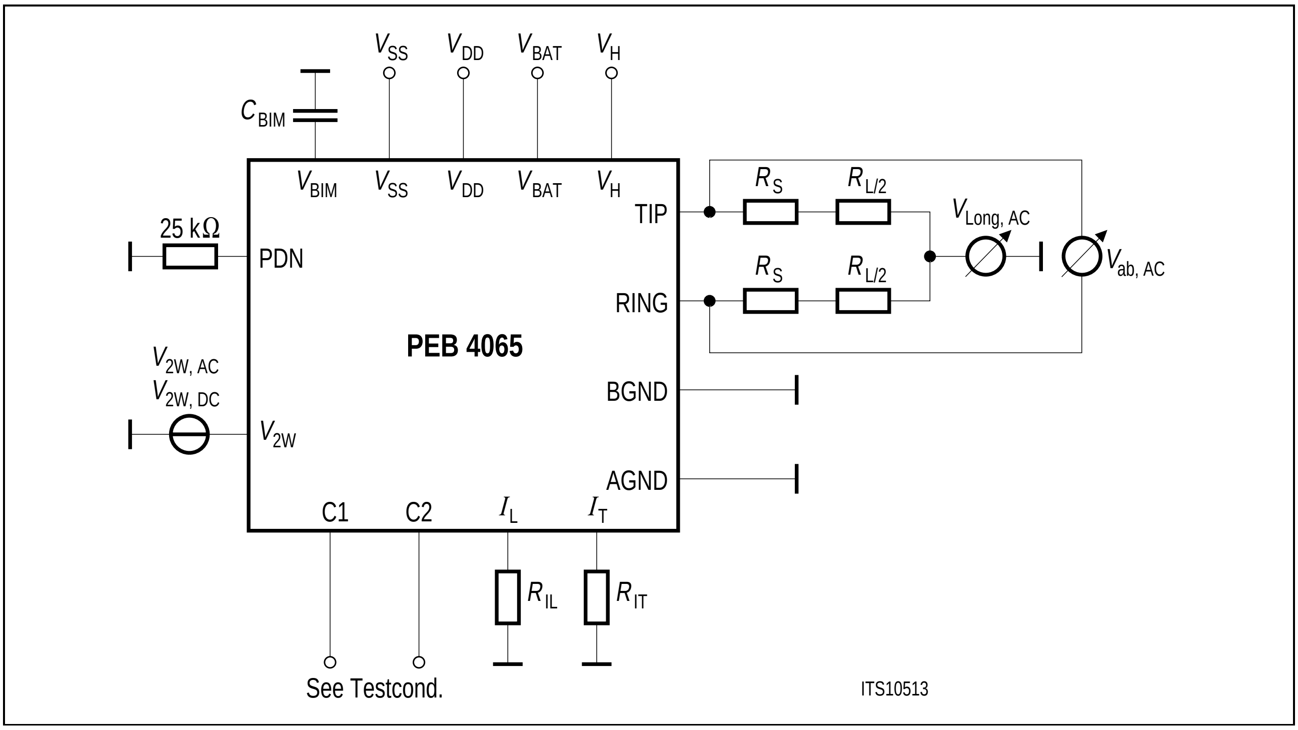
Test Figure 4 Receive Gain, Transversal Current Ratio, THD, Noise and Power Supply Rejection



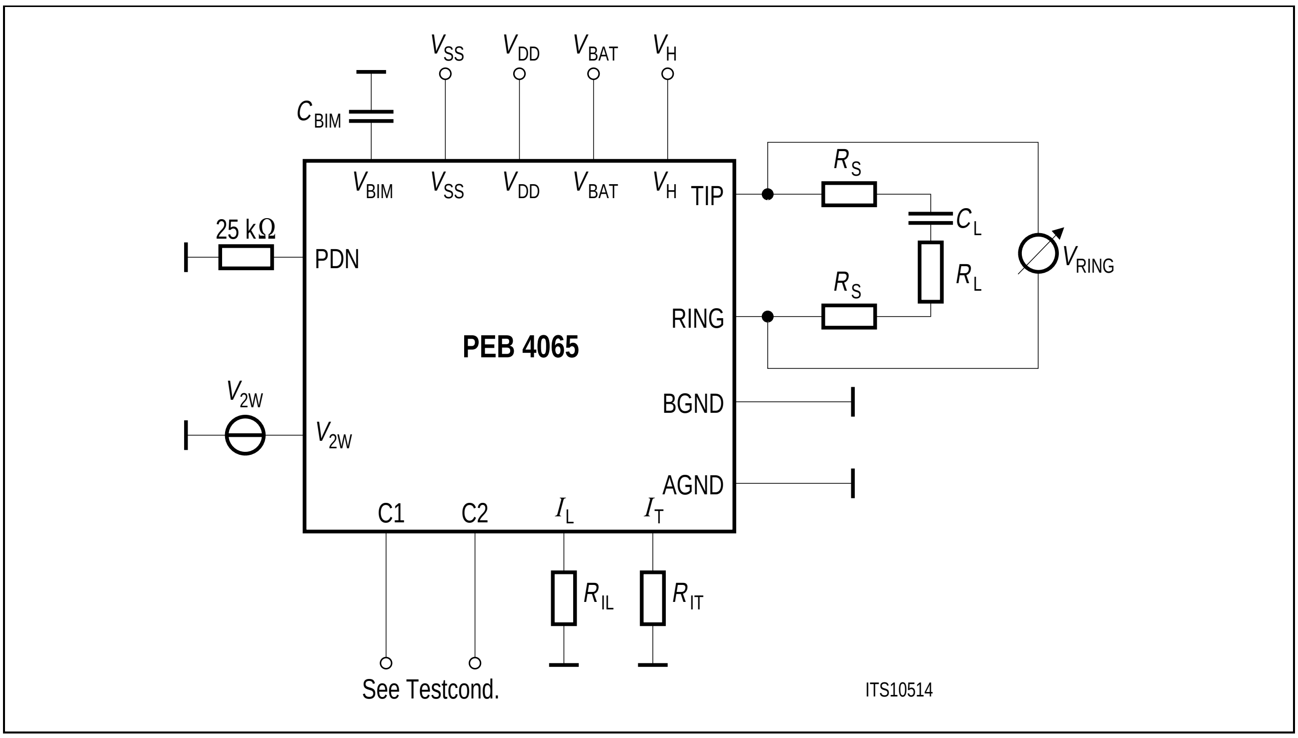
Test Figure 5 Teletax Distortion



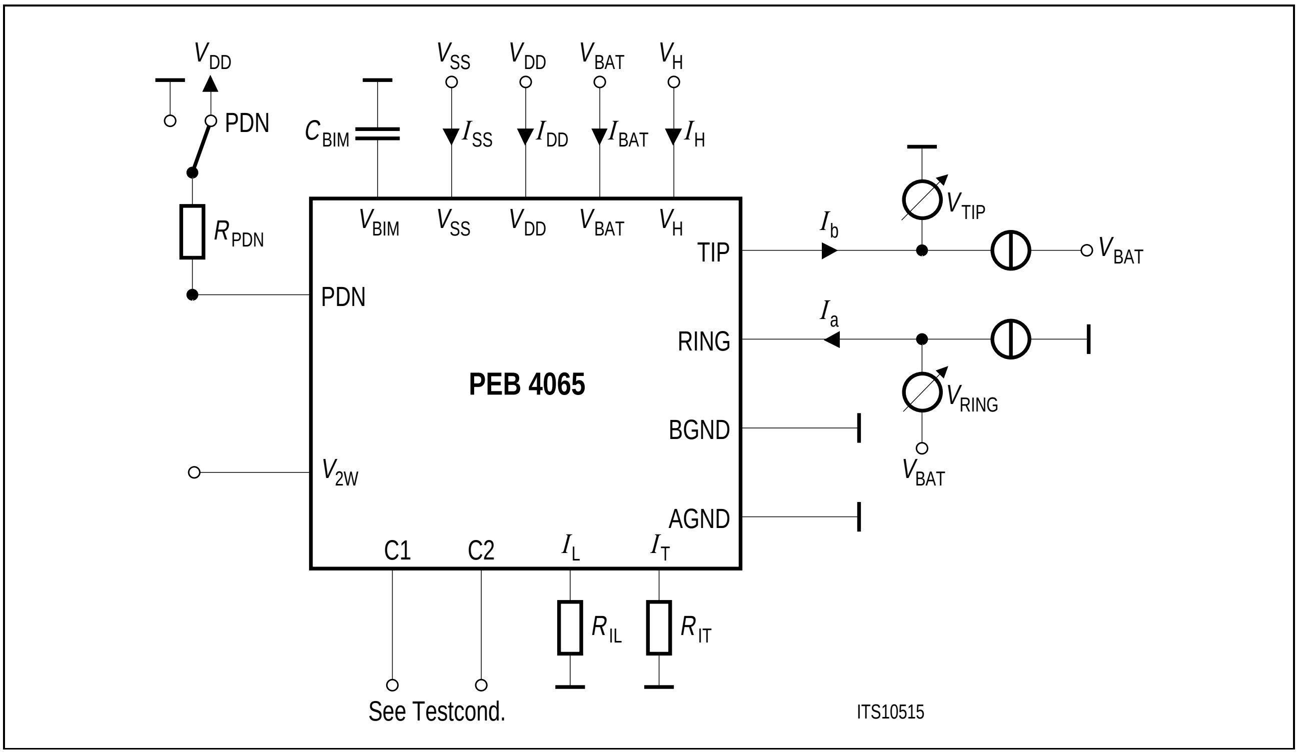
Test Figure 6 Longitudinal to Transversal Rejection Ratio



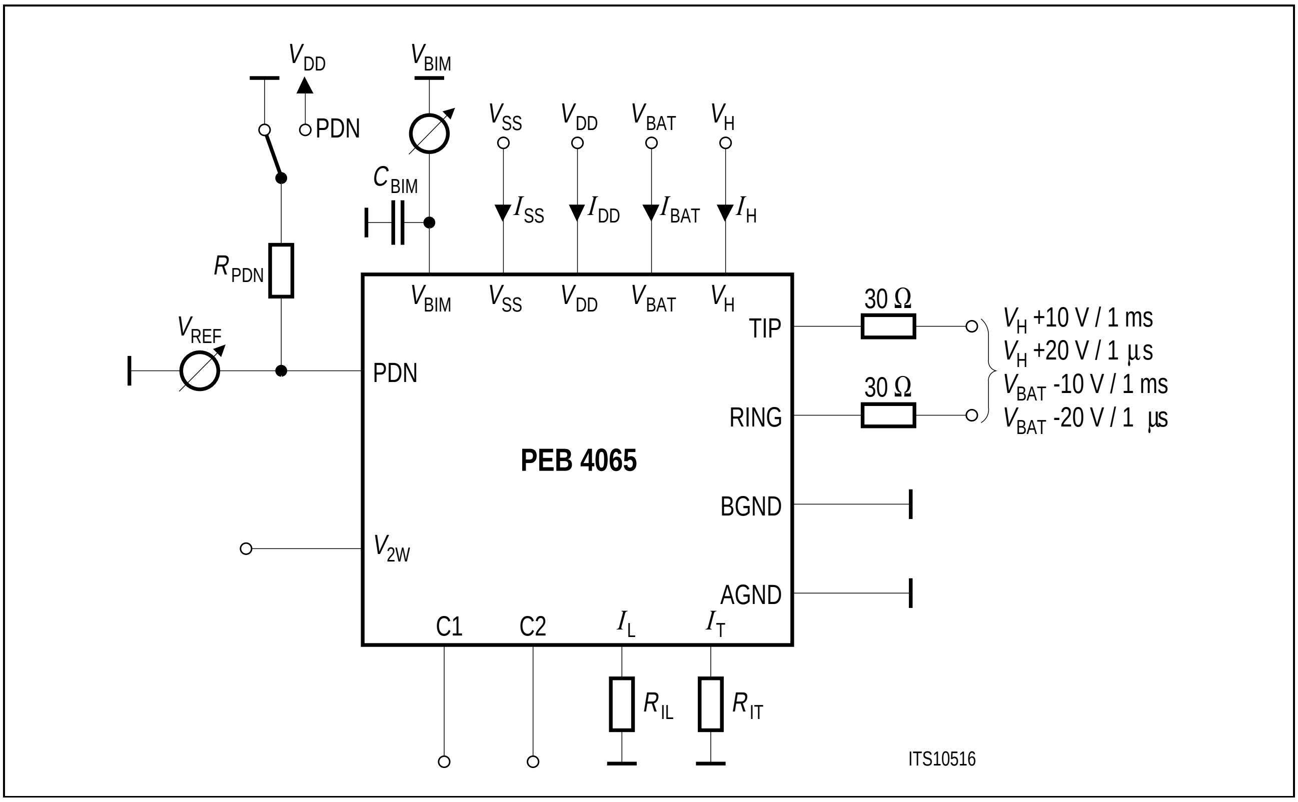
Test Figure 7 Transversal to Longitudinal Rejection Ratio



Test Figure 8 Ringing



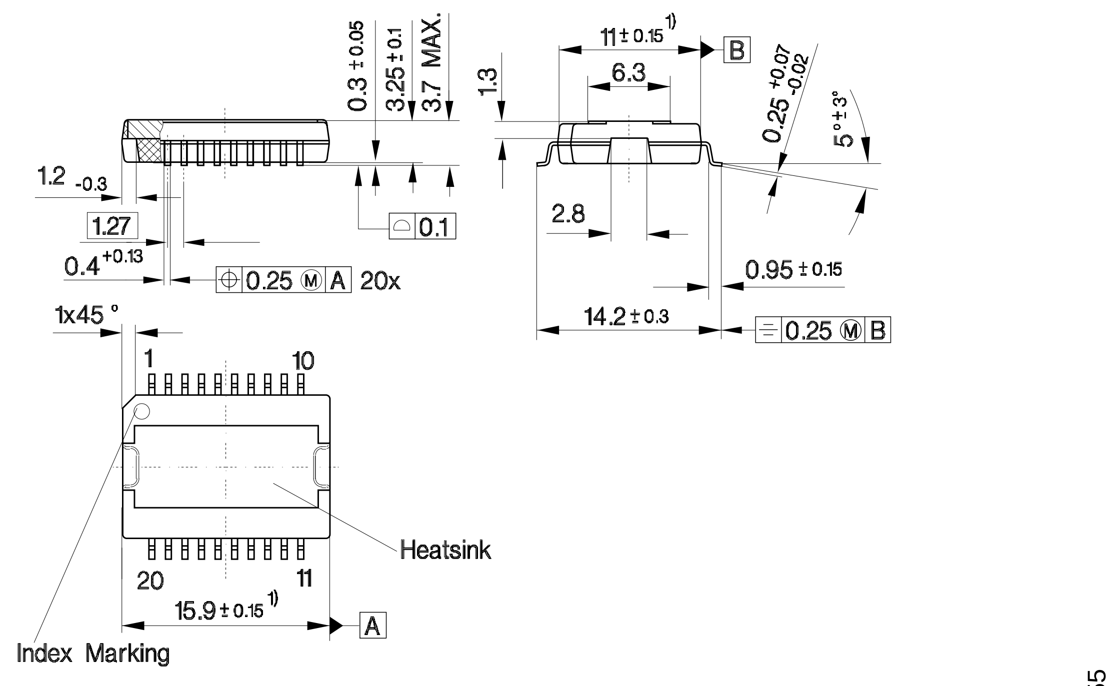
Test Figure 9 Output Resistance in PDNR Mode



Test Figure 10 TIP, RING Overvoltage Pulses

3 Package Outlines

P-DSO-20-5
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm